LSI402ZX Digital Signal Processor

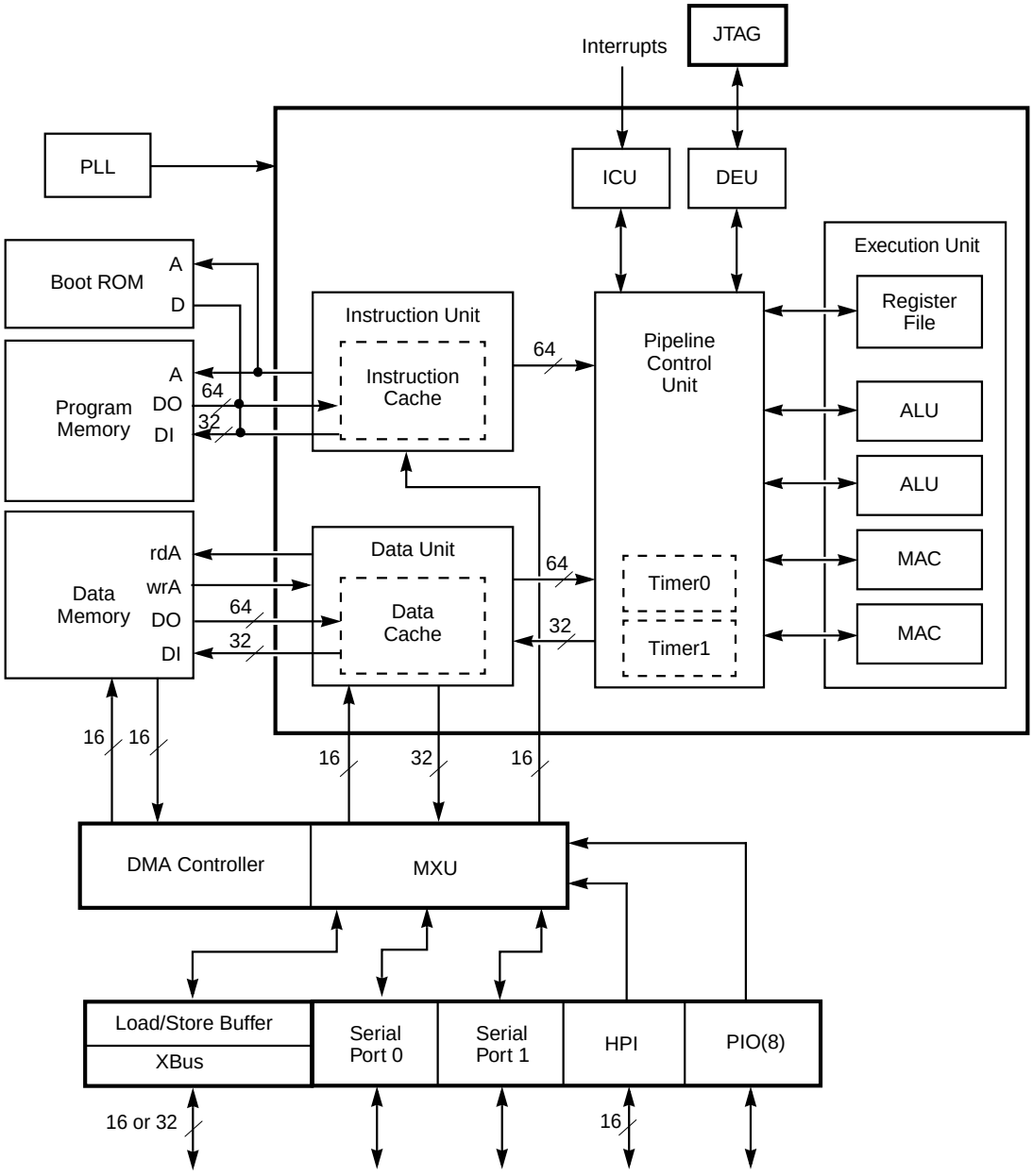
Preliminary Datasheet

The LSI402ZX is a 16-bit fixed-point digital signal processor (DSP) based on the LSI Logic ZSP400 DSP core. The LSI402ZX contains an entire DSP system on a single chip, and is designed for applications requiring high throughput and flexibility coupled with a high speed I/O, such as communications infrastructure equipment.

The LSI402ZX operates at a clock rate of 200 MHz for a maximum effective throughput of 800 RISC-like MIPS. The LSI402ZX RISC architecture is easy to program and uses a four-way superscalar pipeline with five stages to process up to 20 instructions at a time. The processor's execution unit contains two multiply-accumulate units (MACs) and two arithmetic logic units (ALUs). The LSI402ZX also supports single cycle add-compare-select, bit manipulation, and 32-bit arithmetic and logic operations.

Figure 1 shows a block diagram of the LSI402ZX.

Figure 1 LSI402ZX Block Diagram



MXU = External Memory Interface Unit
HPI = Host Processor Interface
PIO = Programmable I/O

ICU = Interrupt Control Unit
DEU = Device Emulation Unit
XBus = External Bus

The LSI402ZX provides 62 Kwords of on-chip instruction zero wait-state RAM and 62 Kwords of on-chip data zero wait-state RAM supported by an eight channel DMA controller, which can transfer instructions and data. For optimum I/O performance and flexibility, the LSI402ZX contains two high speed time-division multiplex (TDM) serial ports, a single 16-bit host interface port, an external memory interface unit, and an eight-pin programmable I/O port. An IEEE 1149.1 JTAG port supports program download and debug.

LSI Logic provides a software development kit containing an assembler, linker, GUI debugger, simulator, C compiler, and JTAG-based hardware emulator.

The LSI402ZX is fabricated in the LSI Logic G12™-p technology. The LSI402ZX is powered by a 1.8 V core and a 3.3 V I/O supply, and is packaged in a 208-ball mini-BGA package.

LSI402ZX Features

Processor

- RISC architecture
  - Instruction grouping by hardware for parallel execution
- Four-way superscalar architecture
  - Two multiply-accumulate units (MACs)
  - Two arithmetic logic units (ALUs)
- 800 RISC-like MIPS maximum throughput at 200 MHz
- Multitasking support
  - Low latency interrupt structure with programmable priority levels
  - Efficient context switch support
- On-chip PLL for clock generation

Applications

- Optimized for communications infrastructure applications
  - Single-cycle dual 16-bit MAC with 40-bit result
  - Single-cycle high-precision (32-bit) MAC with 40-bit result
  - Two-cycle complex multiply
  - Single-cycle add-compare-select for Viterbi decoding

Technology

- 208-ball mini-BGA package

Memory

- 62 Kword internal instruction RAM
- 62 Kword internal data RAM
- Eight channel DMA controller
  - Supports fast I/O transfers
  - Transfer instructions or data to and from internal memory
- 32-bit external memory interface unit
  - Glueless interface to SBSRAMs
  - 20-bit address space (2 Mwords) for both instruction and data memory
- Glueless interface to 16-bit SRAMs and peripherals
- 2 Kword internal boot ROM

I/O

- Two high-speed serial ports with TDM mode
  - H.100/H.110 bit stream compatible
- 8/16-bit host processor interface
- 8-pin programmable I/O port
- IEEE 1149.1 compliant JTAG port

Timers

- Two 16-bit timers with a 6-bit prescale value
- Single-shot and continuous mode

Functional Description

The LSI402ZX contains an entire DSP system and allows attachment of external memory and peripherals. Refer to Figure 1 for a block diagram of the LSI402ZX.

The pipeline control unit attempts to group instructions for parallel execution, resolving data and resource dependencies in the program sequence. By scheduling instructions for execution by the four functional units (the two MACs and two ALUs), it relieves the programmer and the compiler of this task. The pipeline control unit also synchronizes the entire operation of the pipeline and processes interrupt requests.

The LSI402ZX is a four-way superscalar processor that employs a five-stage pipeline. At any time, there may be a maximum of twenty instructions in various stages of execution in the pipeline. The five pipeline stages of this machine are Fetch/Decode (F/D), Group (G), Read (R), Execute (E), and Write Back (W).

The pipeline control unit also contains two 16-bit timers for interrupt generation. Each timer is fully programmable and has a 6-bit prescaler. Once enabled, the timers count down from the user-specified initial value to zero at a rate determined by the scaled output of the LSI402ZX output clock. The timers generate an interrupt when zero is reached. The timers can be configured to automatically reload with the initial count to generate periodic interrupts.

The interrupt control unit interfaces with the pipeline control unit. A nonmaskable interrupt (NMI) pin into the LSI402ZX allows for a separate interrupt control unit.

The data unit fetches data and sends them to the data cache. The data unit contains the data prefetcher and cache, and contains the logic for two circular buffers.

The instruction unit fetches instructions, decodes and dispatches them, and places the instructions in the instruction cache. The instruction unit contains the instruction cache, the instruction prefetcher, and the instruction dispatch unit. The instruction unit also contains branch prediction logic.

The control register file contains a set of 16-bit control registers, used for mode control as well as status and flag information.

The execution unit performs all arithmetic and logical operations in the LSI402ZX. The execution unit contains two 16-bit arithmetic logic units (ALUs), two 16 x 16 multiply and accumulate (MAC) units, and a general purpose (operand) register file.

The two ALUs are identical and can be combined as a single 32-bit ALU. The MAC units can perform two 16-bit x 16-bit multiply operations and a single 40-bit accumulation per cycle or one 32-bit x 32-bit multiply operation and a single 40-bit accumulation per cycle.

The LSI402ZX contains a 2 Kword internal boot ROM that provides self-test and debugging capabilities, as well as the ability to download code to instruction memory through the host processor interface. The boot ROM supports debugging through the JTAG port.

The LSI402ZX provides an eight-channel DMA controller. Each channel supports zero-overhead instruction or data transfers to or from the entire contents of internal instruction and/or data RAM to either the external memory interface unit, one of the serial ports, or the host processor interface. The eight DMA channels are segmented between four nonindexed and four indexed channels.

Nonindexed DMA channels perform only sequential accesses to or from internal memory. A transfer occurs at the specified memory location whenever an interrupt from the specified peripheral occurs. The interrupt request may come from the host processor interface or one of the two serial ports. After the interrupt, the pointer register updates with the next internal memory location. When the DMA channel pointer reaches the buffer length, the processor generates a DMA interrupt request and terminates the DMA transaction.

Indexed DMA channels perform sequential or indexed accesses to or from internal memory. These channels are designed specifically to work with the TDM serial ports, but can be used with other devices in nonindexed mode. Data buffers can read from or write to DSP memory corresponding to logical TDM channels (time slots). The user specifies the buffer length and the number of buffers to service, and the DMA controller automatically updates the pointer for each transfer within a frame. When a frame transfer completes, the pointer updates the memory address and begins transferring data for the next frame. When

the DMA channel pointer reaches the last location of the last buffer, the processor generates a DMA interrupt and sets the bit corresponding to the channel in the DMA status register. This terminates the DMA transaction.

The external memory interface unit connects the LSI402ZX to off-chip memory or peripherals through a 32-bit data bus and an 18-bit address bus. The external memory interface unit provides a glueless interface to 16-bit asynchronous memory devices (ROM, EPROM, and SRAM) and 32-bit synchronous-burst SRAMs (SBSRAM). An external memory page register extends the external memory space to 20-bits.

The LSI402ZX contains two identical synchronous serial ports that support 8-bit or 16-bit transfers. The serial ports are capable of generating their own bit clock and frame sync signals. The maximum transfer rate in either active or passive mode is one-half the processor clock rate. The serial ports support burst, continuous, and TDM mode transfers.

Both serial ports of the LSI402ZX provide a TDM mode compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals. The user selects the word length (8- or 16-bits) and frame length (1–128 time slots) for TDM transfers. Transmit and receive time slots are programmed individually and can be modified on the fly.

The host processor interface (HPI) is an asynchronous 8 or 16-bit parallel port. The port is passive only. The HPI supports Motorola and Intel style memory interfaces, and supports word transfers in both modes. The active level of the status signals and the data strobe are programmable by the user.

Eight programmable I/O signals support general-purpose hardware interface. Each programmable I/O may be configured as either an input or an output pin.

The JTAG port of the LSI402ZX is an IEEE 1149.1 compliant test access port (TAP) that provides access to all on-chip resources. The device emulation unit (DEU) works in conjunction with code residing in the boot ROM to provide full-speed in-circuit emulation, allowing full visibility and

control of the device memory and registers. Working together, the JTAG port, the device emulation unit, and the boot ROM provide the capability to download to the LSI402ZX internal and external memory.

The LSI402ZX uses an on-chip PLL to generate a high frequency processor clock from a slower, off-chip external clock source. The off-chip clock source is applied to the CLKIN pin of the LSI402ZX and must be a crystal oscillator within the frequency range of 2 to 40 MHz[1]. The CLKOUT pin reflects the processor clock frequency. The processor clock can use an off-chip clock source directly by bypassing the on-chip PLL.

Instruction Set Summary

Table 1 summarizes the ZSP instruction set used by the LSI402ZX.

Table 1 ZSP Instruction Set

Instruction	Description
ABS	Absolute Value
ABS.E	Absolute Value (Extended Precision)
ADD	Add Immediate
ADD	Add Registers
ADD.E	Add Registers (Extended Precision)
ADDC.E	Add With Carry (Extended Precision)
AGN0	Again0
AGN1	Again1
AGN2	Again2
AGN3	Again3
AND	Logical AND
(Sheet 1 of 6)	

1. The 402ZX is a fully static device. The CLKIN signal will accept input down to DC when the PLL is bypassed.

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
AND.E	Logical AND (Extended Precision)
BC	Branch on Carry
BGE	Branch on Greater than or Equal To
BGT	Branch on Greater Than
BITC	Bit Clear Control Register
BITC	Bit Clear Operand Register
BITI	Bit Invert Control Register
BITI	Bit Invert Operand Register
BITS	Bit Set Control Register
BITS	Bit Set Operand Register
BITT	Bit Test Control Register
BITT	Bit Test Operand Register
BLE	Branch On Less Than Or Equal To
BLT	Branch On Less Than
BNC	Branch On No Carry
BNOV	Branch On No Overflow
BNZ	Branch On Not Zero
BOV	Branch On Overflow
BR	Unconditional Branch
BZ	Branch On Zero
CALL	Call Label/Operand Register
CMACI.A	Complex MAC Imaginary To Accumulator A
CMACI.B	Complex MAC Imaginary To Accumulator B
CMACR.A	Complex MAC Real To Accumulator A
(Sheet 2 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
CMACR.B	Complex MAC Real To Accumulator B
CMP	Compare Immediate/Register to Register
CMP.E	Compare Immediate/Register to Register (Extended Precision)
CMULI.A	Complex Multiplication Imaginary To Accumulator A
CMULI.B	Complex Multiplication Imaginary To Accumulator B
CMULR.A	Complex Multiplication Real To Accumulator A
CMULR.B	Complex Multiplication Real To Accumulator B
DMAC.A	Double MAC To Accumulator A
DMAC.B	Double MAC To Accumulator B
DMUL.A	Multiplication (Extended Precision) To Accumulator A
DMUL.B	Multiplication (Extended Precision) To Accumulator B
IMUL.A	Integer Multiply To Accumulator A
IMUL.B	Integer Multiply To Accumulator B
LD	Load
LDDU	Load Double With Update
LDU	Load With Update
LDX	Load With Register Based Offset
LDXU	Load With Register Based Offset And Update
MAC.A	Multiply Accumulate To Accumulator A
MAC.B	Multiply Accumulate To Accumulator B
MAC2.A	Dual MAC To Accumulator A
MAC2.B	Dual MAC To Accumulator B
MACN.A	Multiply Accumulate With Negation To Accumulator A
MACN.B	Multiply Accumulate With Negation To Accumulator B
(Sheet 3 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
MAX	Maximum
MAX.E	Maximum (Extended Precision)
MIN	Minimum
MIN.E	Minimum (Extended Precision)
MOV	Move Control Register To Operand Register
MOV	Move Immediate To Operand Register
MOV	Move Operand Register To Control Register
MOV	Move Operand Register To Operand Register
MOV	Move to PC
MOVH	Move Immediate To Higher Byte Of Control Register
MOVH	Move Immediate To Higher Byte Of Operand Register
MOVL	Move Immediate To Lower Byte Of Operand Register
MOVL	Move Immediate To Lower Byte Of Control Register
MUL.A	Multiply To Accumulator A
MUL.B	Multiply To Accumulator B
MULN.A	Multiply With Negation To Accumulator A
MULN.B	Multiply With Negation To Accumulator B
NEG	Negate
NEG.E	Negate (Extended Precision)
NOP	No Operation
NORM	Normalize
NORM.E	Normalize (Extended Precision)
NOT	Logical Not
NOT.E	Logical Not (Extended Precision)
(Sheet 4 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
OR	Logical Or
OR.E	Logical Or (Extended Precision)
PADD.A	Parallel Add Registers To Accumulator A
PADD.B	Parallel Add Registers To Accumulator B
PSUB.A	Parallel Subtract Registers To Accumulator A
PSUB.B	Parallel Subtract Registers To Accumulator B
RET	Return From Subroutine
RETI	Return From Interrupt
REVB	Reverse Bit
ROUND.E	Round (Extended Precision)
SHLA	Shift Left Arithmetic Immediate
SHLA	Shift Left Arithmetic Register
SHLA.E	Shift Left Arithmetic Immediate (Extended Precision)
SHLA.E	Shift Left Arithmetic Register (Extended Precision)
SHLL	Shift Left Logical Immediate
SHLL	Shift Left Logical Register
SHLL.E	Shift Left Logical Immediate (Extended Precision)
SHLL.E	Shift Left Logical Register (Extended Precision)
SHRA	Shift Right Arithmetic Immediate
SHRA	Shift Right Arithmetic Register
SHRA.E	Shift Right Arithmetic Immediate (Extended Precision)
SHRA.E	Shift Right Arithmetic Register (Extended Precision)
SHRL	Shift Right Logical Immediate
SHRL	Shift Right Logical Register
(Sheet 5 of 6)	

Table 1 ZSP Instruction Set (Cont.)

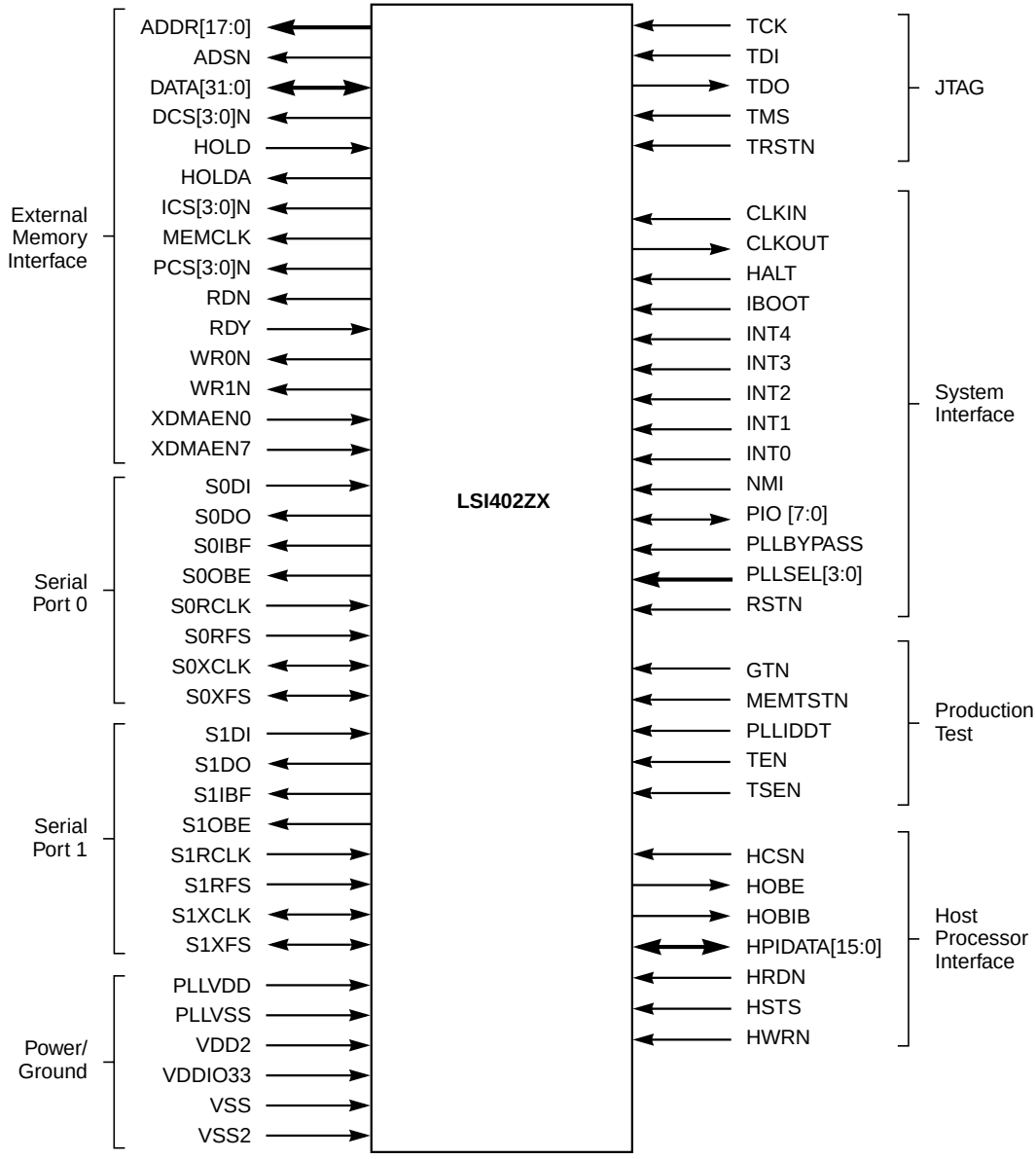
Instruction	Description
SHRL.E	Shift Right Logical Immediate (Extended Precision)
SHRL.E	Shift Right Logical Register (Extended Precision)
ST	Store
STDU	Store Double With Update
STU	Store With Update
STX	Store With Register Based Offset
STXU	Store With Register Based Offset And Update
SUB	Subtract
SUB.E	Subtract (Extended Precision)
SUBC.E	Subtract With Carry (Extended Precision)
VIT_A	Viterbi Instruction For Point A
VIT_B	Viterbi Instruction For Point B
XOR	Exclusive Or
XOR.E	Exclusive Or (Extended Precision)

(Sheet 6 of 6)

Signal Descriptions

This section describes the LSI402ZX signals, as shown in Figure 2.

Figure 2 LSI402ZX System Interfaces



The signals have been divided into the following tables:

- Table 2, “System Interface Signals,” on page 15
- Table 3, “External Memory Interface Unit Signals,” on page 16
- Table 4, “Serial Port Signals,” on page 17
- Table 5, “Host Processor Interface (HPI) Signals,” on page 17
- Table 6, “JTAG Interface Signals,” on page 18
- Table 7, “Power/Ground Signals,” on page 18
- Table 8, “Production Test Signals,” on page 18

For complete signal descriptions, refer to the *LSI402ZX Digital Signal Processor User’s Guide.*

Table 2 System Interface Signals

Signal	I/O	Description
CLKIN	Input	Master Clock Input
CLKOUT	Output	Clock Out (reflects the processor clock)
HALT	Input	Halt Processor Clock[1]
IBOOT	Input	Boot Device Select
INT4	Input	External Hardware Interrupt 4
INT3	Input	External Hardware Interrupt 3
INT2	Input	External Hardware Interrupt 2
INT1	Input	External Hardware Interrupt 1
INT0	Input	External Hardware Interrupt 0
NMI	Input	Nonmaskable Interrupt
PIO[7:0]	Bidirectional	Programmable I/O
PLLBYPASS	Input	PLL Bypass[2]
PLLSEL[3:0]	Input	PLL Multiplier Select
RSTN	Input	Device Reset (active LOW)

1. When HIGH.
2. LSI402ZX uses internal PLL when LOW, uses CLKIN signal directly (bypassing internal PLL) when HIGH.

Table 3 External Memory Interface Unit Signals

Signal	I/O	Description
ADDR[17:0]	Output	External Memory Address Bus
ADSN	Output	Address Strobe
DATA[31:0]	Bidirectional	External Memory Data Bus
DCS[3:0]N	Output	Data Memory Chip Selects
HOLD	Input	External Memory Access Hold Request
HOLDA	Output	External Memory Access Hold Acknowledge
ICS[3:0]N	Output	Instruction Memory Chip Selects
MEMCLK	Output	Memory Clock
PCS[3:0]N	Output	Memory-Mapped Peripheral Chip Selects
RDN	Output	External Memory Read Strobe
RDY	Input	Hardware Wait State
WR0N	Output	External Memory Interface Write Strobe
WR1N	Output	External Memory Interface Write Strobe
XDMAEN0[1]	Input	External DMA Channel 0 Enable
XDMAEN7[2]	Input	External DMA Channel 7 Enable

1. The TEN and XDMAEN0 signals share a package ball. PLLSEL[3:0] controls the currently active signal. When PLLSEL[3:0] is set to 0b1111, the TEN signal is active. All other settings of PLLSEL[3:0] enable the XDMAEN0 signal.
2. The TSEN and XDMAEN7 signals share a package ball. PLLSEL[3:0] controls the currently active signal. When PLLSEL[3:0] is set to 0b1111, the TSEN signal is active. All other settings of PLLSEL[3:0] enable the XDMAEN7 signal.

Table 4 Serial Port Signals

Signal[1]	I/O	Description
SxDI	Input	Data Input
SxDO	Output	Data Output
SxIBF	Output	Input Buffer Full
SxOBE	Output	Output Buffer Empty
SxRCLK	Input	Receive Clock
SxRFS	Input	Receive Frame Sync
SxXCLK	Bidirectional	Transmit Clock
SxXFS	Bidirectional	Transmit Frame Sync

1. Each serial port signal exists for both serial port 0 and serial port 1. The signal names are prepended with S0 and S1 (for example, S0DO and S1DO).

Table 5 Host Processor Interface (HPI) Signals

Signal	I/O	Description
HCSN	Input	HPI Chip Select
HOBE	Output	HPI Output Buffer Empty
HOBIB	Output	HPI Output Status
HPIDATA[15:0]	Bidirectional	HPI Data Bus
HRDN	Input	HPI Intel Mode Read Strobe/Motorola Mode Data Strobe
HSTS	Input	HPI Input Status
HWRN	Input	HPI Intel Mode Write Strobe/Motorola Mode Data Direction

Table 6 JTAG Interface Signals

Signal	I/O	Description
TCK	Input	Test Clock
TDI	Input	Test Data Input
TDO	Output	Test Data Output
TMS	Input	Test Mode Select
TRSTN	Input	Test Port Reset

Table 7 Power/Ground Signals

Signal	I/O	Description
PLLVDD	Input	PLL Power
PLLVSS	Input	PLL Ground
VDD2	Input	Core Power
VDDIO33	Input	I/O Device Power
VSS	Input	I/O Device Ground
VSS2	Input	Core Ground

Table 8 Production Test Signals

Signal	I/O	Description
GTN	Input	Global Test (Tie HIGH during Normal Operation)
MEMTSTN	Input	Reserved. Must be Tied HIGH (3.3 V)
PLLIDDT	Input	Reserved. Must be tied LOW.
TEN[1]	Input	Production Test Enable
TSEN[2]	Input	Production Test Enable

1. The TEN and XDMAEN0 signals share a package ball. PLLSEL[3:0] controls the currently active signal. When PLLSEL[3:0] is set to 0b1111, the TEN signal is active. All other settings of PLLSEL[3:0] enable the XDMAEN0 signal.
2. The TSEN and XDMAEN7 signals share a package ball. PLLSEL[3:0] controls the currently active signal. When PLLSEL[3:0] is set to 0b1111, the TSEN signal is active. All other settings of PLLSEL[3:0] enable the XDMAEN7 signal.

Functional Waveforms

This section contains functional waveforms for selected LSI402ZX operations. For complete timing information refer to the *LSI402ZX Digital Signal Processor User's Guide*.

Serial Port Timing

The two serial ports in the LSI402ZX are identical. This section contains transmit and receive timing waveforms for the serial ports. The timing for both burst/continuous mode and TDM mode is identical.

Figure 3 shows the transmit timing for the serial ports when the frame sync and data lines are coincident and the transmit frame sync and clock signals are generated externally. Table 9 shows the timing relations for the signals in Figure 3.

Figure 3 Serial Port Transmit Timing for axfs = 0b00 (XFS/XCLK as Inputs)

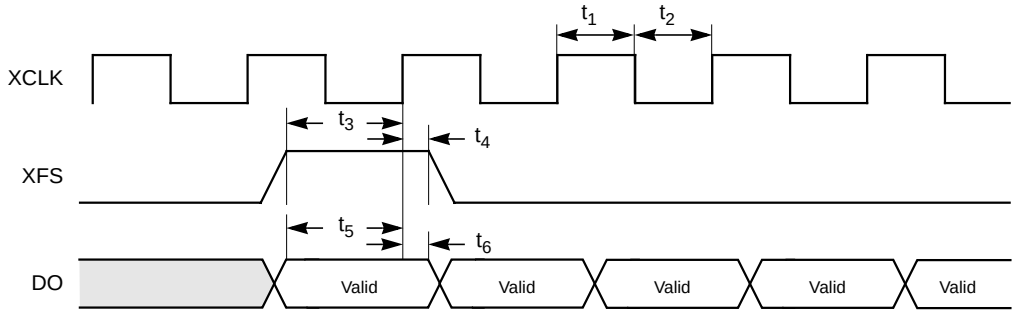


Table 9 Serial Port Transmit Timing Values (XFS/XCLK as Inputs)

Symbol	Parameter	Min	Max	Unit
t_1	Clock HIGH[1]	1	–	Processor Clock Periods
t_2	Clock LOW[1]	1	–	
t_3	XFS Setup Time	4	–	ns
t_4	XFS Hold Time	1	–	
t_5	Data Out Setup Time	4	–	
t_6	Data Out Hold Time	1	–	

1. XCLK must maintain a 50% duty cycle.

Figure 4 shows the transmit timing for the serial ports when the frame sync and data lines are coincident and the transmit frame sync and clock signals are generated by the serial port. Table 10 shows the timing relations for the signals in Figure 4.

Figure 4 Serial Port Transmit Timing for axfs = 0b00 (XFS/XCLK as Outputs)

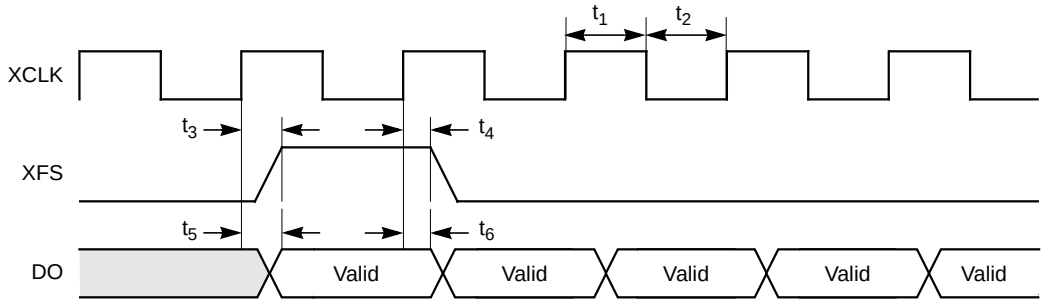


Table 10 Serial Port Transmit Timing Values (XFS/XCLK as Outputs)

Symbol	Parameter	Min	Max	Unit
t_1	Clock HIGH	1	–	Processor Clock Periods
t_2	Clock LOW	1	–	
t_3	XFS Propagation Delay	1	4	ns
t_4	XFS Propagation Delay	1	–	
t_5	Data Out Propagation Delay	1	4	
t_6	Data Out Hold Time	1	–	

Figure 5 shows the receive timing for the serial ports when the frame sync and data lines are coincident. The receive frame sync and clock signals are always generated externally. Table 11 shows the timing relations for the signals in Figure 5.

Figure 5 Serial Port Receive Timing (arfs = 0b00)

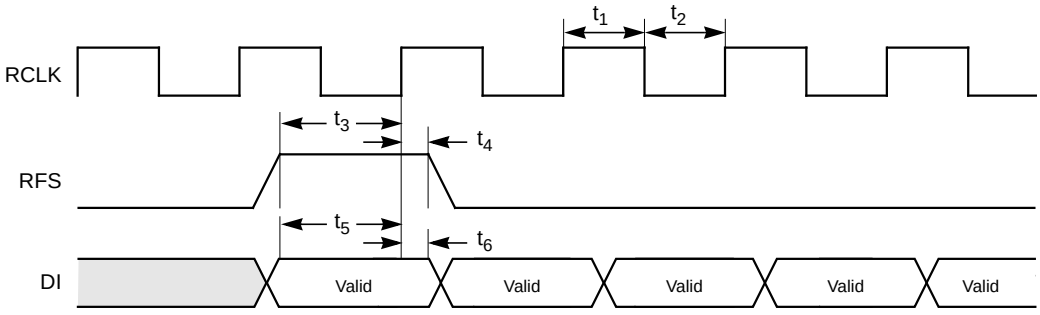


Table 11 Serial Port Receive Timing Values

Symbol	Parameter	Min	Max	Unit
t_1	Clock HIGH[1]	1	–	Processor Clock Periods
t_2	Clock LOW[1]	1	–	
t_3	RFS Setup Time	4	–	ns
t_4	RFS Hold Time	1	–	
t_5	Data In Setup Time	4	–	
t_6	Data In Hold Time	1	–	

1. RCLK must maintain a 50% duty cycle.

External Memory Interface Unit Timing

The external memory interface unit connects the LSI402ZX to external memory and peripherals.

Asynchronous Mode

For all waveforms in this section, the dwait register fields have the following values:

- csrw is set to 0x0
- rwpw is set to 0x4
- rwcs is set to 0x0

Figure 6 shows an instruction or data memory read with four wait-state cycles. Table 12 describes the timing relationships in Figure 6.

Figure 6 Asynchronous External Instruction or Data Memory Read (4-Cycle Wait State)

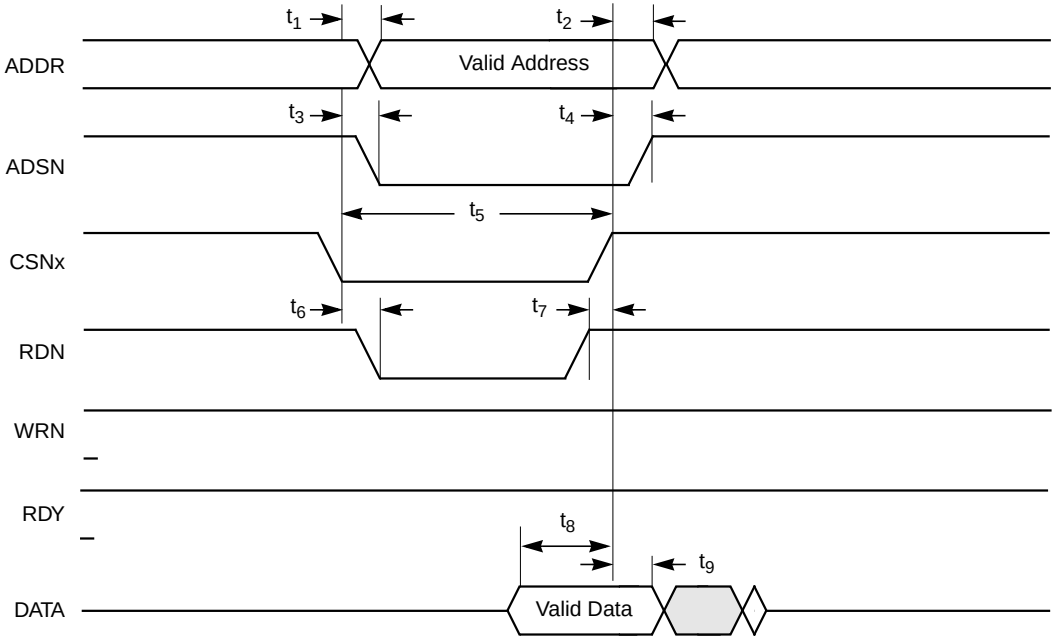


Table 12 External Instruction Or Data Read Timing (4-Cycle Wait State)

Reference	Description	Min[1]	Max[1]	Unit
t_1	CSNx LOW to ADDR Valid	–	1	ns
t_2	ADDR Hold Time (CSNx HIGH to ADDR Invalid)	2	–	ns
t_3	CSNx LOW to ADSN LOW	–	1	ns
t_4	ADSN Hold Time (CSNx HIGH to ADSN HIGH)	0	–	ns
t_5	Enable Pulse Width (CSNx LOW to CSNx HIGH)	T • (csrw + rwpw + rwcs)	–	ns
t_6	CSNx LOW to RDN LOW	–	T • csrw	ns

Table 12 External Instruction Or Data Read Timing (4-Cycle Wait State)

Reference	Description	Min[1]	Max[1]	Unit
t_7	RDN HIGH to CSNx HIGH	–	T • rwcs	ns
t_8	Data Valid to CSNx HIGH	T	–	ns
t_9	Data Hold Time	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwcs are fields in the dwait register.

Figure 7 shows an instruction or data memory write with four wait-state cycles. Table 13 describes the timing relationships in Figure 7.

Figure 7 Asynchronous External Data or Instruction Memory Write (4-Cycle Wait State)

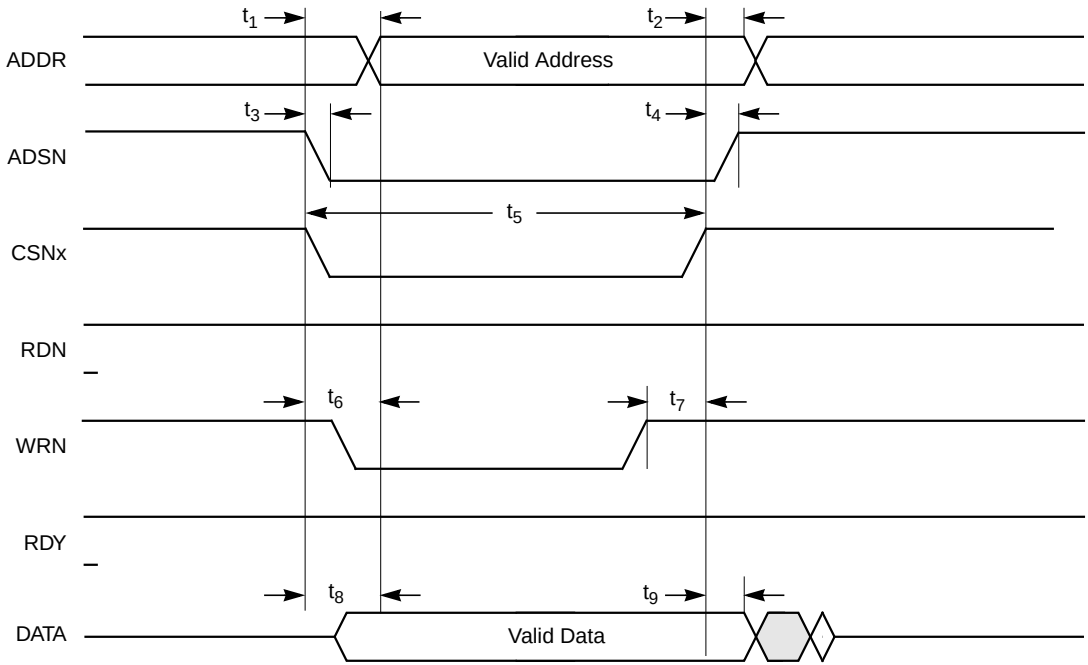


Table 13 External Instruction or Data Write Timing

Reference	Description	Min[1]	Max[1]	Units
t_1	CSNx LOW to ADDR Valid	–	1	ns
t_2	ADDR Hold Time (CSNx HIGH to ADDR Invalid)	2	–	ns
t_3	CSNx LOW to ADSN LOW	–	1	ns
t_4	ADSN Hold Time (CSNx HIGH to ADSN HIGH)	0	–	ns
t_5	CSNx LOW to CSNx HIGH[2]	T • (csrw + rwpw + rwcs)	–	ns
t_6	CSNx LOW to WRN LOW[2]	–	T • csrw	ns
t_7	WRN HIGH to CSNx HIGH[2]	–	T • rwcs	ns
t_8	CSNx LOW to Data Valid	–	1	ns
t_9	Data Hold Time (CSNx HIGH to Data Invalid)	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwcs are fields in the dwait register.
2. These values are much greater (~10 ns) than t_9 (~1 ns).

Synchronous Mode

Figure 8 shows the timing relationships for synchronous external instruction or data reads. Table 14 describes the annotations shown in Figure 8.

Figure 8 Synchronous Mode Timing (Divide by Two)

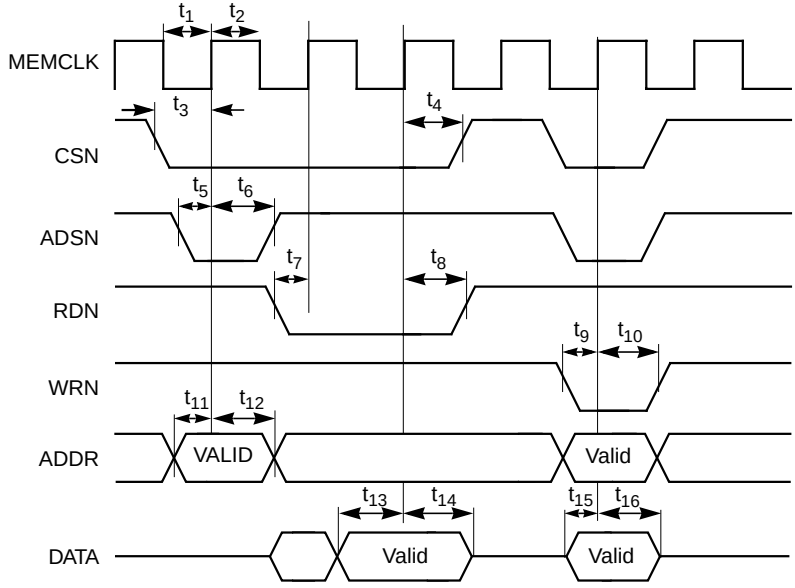


Table 14 Synchronous Memory Timing, 2:1 Mode

Symbol	Description	Min	Max	Units
t_1	Clock LOW	1	–	Cycles
t_2	Clock HIGH	1	–	Cycles
t_3	Clock LOW to CSN LOW	–	1	ns
t_4	Clock LOW to CSN HIGH	–	1	ns
t_5	Clock LOW to ADSN LOW	–	1	ns
t_6	Clock LOW to ADSN HIGH	–	1	ns
t_7	Clock LOW to RDN LOW	–	1	ns
t_8	Clock LOW to RDN HIGH	–	1	ns
t_9	Clock LOW to WRN LOW	–	1	ns
t_{10}	Clock LOW to WRN HIGH	–	1	ns
t_{11}	Clock LOW to ADDR Valid	–	1	ns
t_{12}	Clock LOW to ADDR Invalid	–	1	ns

Table 14 Synchronous Memory Timing, 2:1 Mode

Symbol	Description	Min	Max	Units
t_{13}	Read Data Setup	2	–	ns
t_{14}	Read Data Hold	1	–	ns
t_{15}	Clock LOW to Write Data Valid	–	1	ns
t_{16}	Clock LOW to Write Data Invalid	–	1	ns

Host Port Interface Timing

The host processor interface (HPI) provides an asynchronous 16-bit parallel port for interfacing with off-chip devices. The HPI operates in either Intel or Motorola mode.

Intel Mode

In Intel mode, HPI read cycles can be initiated/ended by either the HRDN read strobe signal or the HCSN chip select signal. The read cycle starts when the latter of both HCSN and HRDN go LOW. That is, to begin the read, both HCSN and HRDN must be LOW, but the last falling edge is used to determine the starting time of the read cycle. Conversely, the first rising edge of either HCSN or HRDN signals the end of the read cycle.

Figure 9 illustrates a host read initiated and completed by HCSN. Table 15 describes the timing relationships in Figure 9.

Figure 9 HPI Host Read, Intel Mode (HPICTL = 0b0000.00xx)

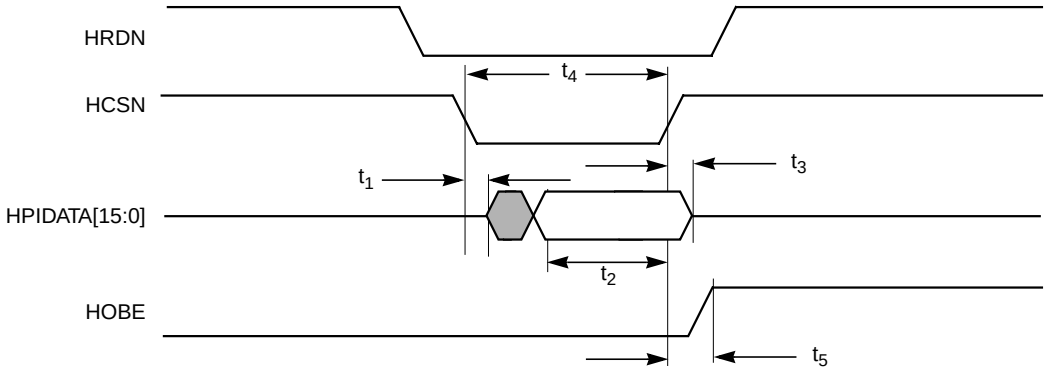


Table 15 HPI Host Read Timing, Intel Mode

Reference	Description	Min	Max	Units
t_1	Strobe (HRDN or HCSN) to Nonhigh-Z State	0.5	–	ns
t_2	Read Data Setup Time	0	–	ns
t_3	Read Data Hold Time	3T	–	ns
t_4	Strobe (HRDN or HCSN) LOW Pulse Width	T	–	ns
t_5	HOBE Delay Time	0	–	ns

In Intel mode, HPI write cycles can be initiated/ended by either the HWRN write strobe signal or the HCSN chip select signal. The write cycle starts when the latter of both HCSN and HWRN go LOW. That is, to begin the write, both HCSN and HWRN must be LOW, but the last falling edge is used to determine the starting time of the write cycle. Conversely, the first rising edge of either HCSN or HWRN signals the end of the write cycle.

Figure 10 illustrates a host write initiated and completed by HCSN. Table 16 describes the timing relationships in Figure 10.

Figure 10 HPI Host Write, Intel Mode

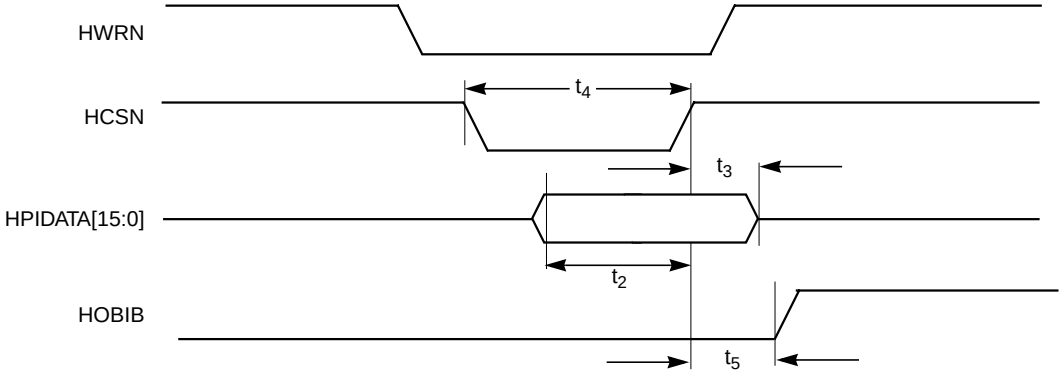


Table 16 HPI Host Write Timing, Intel Mode

Reference	Description	Min	Max	Units
t_1	Strobe (HWRN or HCSN) to Nonhigh-Z State	0.5	–	ns
t_2	Write Data Setup Time	0	–	ns
t_3	Write Data Hold Time	3T	–	ns
t_4	Strobe (HWRN or HCSN) LOW Pulse Width	T	–	ns
t_5	HOBE Delay Time	0	–	ns

Motorola Mode

In Motorola mode, the HRDN signal operates as a data strobe for both reads and writes. The HWRN signal determines the data direction. For writes, HWRN must be LOW.

Figure 11 illustrates a host read initiated and completed by HRDN. Table 17 describes the timing relationships in Figure 11.

Figure 11 HPI Host Read, Motorola Mode

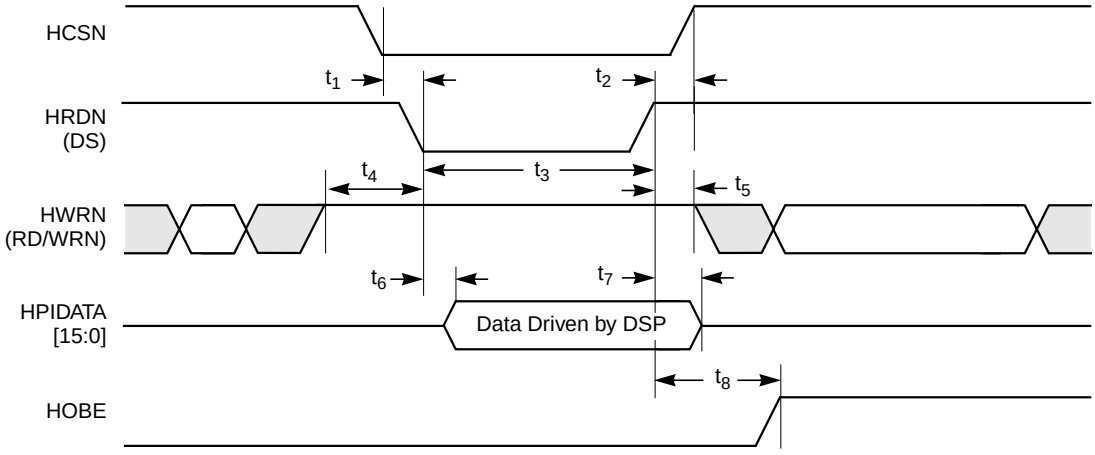


Table 17 HPI Host Read Timing, Motorola Mode

Reference	Description	Min	Max	Units
t_1	HCSN to DS Setup Time (LOW to LOW)	0.5	–	ns
t_2	DS to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t_3	DS Pulse Width (LOW to HIGH)	3T	–	ns
t_4	RD/WRN to DS Setup Time (HIGH to LOW)	T	–	ns
t_5	DS to RD/WRN Hold Time	0	–	ns
t_6	Data Delay (LOW to Valid)	–	T	ns
t_7	Data Hold (HIGH to Invalid)	0	–	ns
t_8	HOBE Delay Time (HIGH to HIGH)	–	T	ns

The HCSN and HRDN signals must both be asserted to perform a host write. The write begins when both signals have been asserted. The write ends when either HCSN or HRDN is deasserted. Figure 12 illustrates a host write initiated and completed by HRDN. Table 18 describes the timing relationships in Figure 12.

Figure 12 HPI Host Write, Motorola Mode

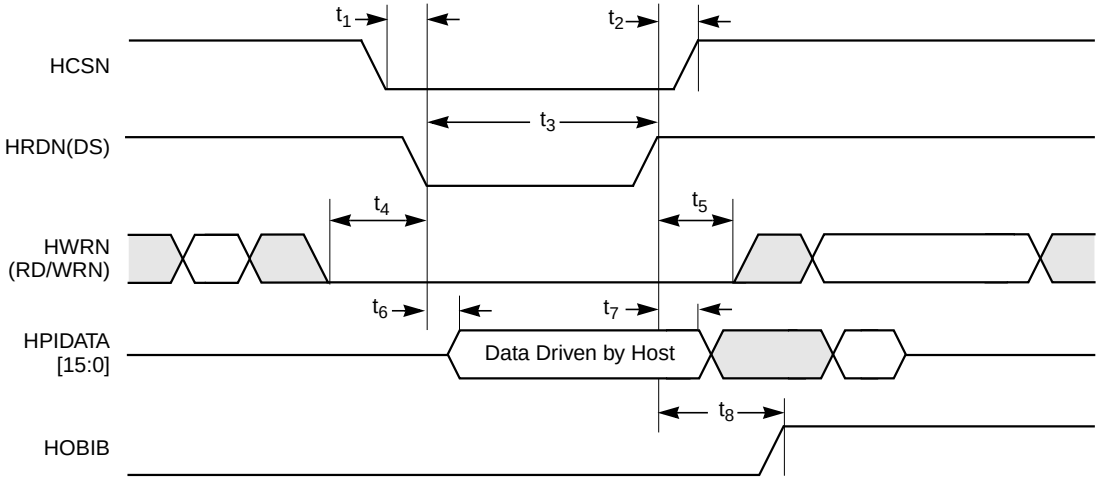


Table 18 HPI Host Write Timing, Motorola Mode

Reference	Description	Min	Max	Units
t_1	HCSN to DS Setup Time (LOW to LOW)	0.5	–	ns
t_2	DS to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t_3	DS Pulse Width (LOW to HIGH)	3T	–	ns
t_4	RD/WRN to DS Setup Time (LOW to LOW)	T	–	ns
t_5	DS to RD/WRN Hold Time	0	–	ns
t_6	Data Delay (LOW to Valid)	–	T	ns
t_7	Data Hold Time (HIGH to Invalid)	0	–	ns
t_8	HOBIB Delay Time (HIGH to HIGH)	–	T	ns

Specifications

This section describes the electrical and mechanical specifications of the LSI402ZX.

DC Characteristics

Table 19 lists the DC characteristics for the LSI402ZX.

Table 19 Electrical Characteristics

Parameter	Symbol	V_{DD} = 1.8 V, PLLVDD = 1.8 V, V_{DDIO33} = 3.3 V	
		Min	Max
Input Voltage Low High (1.8 V Supply) High (3.3 V I/O Supply)	 V_{IL} V_{IH} V_{IH}	 0 V 1.05 V 2.0 V	 0.8 V V_{DD} + 0.3 V V_{DDIO33} + 0.3 V
Input Current	I_{IN}	–10 µA	10 µA
Output Low Voltage @ +2 mA (Low)	V_{OL}	–	0.4
Output High Voltage @ –2mA (High)	V_{OH}	2.4	–
Output 3-State Current Low High	 I_{OZL} I_{OZH}	 –10 µA –	 – –10 µA
Input Capacitance	C_I	–	5.5 pF

Table 20 lists the power dissipation characteristics of the LSI402ZX. LSI Logic recommends an I/O supply current rating of 1 A or greater.

Table 20 LSI402ZX Power Dissipation

Frequency	Voltage	Power Dissipation
120 MHz	1.8 V	650 mW (maximum)
170 MHz	1.8 V	850 mW (maximum)
200 MHz	1.8 V	860 mW (typical) 1 W (maximum)

Table 21 lists the recommended operating conditions for the LSI402ZX.

Table 21 Recommended Operating Conditions

Parameter	Symbol	V_{DD} = 1.8 V, PLLVDD = 1.8 V, V_{DDIO33} = 3.3 V	
		Min	Max
Core Operating Voltage	V_{DD}	1.65	1.95
PLL Operating Voltage	PLLVDD	1.65	1.95
I/O Operating Voltage	V_{DDIO33}	3.0	3.6
Output Voltage	V_O	0	V_{DDIO33}
Junction Temperature (Commercial Operating Conditions)	T_J	0 ˚C	85 ˚C
Ambient Temperature (Commercial Operating Conditions)	T_A	0 ˚C	70 ˚C

Table 22 lists the absolute maximum ratings for the LSI402ZX. Operation beyond the limits specified in this table may cause permanent device damage.

Table 22 Absolute Maximum Ratings[1]

Property	Min	Max
DC Supply Voltage (VDD, PLLVDD)[2]	–0.3 V	2.2 V
3.3 V I/O Input Voltage (VDDIO33)	–0.3 V	3.9 V

1. Referenced to VSS
2. Internal cells operate at 1.8 V

Mechanical Specifications

The LSI402ZX is packaged in a 208-ball mini-BGA package (package code HG). Table 23 shows the thermal resistance for the package.

Table 23 Thermal Resistance (Junction-Case)

Maximum Thermal Resistance (θ_{JC}, °C/W)
4.5

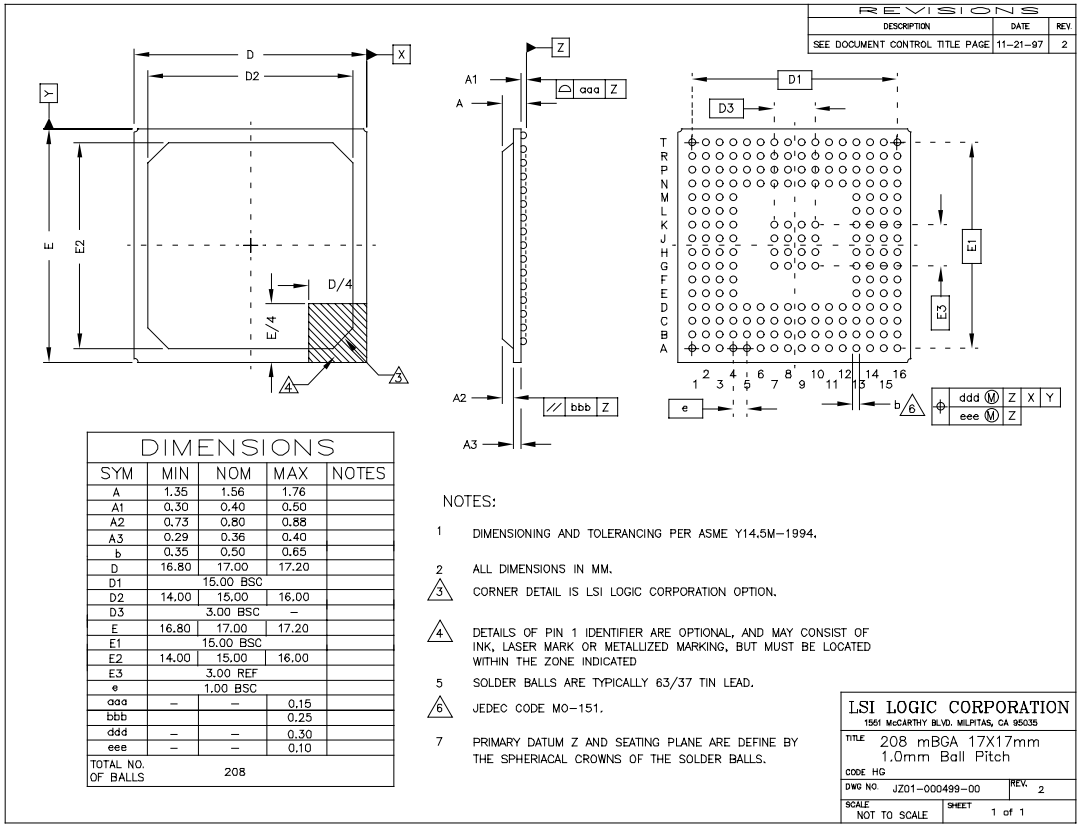
Table 24 shows the package case-to-ambient thermal resistance.

Table 24 Thermal Resistance (Case-Ambient)

Maximum Thermal Resistance (θ_{CA}, °C/W)	Airflow (LFPM)
30	0
27	200
25.5	400

Figure 13 shows a mechanical drawing of the LSI402ZX's package.

Figure 13 208 mini-BGA (HG) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code HG.**

Figure 14 shows the 208-pin BGA top view.

Figure 14 208-Pin BGA Top View

A1 RSTN	A2 XDMAEN0	A3 NMI	A4 INT1	A5 INT4	A6 VSS	A7 TRSTN	A8 HRDN	A9 VDDIO	A10 HPIDATA2	A11 HPIDATA6	A12 VDDIO	A13 HPIDATA10	A14 HPIDATA13	A15 HPIDATA15	A16 VDD2
B1 MEMTSTN	B2 VDDIO	B3 XDMAEN7	B4 INT0	B5 INT3	B6 VDD2	B7 TMS	B8 TSE	B9 VDD2	B10 HPIDATA3	B11 HPIDATA7	B12 HPIDATA8	B13 HPIDATA12	B14 HPIDATA14	B15 CLKOUT	B16 PLLVSS
C1 IBOOT	C2 HALT	C3 VDD2	C4 INT2	C5 TCK	C6 TDI	C7 HCSN	C8 HSTS	C9 VDDIO	C10 HPIDATA1	C11 HPIDATA5	C12 VDD2	C13 HPIDATA11	C14 HPIDATA11	C15 PLLVDD	C16 CLKIN
D1 PIO7	D2 HOLDA	D3 HOLD	D4 PIO6	D5 GTN	D6 TDO	D7 HWRN	D8 HOBIB	D9 HOBE	D10 HPIDATA0	D11 HPIDATA4	D12 VSS	D13 HPIDATA9	D14 PLLSEL1	D15 PLLSEL0	D16 VSS
E1 PIO4	E2 PIO5	E3 VDDIO	E4 VDD2									E13 VDD2	E14 RDY	E15 PLLSEL2	E16 PLLSEL3
F1 PIO3	F2 VSS	F3 PIO2	F4 PIO1									F13 WR0N	F14 ADSN	F15 MEMCLK	F16 VSS
G1 S1DO	G2 PIO0	G3 S1XFS	G4 S1XCLK			G7 VSS2	G8 VSS2	G9 VSS2	G10 VSS2			G13 VDD2	G14 VSS	G15 WR1N	G16 RDN
H1 S1IBF	H2 S1OBE	H3 S1RCLK	H4 S1RFS			H7 VSS2	H8 VSS2	H9 VSS2	H10 VSS2			H13 PCS2N	H14 PCS1N	H15 VDDIO	H16 PCS0N
J1 VSS	J2 S0DO	J3 VDDIO	J4 S1DI			J7 VSS2	J8 VSS2	J9 VSS2	J10 VSS2			J13 PCS3N	J14 DCS0N	J15 DCS2N	J16 DCS1N
K1 S0OBE	K2 S0IBF	K3 S0XCLK	K4 S0XFS			K7 VSS2	K8 VSS2	K9 VSS2	K10 VSS2			K13 DCS3N	K14 ICS0N	K15 ICS2N	K16 ICS1N
L1 S0DI	L2 VDDIO	L3 S0RFS	L4 S0RCLK									L13 ICS3N	L14 VSS	L15 ADDR0	L16 VDDIO
M1 DATA31	M2 DATA30	M3 VSS	M4 VDD2									M13 ADDR1	M14 ADDR2	M15 ADDR4	M16 ADDR3
N1 DATA28	N2 DATA27	N3 DATA29	N4 DATA18	N5 VSS	N6 DATA13	N7 DATA11	N8 DATA7	N9 VDDIO	N10 DATA4	N11 VDD2	N12 ADDR17	N13 VSS	N14 VDDIO	N15 ADDR5	N16 VDD2
P1 VDDIO	P2 VDD2	P3 DATA23	P4 DATA20	P5 VDD2	P6 DATA14	P7 VSS	P8 DATA8	P9 VSS	P10 DATA3	P11 VSS	P12 ADDR16	P13 VSS	P14 ADDR9	P15 ADDR7	P16 ADDR6
R1 DATA26	R2 DATA24	R3 VDDIO	R4 DATA21	R5 DATA17	R6 DATA16	R7 DATA12	R8 DATA10	R9 DATA5	R10 VDDIO	R11 DATA0	R12 VDDIO	R13 ADDR14	R14 ADDR11	R15 VDD2	R16 ADDR8
T1 DATA25	T2 DATA22	T3 VSS	T4 DATA19	T5 VDDIO	T6 DATA15	T7 VDDIO	T8 DATA9	T9 DATA6	T10 DATA2	T11 DATA1	T12 ADDR15	T13 ADDR13	T14 ADDR12	T15 ADDR10	T16 VDDIO

Table 25 lists the mapping of LSI402ZX signals to balls on the package. Refer to Figure 14 for the package ball grid.

Table 25 208 Signal to Balls on the Package List

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ADDR0	L15	DATA21	R4	ICS0N	K14	S1DI	J4	VDDIO	R3
ADDR1	M13	DATA22	T2	ICS1N	K16	S1DO	G1	VDDIO	T16
ADDR2	M14	DATA23	P3	ICS2N	K15	S1IBF	H1	VDDIO	T5
ADDR3	M16	DATA24	R2	ICS3N	L13	S1OBE	H2	VDDIO	T7
ADDR4	M15	DATA25	T1	INT0	B4	S1RCLK	H3	VSS	A6
ADDR5	N15	DATA26	R1	INT1	A4	S1RFS	H4	VSS	D12
ADDR6	P16	DATA27	N2	INT2	C4	S1XCLK	G4	VSS	D16
ADDR7	P15	DATA28	N1	INT3	B5	S1XFS	G3	VSS	F16
ADDR8	R16	DATA29	N3	INT4	A5	TCK	C5	VSS	F2
ADDR9	P14	DATA30	M2	MEMCLK	F15	TDI	C6	VSS	G14
ADDR10	T15	DATA31	M1	MEMTSTN	B1	TDO	D6	VSS	J1
ADDR11	R14	DCS0N	J14	NMI	A3	TMS	B7	VSS	L14
ADDR12	T14	DCS1N	J16	PCS0N	H16	TRSTN	A7	VSS	M3
ADDR13	T13	DCS2N	J15	PCS1N	H14	TSE	B8	VSS	N13
ADDR14	R13	DCS3N	K13	PCS2N	H13	VDD2	A16	VSS	N5
ADDR15	T12	GTN	D5	PCS3N	J13	VDD2	B6	VSS	P11
ADDR16	P12	HALT	C2	PIO0	G2	VDD2	B9	VSS	P13
ADDR17	N12	HCSN	C7	PIO1	F4	VDD2	C12	VSS	P7
ADSN	F14	HOBE	D9	PIO2	F3	VDD2	C3	VSS	P9
CLKIN	C16	HOBIB	D8	PIO3	F1	VDD2	E13	VSS	T3
CLKOUT	B15	HOLD	D3	PIO4	E1	VDD2	E4	VSS2	G10
DATA0	R11	HOLDA	D2	PIO5	E2	VDD2	G13	VSS2	G7
DATA1	T11	HPIDATA0	D10	PIO6	D4	VDD2	M4	VSS2	G8
DATA2	T10	HPIDATA1	C10	PIO7	D1	VDD2	N11	VSS2	G9
DATA3	P10	HPIDATA2	A10	PLLBYPASS	C14	VDD2	N16	VSS2	H10
DATA4	N10	HPIDATA3	B10	PLLSEL0	D15	VDD2	P2	VSS2	H7
DATA5	R9	HPIDATA4	D11	PLLSEL1	D14	VDD2	P5	VSS2	H8
DATA6	T9	HPIDATA5	C11	PLLSEL2	E15	VDD2	R15	VSS2	H9
DATA7	N8	HPIDATA6	A11	PLLSEL3	E16	VDDIO	A12	VSS2	J10
DATA8	P8	HPIDATA7	B11	PLLVDD	C15	VDDIO	A9	VSS2	J7
DATA9	T8	HPIDATA8	B12	PLLVSS	B16	VDDIO	B2	VSS2	J8
DATA10	R8	HPIDATA9	D13	RDN	G16	VDDIO	C9	VSS2	J9
DATA11	N7	HPIDATA10	A13	RDY	E14	VDDIO	E3	VSS2	K10
DATA12	R7	HPIDATA11	C13	RSTN	A1	VDDIO	H15	VSS2	K7
DATA13	N6	HPIDATA12	B13	S0DI	L1	VDDIO	J3	VSS2	K8
DATA14	P6	HPIDATA13	A14	S0DO	J2	VDDIO	L16	VSS2	K9
DATA15	T6	HPIDATA14	B14	S0IBF	K2	VDDIO	L2	WR0N	F13
DATA16	R6	HPIDATA15	A15	S0OBE	K1	VDDIO	N14	WR1N	G15
DATA17	R5	HRDN	A8	S0RCLK	L4	VDDIO	N9	XDMAEN0	A2
DATA18	N4	HSTS	C8	S0RFS	L3	VDDIO	P1	XDMAEN7	B3
DATA19	T4	HWRN	D7	S0XCLK	K3	VDDIO	R10		
DATA20	P4	IBOOT	C1	S0XFS	K4	VDDIO	R12		

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