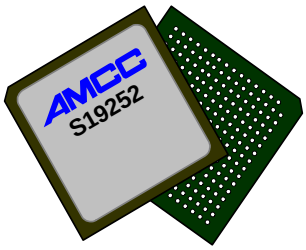


S19252

STS-192 SONET/SDH/FEC/GbE/FC 16-bit EDC Transceiver with 10 G Clock

Features

- Operational from 9.9 Gbps to 11.3 Gbps
- Built-In Self Test (BIST) with Error Counter
- On-chip High-Frequency PLLs for Clock Recovery and Clock Gen.
- 16-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indicators
- Reference Loop Timing Modes
- Line and Diagnostic Loopback Mode for Faulty Node Identification
- -40°C to 85°C Industrial Temperature Range
- Supports MDIO, I2C and SPI serial interface
- Complies with applicable OIF SFI-4 Phase 1, Telcordia/ITU-T, 300-pin MSA, IEEE 802.3ae and XFP MSA Standards
- 2000 V ESD rating on low speed pins, 1000 V on high speed I/Os
- 15 mm x 15 mm^2, 0.8 mm pitch package with Green / RoHS compliant lead free option.
- 1.2 W typical
- JTAG support

Transmitter Features

- Ref. Freq. of 155.52 or 622.08 MHz (or eq. FEC rate); Common 10 GbE/10 G FC Ref. of 156.25 MHz or 159.375 MHz for 10 G FC; Divide by 16 or 64 of the TX rates
- Internal, Self-Initializing FIFO to Decouple Transmit Clocks
- Programmable TSD Output Differential Swing
- 10 G Transmitter Serial Clock Output
- Duo Binary Encoding

Receiver Features

- LOS/RSSI
- ISI compensation. Tolerates additional 350 ps/nm of chromatic dispersion with an OSNR penalty of 1.0dB over a traditional demux
- Tolerates up to 36" of Standard FR-4 Material
- Adaptive Post-Amplifier Offset Adjust
- Phase Adjust of -0.11 to +0.085 UI
- Ref. Freq. of 155.52 MHz or 622.08 MHz (or eq. FEC rate); Common ref. of 156.25 MHz for 10 GbE/10 GFC or 159.375 MHz for 10 GFC; Divide by 16 or 64 of the RX rates
- Capability to Interface with Single-Ended or Differential TIAs (Center Tap Option)
- Input Sensitivity of 10 mV p-p (one wire or two wire) at 10^{-12} BER

Applications

- SONET/SDH and 10GbE-Based Transmission Systems & Modules
- Section Repeaters
- Add Drop Multiplexers (ADM)
- Broad-Band Cross-Connects
- Fiber Optic Test Equipment

Description

The S19252 MUX/DeMux chip is a fully integrated serialization/de-serialization SONET STS-192/10 GB Ethernet/Fiber Channel transceiver with Electronic Dispersion Compensation (EDC). This device can be used to compensate channel impairments caused by Single Mode Fiber (SMF) and copper medium. The chip performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH, 10 Gigabit Ethernet (10 GbE) and 10 Gigabit Fibre Channel (10 G FC) transmission standards. The figure below shows a typical network application. The other application block diagrams are shown on page 2.

On-chip clock synthesis PLL components are contained in the S19252 chip, allowing the use of a slower external transmit clock reference. The chip can be used with 155.52 MHz or 622.08 MHz (or equivalent FEC/10 GbE/10 G FC rates) reference clocks, in support of existing system clocking schemes. The low-jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

Overview

The S19252 transceiver incorporates SONET/SDH/10 GbE/10 G Fibre Channel serialization and deserialization functions. This chip can be used to implement the front end of SONET/10 GbE/10 G Fibre Channel equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial, and serial-to-parallel conversion and system timing.

AMCC Suggested Interface Devices

GANGES (S19202)	STS-192 POS/ATM SONET/SDH Mapper
Rubicon/Niagara	OC-192/48/12/3 DW/FEC/PM and ASYNC Mapper Device
HUDSON (S19203)	Variable Rate Digital Wrapper Framer/Deframer, Performance Monitor, and FEC Device
MEKONG (S19204)	STS-192 Pointer Processor
KHATANGA (S19205)	STS-192c SONET/SDH Framer/Mapper with Integrated MAC
S19233	Dual CDR imbedded in XFP module

The sequence of operations is as follows:

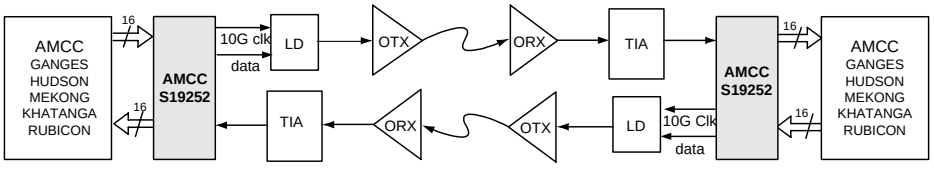
Transmitter Operations

- 16-bit parallel input
- Parallel-to-serial conversion
- Serial data output
- Serial clock output

Receiver Operations

- Serial input to post-Amplifier
- ISI compensation
- LOS and RSSI
- Threshold and phase adjustment for improved BER
- Clock and data recovery
- Serial-to-parallel conversion
- 16-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.



System Block Diagram with the S19252

S19252

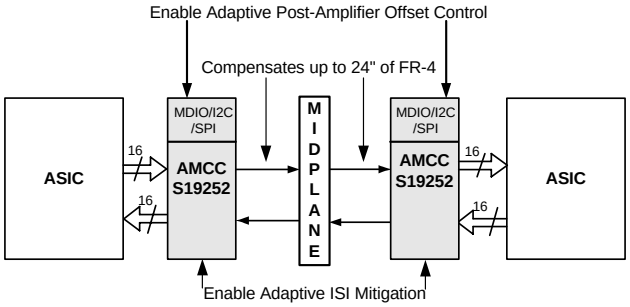


Figure 1. Mid-Plane Application Block Diagram

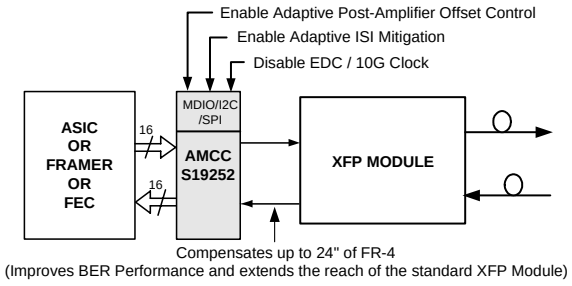


Figure 2. XFP Application Block Diagram

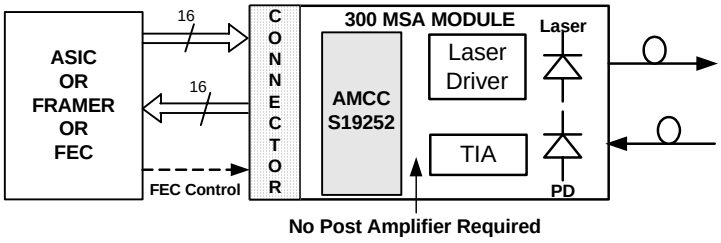


Figure 3. 300 MSA Application Block Diagram

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