FAN53418

Synchronous DC-DC MOSFET Driver

Features

- Drives N-channel High-Side and Low-Side MOSFETs in a synchronous buck configuration
- Internal Adaptive "Shoot-Through" Protection
- High Switching Frequency (> 500kHz)
  - 30ns Output Rise/Fall Times w/3000pF load
  - 20ns Propagation Delay
- 12V High-Side and 12V Low-Side Drive
- $\overline{OD}$ input for Output Disable – allows for synchronization with PWM controller
- SOIC-8 Package

Applications

- Multi-phase VRM/VRD regulators for Microprocessor Power
- High Current/High Frequency DC/DC Converters
- High Power Modular Power Supplies

General Description

The FAN53418 is a high frequency, dual MOSFET driver specifically designed to drive two power N-Channel MOSFETs in a synchronous rectified buck converter. These drivers combined with a FAN53168 Multi-Phase Buck PWM controller and power MOSFETs form a complete core voltage regulator solution for advanced microprocessors.

The FAN53418 drives both the upper and lower gates in a synchronous rectifier to +12V. The upper gate drive implements bootstrapping with only an external capacitor and diode required. This reduces implementation complexity and allows the use of higher performance, cost effective, N-Channel MOSFETs.

The output drivers in the FAN53418 have the capacity to efficiently switch power MOSFETs at frequencies over 500kHz. Each driver is capable of driving a 3000pF load with a ~20ns propagation delay and ~30ns transition time. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously. Additionally an Output Disable function is included to synchronize the driver with the PWM controller. The FAN53418 is rated for operation from 0°C to +85°C and is available in a low-cost SOIC-8 package.

Basic Application

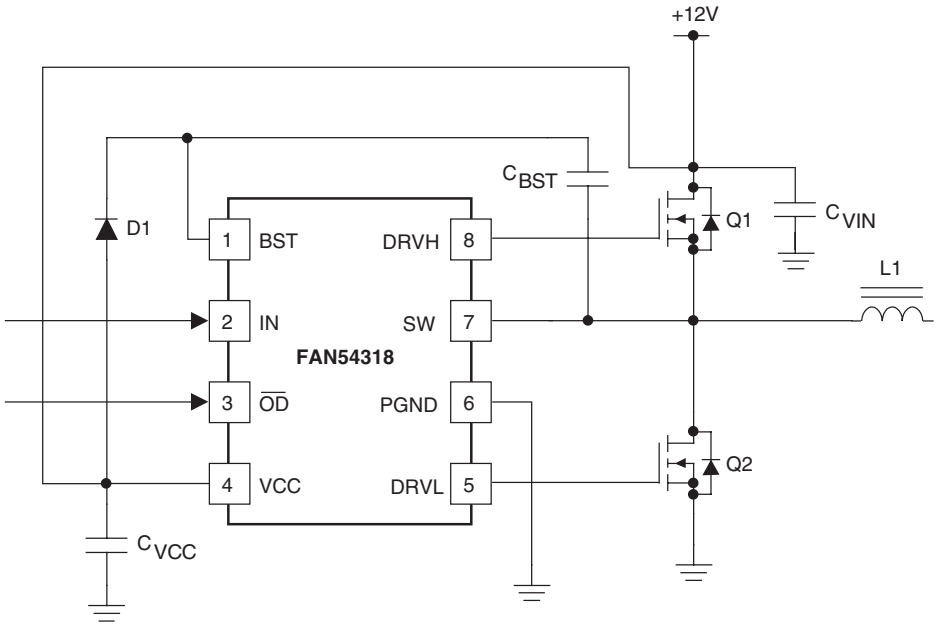
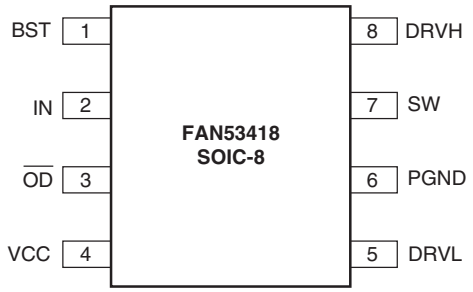


Figure 1. Basic Application Circuit

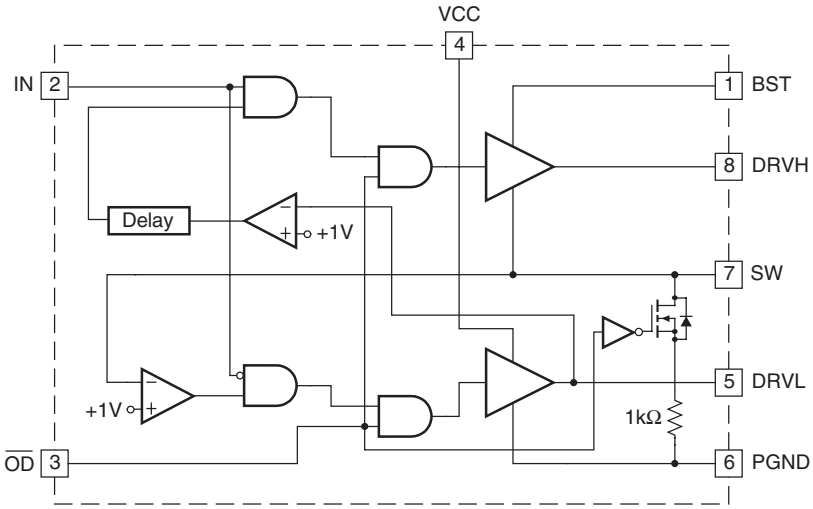
Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function Description
1	BST	**Bootstrap Supply Input**. Provides voltage supply to high-side MOSFET driver. Connect to bootstrap capacitor (typically 100nF to 1µF). See Applications Section for detailed information.
2	IN	**PWM Signal Input**. This pin accepts a digital logic-level PWM switching signal from the controller.
3	$\overline{OD}$	**Output Disable**. When low, this pin disables PWM switching and pulls DRVH and DRVL low.
4	VCC	**Power Input**. +12V chip bias power. Bypass with a 1µF ceramic capacitor.
5	DRVL	**Low Side Gate Drive Output**. Connect to the gate of low-side power MOSFET(s).
6	PGND	**Power Ground**. Power ground connect close to low-side MOSFET to minimize ground loops.
7	SW	**Switch Node Input**. Connect to switching node between HS and LS MOSFETs. It is necessary for adaptive shoot-thru protection. Also it provides return for high-side bootstrapped driver.
8	DRVH	**High Side Gate Drive Output**. Connect to the gate of high-side power MOSFET(s).

Internal Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Max.	Units
Supply Voltage: V_{CC} to PGND	-0.3	+15	V
SW to PGND	-5	+15	V
BST to SW Voltage: $V_{BST} – V_{SW}$	-0.3	+15	V
BST Voltage: V_{BST} – PGND	-0.3	V_{CC} + 15	V
DRVH	V_{SW} – 0.3	V_{BST} + 0.3	V
DRVL (<200ns duration)	-2	V_{CC} + 0.3	V
Voltage on any other pin	-0.3	V_{CC} + 0.3	V

Thermal Information

Parameter	Min.	Typ.	Max.	Units
Operating Junction Temperature (T_J)	0		+150	°C
Storage Temperature	–65		+150	°C
Lead Soldering Temperature, 10 seconds			+300	°C
Vapor Phase, 60 seconds			+215	°C
Infrared, 15 seconds			+220	°C
Power Dissipation (P_D) @ T_A = 25°C			1052	mW
Thermal Resistance (Θ_{JA})*		95		°C/W

Recommended Operating Conditions See Figure 1

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage V_{CC}	V_{CC} to GND	10.8	12	13.2	V
Ambient Operating Temperature		0		+85	°C
Operating Junction Temperature (T_J)		0		+150	°C

Note:

1. Θ_{JA} is defined as 2 oz., 4 layer copper PCB with 1 in^2 thermal pad.

Electrical Specifications

(Vcc = 12V, and T_A = 0°C to +85°C, V_{BST} = 4V to 26V, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Input Supply							
Supply Voltage Range	V_{CC}		•	4.15		13.2	V
Supply Current	I_{SYS}	BST = 12V, IN = 0V	•		3	6	mA
$\overline{OD}$ Input							
Input High Voltage	$V_{IH(OD)}$		•	2.8			V
Input Low Voltage	$V_{IL(OD)}$		•			0.8	V
Input Current	$I_{IL(OD)}$		•	-1		+1	µA
Propagation Delay Time[2]	$t_{pdl(OD)}$ $t_{pdh(OD)}$	See Figure 2 See Figure 2	• •		15 20	30 40	ns ns
PWM Input							
Input High Voltage	$V_{IH(PWM)}$		•	3.5			V
Input Low Voltage	$V_{IL(PWM)}$		•			0.8	V
Input Current	$I_{IL(PWM)}$		•	-1		+1	µA
High-Side Driver							
Output Resistance, Sourcing Current		$V_{BST} – V_{SW}$ = 12V	•		1.8	3.0	Ω
Output Resistance, Sinking Current		$V_{BST} – V_{SW}$ = 12V	•		1.0	2.5	Ω
Transition Times[2]	t_{rDRVH} t_{fDRVH}	See Figure 3, $V_{BST} – V_{SW}$ = 12V, C_{LOAD}=3nF See Figure 3, $V_{BST} – V_{SW}$ = 12V, C_{LOAD}=3nF	• •		35 20	45 30	ns ns
Propagation Delay[2,3]	$t_{pdhDRVH}$ $t_{pdlDRVH}$	See Figure 3, $V_{BST} – V_{SW}$ = 12V See Figure 3, $V_{BST} – V_{SW}$ = 12V	• •		40 20	65 35	ns ns
Low-Side Driver							
Output Resistance, Sourcing Current			•		1.8	3.0	Ω
Output Resistance, Sinking Current			•		1.0	2.5	Ω
Transition Times[2]	t_{rDRVL} t_{fDRVL}	See Figure 3, C_{LOAD} = 3nF See Figure 3, C_{LOAD} = 3nF	• •		25 21	35 30	ns ns
Propagation Delay[2,3]	$t_{pdhDRVL}$ $t_{pdlDRVL}$	See Figure 3 See Figure 3	•		30 10	60 20	ns ns

Notes:

1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control.
2. AC Specifications guaranteed by design/characterization – NOT tested in production.
3. For propagation delays "t_{pdh}" refers to low-to-high signal transition and "t_{pdl}" refers to high-to-low signal transition.

Timing Characteristics

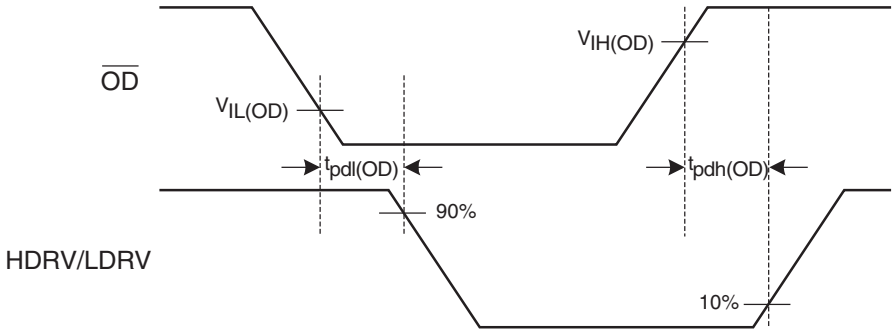


Figure 2. Output Disable Timing

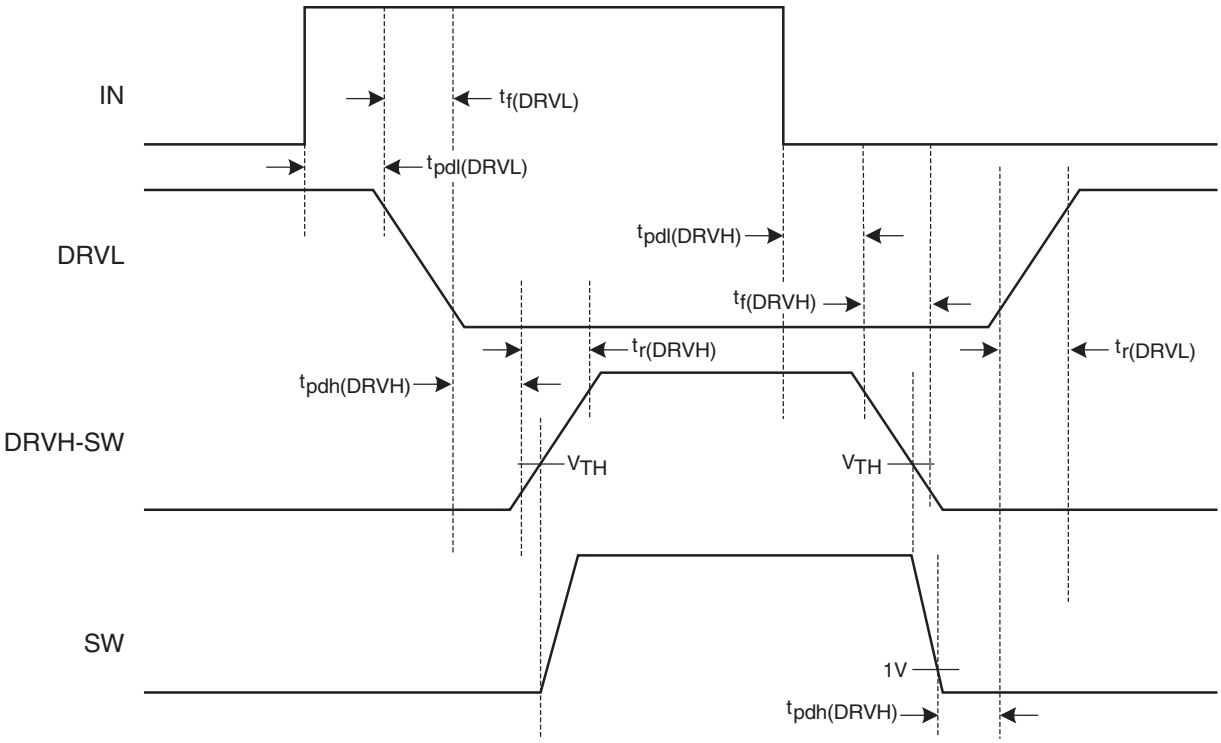
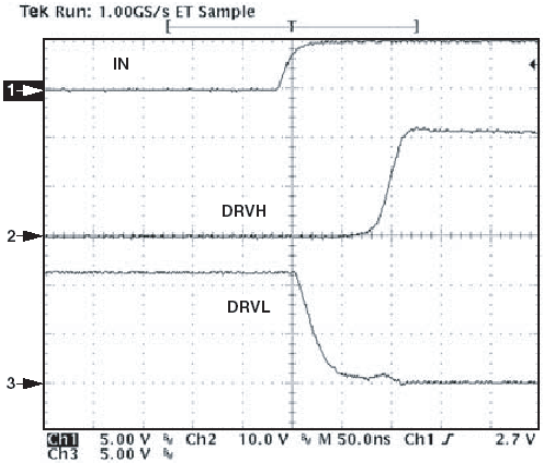
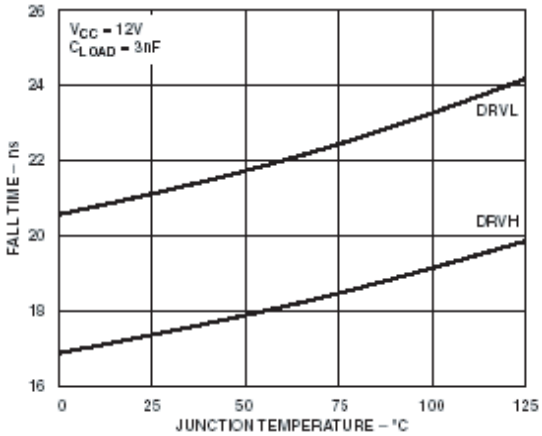


Figure 3. Non-overlap Timing Diagram (Timing is referenced to the 90% and 10% points unless otherwise noted)

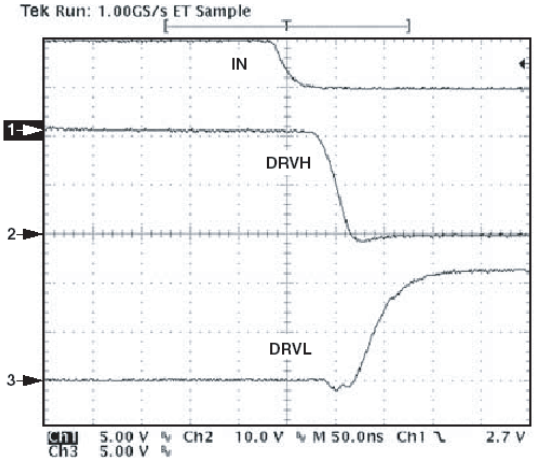
Typical Characteristics



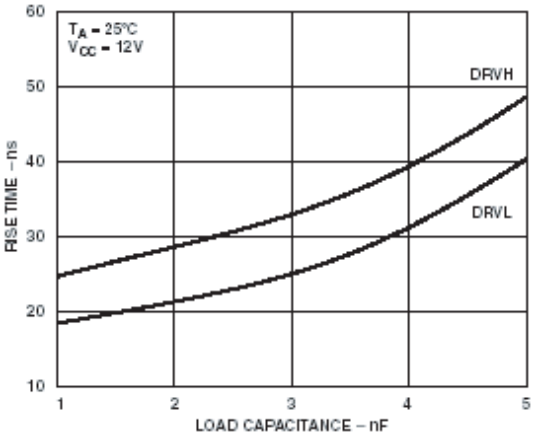
DRVH Rise and DRVL Fall Times



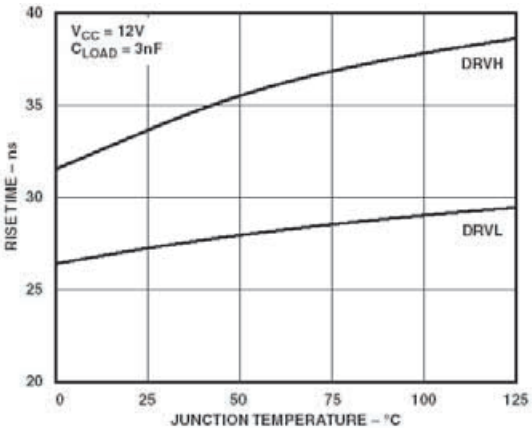
DRVH and DRVL Fall Times vs. Temperature



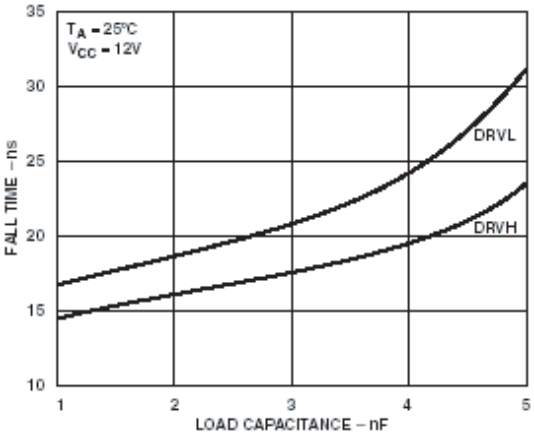
DRVH Fall and DRVL Rise Times



DRVH and DRVL Rise Times vs. Load Capacitance

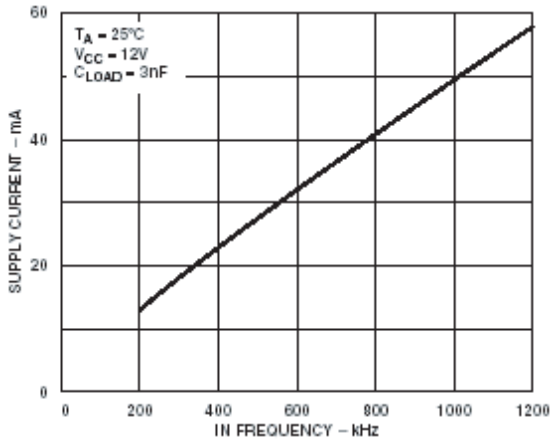


DRVH and DRVL Rise Times vs. Temperature

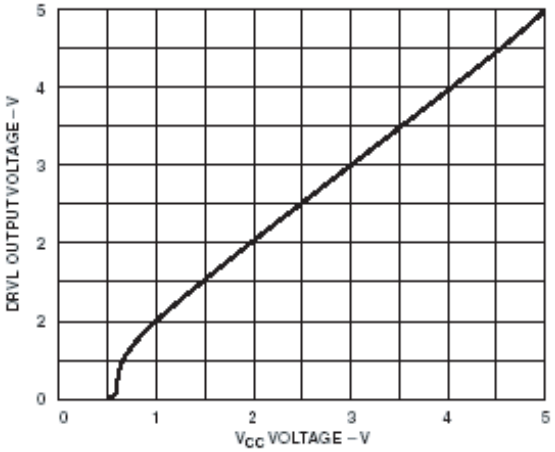


DRVH and DRVL Fall Times vs. Load Capacitance

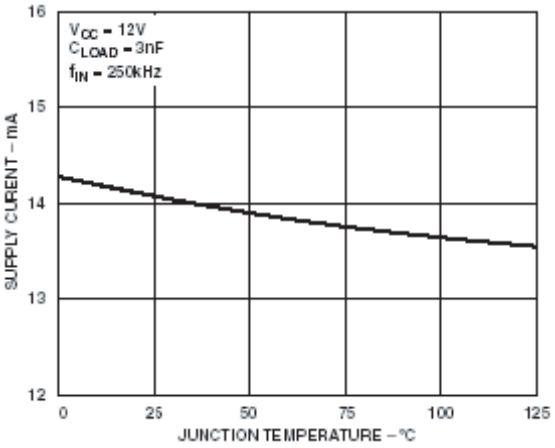
Typical Characteristics (Continued)



Supply Curreny vs. Frequency



DRVL Output Voltage vs. Supply Voltage



Supply Current vs. Temperature

Theory of Operation

The FAN53418 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3nF load at frequencies over 500kHz.

A more detailed description of the FAN53418 and its features follows. Refer to the Internal Block Diagram.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(on)}$ N-channel MOSFETs. The bias to the low-side driver is internally connected to the VCC supply and PGND. When the driver is enabled, the driver's output is 180 degrees out of phase with the PWM input. When the FAN53418 is disabled, the low-side gate is held low.

High-Side Driver

The high-side driver is designed to drive a floating low $R_{DS(on)}$ N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the BST and SW pins.

The bootstrap circuit comprises a diode, D1, and bootstrap capacitor, C_{BST}. When the FAN53418 is starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to VCC through D1. When the PWM input goes high, the high-side driver will begin to turn the high-side MOSFET, Q1, on by pulling charge out of C_{BST}. As Q1 turns on, the SW pin will rise up to V_{IN}, forcing the BST pin to $V_{IN} + V_{C(BST)}$, which is enough gate to source voltage to hold Q1 on. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET, Q2, turns on, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to V_{CC} again.

The high-side driver's output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Overlap Protection Circuit

The overlap protection circuit prevents both of the main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on-off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from Q1's turn off to Q2's turn on, and by internally setting the delay from Q2's turn off to Q1's turn on.

To prevent the overlap of the gate drives during Q1's turn off and Q2's turn on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 will begin to turn off (after a propagation delay), but before Q2 can turn on the overlap protection circuit waits for the voltage at the SW pin to fall from V_{IN} to 1V. Once the voltage on the SW pin has fallen to 1V, Q2 will begin turn on. By waiting for the voltage on the SW pin to reach 1V, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, gate charge, and drive current.

To prevent the overlap of the gate drives during Q2's turn off and Q1's turn on, the overlap circuit provides a internal delay that is set to 50ns. When the PWM input signal goes high, Q2 will begin to turn off (after a propagation delay), but before Q1 can turn on the overlap protection circuit waits for the voltage at DRVL to drop to around 10% of V_{CC}. Once the voltage at DRVL has reached the 10% point, the overlap protection circuit will wait for a 20 ns typical propagation delay. Once the delay period has expired, Q1 will begin turn on.

Application Information

Supply Capacitor Selection

For the supply input (V_{CC}) of the FAN53418, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 4.7µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the FAN53418.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a diode, as shown in Figure 1. Selection of these components can be done after the high-side MOSFET has been chosen.

The bootstrap capacitor must have a voltage rating that is able to handle twice the maximum supply voltage. A minimum 50V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}} \quad (1)$$

where Q_{GATE} is the total gate charge of the high-side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive. For example, an FDD6696 has a total gate charge of about 17nC. For an allowed droop of 200mV, the minimum required bootstrap capacitance is 85nF. A good quality 100nF X7R ceramic capacitor should be used.

A small–signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15V rating to withstand the maximum supply voltage. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \quad (2)$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in-circuit, since this is dependent on the source impedance of the 12V supply and the ESR of C_{BST}.

PC Board Layout Considerations

Use the following general guidelines when designing printed circuit boards:

1. Trace out the high-current paths and use short, wide (>20 mil) traces to make these connections.
2. Connect the PGND pin of the FAN53418 as close as possible to the source of the lower MOSFET.
3. The V_{CC} bypass capacitor should be located as close as possible to VCC and PGND pins.
4. Use vias to other layers when possible to maximize thermal conduction away from the IC.

Figure 4 gives an example of typical land patterns based on the guidelines given above. For a complete CPU voltage regulator subsystem, please refer to the FAN53168 data sheet.

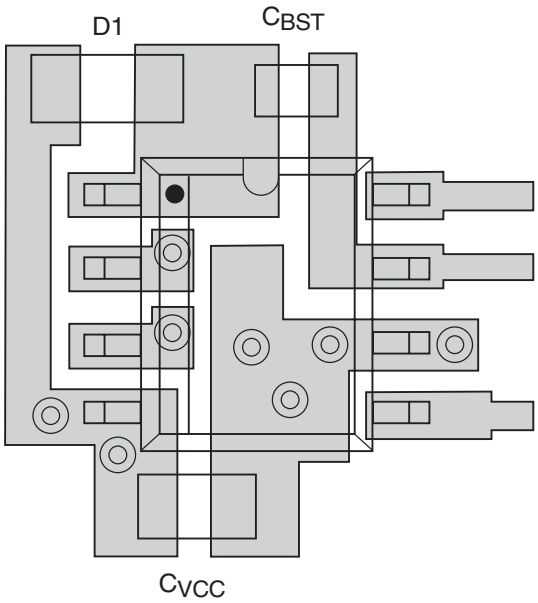
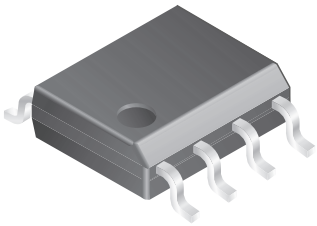


Figure 4. External Component Placement Examples for the FAN53418

Mechanical Dimensions

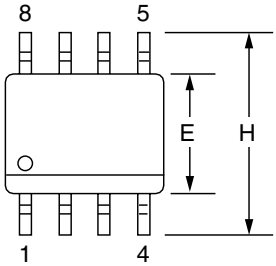
8-Lead Small Outline IC (SOIC) 0.150" Body Width

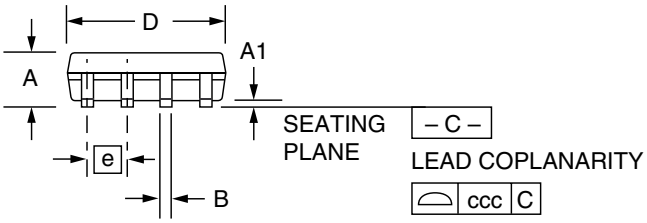


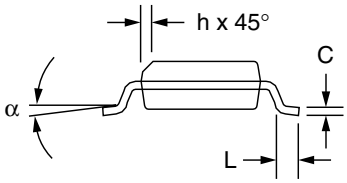
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Temperature Range	Package
FAN53418M	0°C to +85°C	SOIC-8

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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