M2005-02
Frequency Translator

DESCRIPTION

The M2005-02 integrates a high performance Phase Locked Loop (PLL) with a Voltage Controlled SAW Oscillator (VCSO) to provide a low jitter Frequency Synthesizer in a 9mm x 9mm surface mount package.

The internal high "Q" SAW filter provides low jitter signal performance and determines the maximum output frequency of the VCSO. A programmable output divider can divide the VCSO frequency by a factor of 4 to achieve an output as low as 77.76MHz with a 311.04MHz VCSO.

The input to the Frequency Synthesizer is provided by selecting between one of two input reference clocks. The maximum input frequency is 250 MHz.

Serial control of the input divider, the feedback divider, and output divider is provided via the configuration logic.

An external loop filter sets the PLL bandwidth which can be optimized to provide jitter attenuation of the input reference clock.

A HOLD feature freezes the VCSO frequency so that a stable output clock can be maintained when both input reference clocks are lost.

The bandwidth control, low phase noise, and HOLD features make the M2005-02 ideal for use as a clock jitter attenuator, frequency translator, and clock frequency generator in OC-3 through OC-192 applications.

FEATURES

- **Output Clock Frequency up to 700MHz**
- **Differential LVPECL Outputs**
- **Internal Low-jitter SAW-based Oscillator**
- **Intrinsic Jitter <1ps rms (12kHz - 20MHz)**
- **Jitter Attenuation of Input Reference Clock**
- **Dual Input MUX**
- **Configurable Loop and Output Dividers**
- **Tunable Loop Filter Response**
- **Single 3.3V Supply**
- **Small 9mm x 9mm SMT Package**
- **HOLD Mode During Loss of Input Reference Clock**

APPLICATIONS

- **SONET / SDH / 10GbE System Synchronization**
- **Add / Drop Muxes, Access and Edge Switches**
- **Line Card System Clock Cleaner / Translator**
- **Optical Module Clock Cleaner / Translator**

ABSOLUTE MAX RATINGS

Inputs, V_I: .... -0.5 to V_{CC}+0.5V

Output, V_O: .... -0.5 to V_{CC}+0.5V

Supply Voltage, V_{CC}: .... 4.6 V

Storage Temperature, T_{STO}: .... -45°C to +100°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics *or* AC Characteristics *is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.*

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FUNCTIONAL BLOCK DIAGRAM

The internal PLL will adjust the VCSO output frequency to be M (feedback divider) divided by P (input divider) times the selected input reference clock frequency. Note that the ratio of M/P times input frequency must be such that it falls within the "lock" range of the VCSO. The M divider (17-bits) can be programmed for a maximum value of 131,071 and a minimum value of 4. The P divider (9-bits) can be set to a maximum value of 511 and a minimum value of 1. The N output divider can be programmed to divide the VCSO output frequency by 1, or 4 and provide a 50% output duty cycle.

The M2005-02 is serially programmed via a 3 wire interface. Figure 1 shows the timing diagram for serial programming.

The relationship between the VCSO frequency, the M & P dividers, and the input REF_CLK is defined as follows:

$$F\ VCSO = F\ REF\_CLK \times \frac{M}{P}$$

When the N output divider is included, the complete relationship for the output frequency is defined as:

$$FOUT = \frac{F\ VCSO}{N} = F\ REF\_CLK \times \frac{M}{N \times P}$$

The N1 input can be hard wired to set the N divider to a specific state that will automatically occur during power-up.

Serial operation occurs when S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divider and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK.

When the HOLD input is asserted the M2005-02 will revert back to the initial accuracy of the VCSO and remain at that frequency until the HOLD signal is returned LOW.


FIGURE 1

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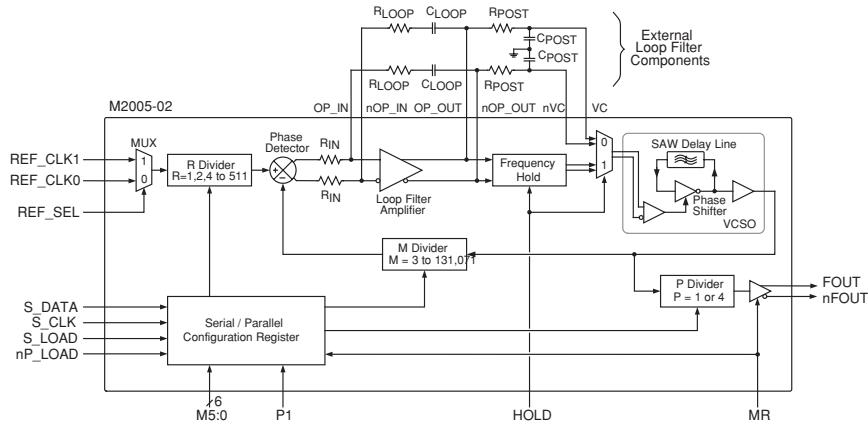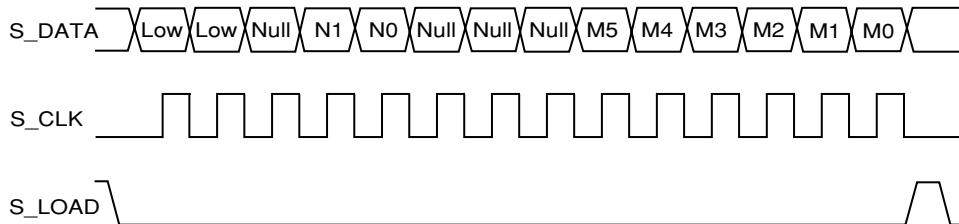
FUNCTIONAL DESCRIPTION

LOOP FILTER

The M2005-02 requires the use of an external loop filter via the provided filter pins. Due to the differential design, the implementation requires two identical RC filters as shown in Figure 2.

FIGURE 2
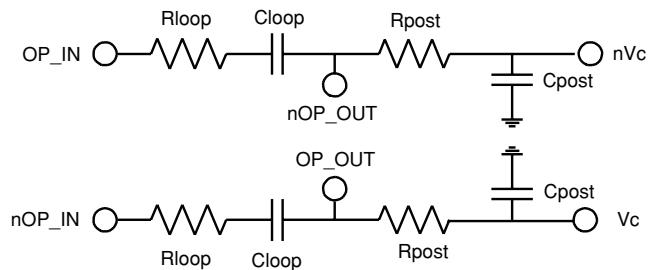
TABLE 1. RECOMMENDED LOOP FILTER VALUES

REF_CLK Frequency	VCSO Frequency	M	N	Fout	Rloop	Cloop	Rpost	Cpost
19.44MHz	622.0800MHz	32	1	622.0800MHz	5KΩ	1MF	50KΩ	100pf

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PIN DESCRIPTIONS

TABLE 2

Pin Number	Name	I/O	Configuration	Description
1, 2, 3	GND	GND		Power Supply Ground
4, 9	OP_IN, nOP_IN	Analog I/O		Used for external loop filter. See Figure 2.
5, 8	nOP_Out, OP_OUT	Analog I/O		Used for external loop filter. See Figure 2.
6, 7	nVC, VC	Input		VCSO Differential Control Voltage Input Pair
10, 14, 26	GND	GND		Power Supply Ground
11, 19, 22, 33	VCC	Power		Positive Supply Pins
12	HOLD	Input	Pull - down	When HIGH the device operates in digital HOLD mode. LVCMOS / LVTTL interface levels.
13	N1	Input	Pull - down	Determines the output divider value as defined in Table 3C. LVCMOS / LVTTL interface levels.
15, 16	FOUT, nFOUT	Output	Unterminated	Differential output, 3.3V LVPECL levels.
17	MR	Input	Pull - down	Logic HIGH resets the reference frequency and N output dividers. Logic LOW enables the outputs. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pull - down	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK.
20	S_DATA	Input	Pull - down	Shift register serial input. Data is sampled on the rising edge of S_CLOCK.
21	S_LOAD	Input	Pull - down	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels
23	REF_CLK1	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
24	REF_CLK0	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
25	REF_SEL	Input	Pull - down	Selects between the different reference clock inputs as the PLL reference source. See Table 3D. LVCMOS / LVTTL interface levels.
27, 28, 29, 30, 31 32, 34, 35, 36	N/C			No connection. Internal test pins.

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PIN CHARACTERISTICS

TABLE 4

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

PARALLEL & SERIAL MODES FUNCTION

TABLE 5A

MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	Conditions
H	X	X	X	X	X	X	Reset, Forces outputs LOW.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

Note: L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

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PARALLEL MODE FUNCTION

TABLE 5B

Inputs N1	Inputs N2	N Divider Value	Output Frequency (MHz) Min	Output Frequency (MHz) Max
0	0	1	311	700
1	0	4	77.75	175

SERIAL MODE FUNCTION

TABLE 5C

Inputs REF_SEL	Reference
0	REF_CLK0
1	REF_CLK1

POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			162		mA

$V_{CC}= 3.3V \pm 5\%$, $T_A= 0°C$ to $70°C$

LVCMOS/LVTTL DC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{IH}	Input High Voltage	REF_SEL, S_LOAD, S_DATA, S_CLOCK, N1, MR		2	VCC + 0.3	V
		REF_CLK0, REF_CLK1		2	VCC + 0.3	V
V_{IL}	Input Low Voltage	REF_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, MR		-0.3	0.8	V
		REF_CLK0, REF_CLK1		-0.3	1.3	V
I_{IH}	Input High Current	N1, MR, S_CLOCK, S_DATA, S_LOAD, REF_SEL, REF_CLK0, REF_CLK1	$V_{DD} = V_{IN} = 3.465V$		150	µA
I_{IL}	Input Low Current	N1, MR, S_CLOCK, S_DATA, S_LOAD, REF_SEL, REF_CLK0, REF_CLK1	$V_{DD} = 3.465$, $V_{IN} = 0V$	-5		µA
V_{OH}	Output High Voltage; NOTE 1			2.6		V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

Note 1: Outputs terminated with 50Ω to V_{CC} /2. See Parameter Measurement section, 3.3V Output Load Test Circuit.

LVPECL DC CHARACTERISTICS

Symbol	Parameter	Signal	Min	Max	Units
V_{OH}	Output High Voltage	FOUT, nFOUT	Vcc – 1.4	Vcc – 1.0	V
V_{OL}	Output Low Voltage	FOUT, nFOUT	Vcc – 2.0	Vcc – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	FOUT, nFOUT	0.6	0.85	V

Note 1: Output terminated with 50Ω to V_{CC} −2.V

INPUT FREQUENCY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
F_{IN}	Input Frequency	REF_CLK0, REF_CLK1	0.005	170	MHz
		S_CLOCK		50	V

Note: Output terminated with 50Ω to $V_{CC} - 2.V$

AC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency			77.75		667	MHz
ØNOISE	Single Side Band		1 KHz offset		-72		dBc/Hz
	Phase Noise		10 kHz offset		-94		dBc/Hz
			100 kHz offset		-123		dBc/Hz
J (t)	Jitter (RMS)		12 kHz to 20 MHz		0.69		ps
odc	Output Duty Cycle				50		%
t_R (Note 1)	Output Rise Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	Fout = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		Fout = 311MHz		325	425	500	ps
		Fout = 622MHz		200	275	350	ps
t_F (Note 1)	Output Fall Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	Fout = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		Fout = 311MHz		325	425	500	ps
		Fout = 622MHz		200	275	350	ps
t_S	Setup Time	M, N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_H	Hold Time	M, N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_{LOCK}	PLL Lock Time					1	ms
t_{PW}	Output Pulse Width	S_LOAD				TBD	ns
F_{HOLD}	Initial Frequency Accuracy in Digital HOLD Mode		Stable Input Clock Selected Until Entering Digital Hold		10		ppm

Note: The output frequencies of 155MHz, 311MHz and 622MHz were chosen for device characterization as these are common optical network clock frequencies.

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PARAMETER MEASUREMENT INFORMATION

DIFFERENTIAL INPUT LEVEL

VCC

nDIFF_CLK

V_{PP} — Cross Points — V_{CMR}

DIFF_CLK

VEE
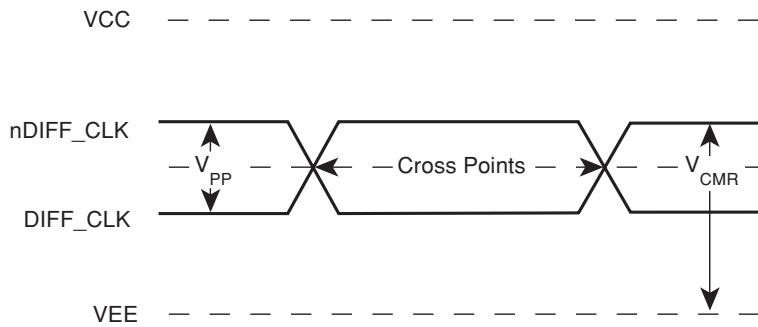
INPUT AND OUTPUT RISE AND FALL TIME

80%   80% V_{SWING}

20%   20%

Clock Inputs
and Outputs

t_R t_F

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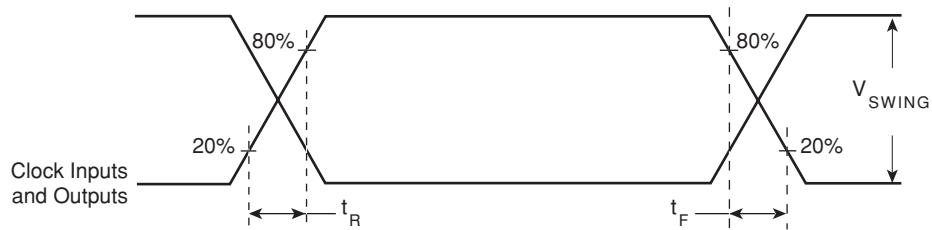
PARAMETER MEASUREMENT INFORMATION

ODC & t$_{PERIOD}$
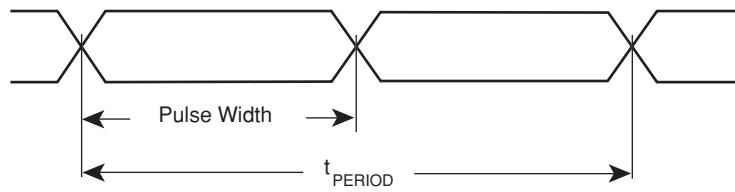
$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

SETUP AND HOLD TIME

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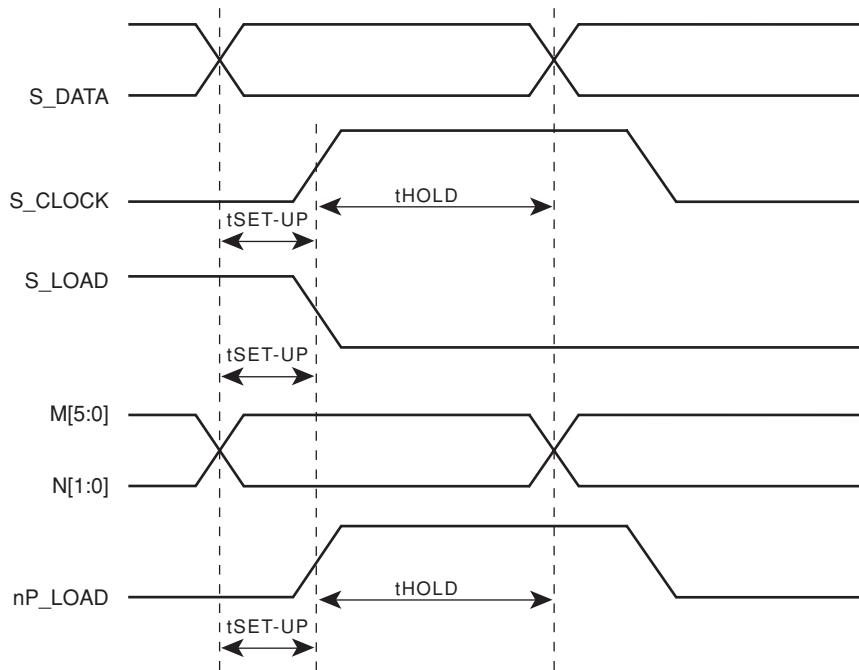
MECHANICAL DIMENSIONS & PIN CONFIGURATION

.354 [9.0]

#27 #19

#28

#18

.354 [9.0]

#36 #10

ORIENTATION TAB

Pin #1

.110 [2.8]

.200 [5.1]

.025 [0.6]

.041 [1.0]

R.006 [R0.2]

.007 [0.2]

PIN#	DESIGNATION	PIN#	DESIGNATION
1	GND	18	S_CLOCK
2	GND	19	VDD
3	GND	20	S_DATA
4	OP_IN	21	S_LOAD
5	nOP_OUT	22	VDD
6	nVC	23	REF_CLK1
7	VC	24	REF_CLK0
8	OP_OUT	25	REF_SEL0
9	nOP_IN	26	GND
10	GND	27	N/C
11	VDD	28	N/C
12	HOLD	29	N/C
13	N1	30	N/C
14	GND	31	N/C
15	FOUT	32	N/C
16	nFOUT	33	VDD
17	MR	34, 35, 36	N/C
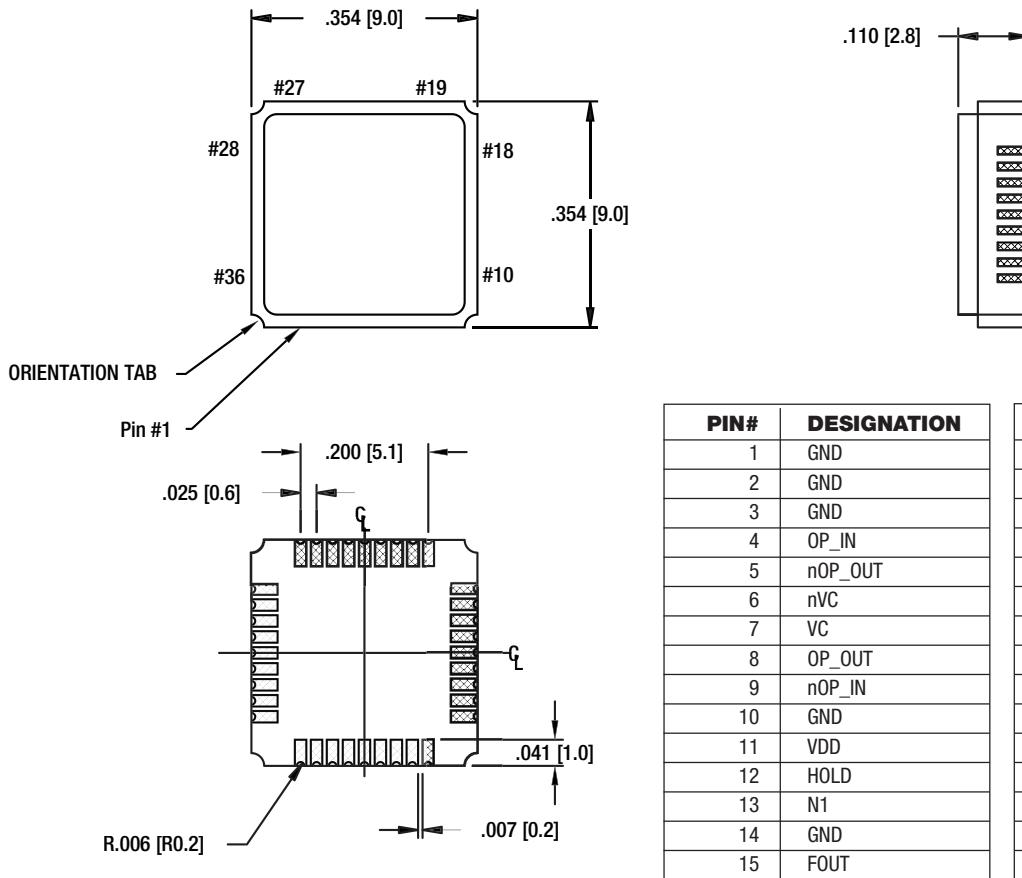
1. DIMENSIONS ARE IN INCHES, ( ) ARE IN MM.

ORDERING INFORMATION

Part Number M2005-02 - 622.0800

Series
Model
VCSO Frequency
(i.e. 622.0800MHz)

Available VCSO Frequencies

622.0800	669.1281
625.0000	669.3266
627.3296	672.1600
644.5313	690.5692
666.5143	693.4830