

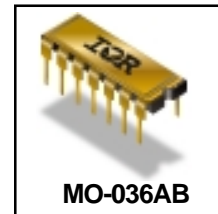
**POWER MOSFET
 THRU-HOLE (MO-036AB)**

**IRFG9110
 JANTX2N7335
 JANTXV2N7335
 REF:MIL-PRF-19500/599
 100V, QUAD P-CHANNEL
 HEXFET® MOSFET TECHNOLOGY**

Product Summary

| Part Number | RDS(on) | ID |
|-------------|---------|--------|
| IRFG9110 | 1.4Ω | -0.75A |

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.



Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light-weight

Absolute Maximum Ratings

| | Parameter | | Units |
|-----------------------------|---------------------------------|---|-------|
| ID @ VGS = -10V, TC = 25°C | Continuous Drain Current | -0.75 | A |
| ID @ VGS = -10V, TC = 100°C | Continuous Drain Current | -0.5 | |
| IDM | Pulsed Drain Current ① | -3.0 | |
| PD @ TC = 25°C | Max. Power Dissipation | 1.4 | W |
| | Linear Derating Factor | 0.011 | W/°C |
| VGS | Gate-to-Source Voltage | ±20 | V |
| EAS | Single Pulse Avalanche Energy ② | 75 | mJ |
| IAR | Avalanche Current ① | — | A |
| EAR | Repetitive Avalanche Energy ① | — | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | -5.5 | V/ns |
| TJ | Operating Junction | -55 to 150 | °C |
| TSTG | Storage Temperature Range | | |
| | Lead Temperature | 300 (0.063 in.(1.6mm) from case for 10s) | |
| | Weight | 1.3 (typical) | g |

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------------------------|--|------|--------|-------------|---------------------|---|
| BV _{DSS} | Drain-to-Source Breakdown Voltage | -100 | — | — | V | V _{GS} = 0V, I _D = -1.0mA |
| ΔBV _{DSS} /ΔT _J | Temperature Coefficient of Breakdown Voltage | — | -0.098 | — | V/°C | Reference to 25°C, I _D = -1.0mA |
| R _{DS(on)} | Static Drain-to-Source On-State Resistance | — | — | 1.4 1.73 | Ω | V _{GS} = -10V, I _D = -0.5A ^④ V _{GS} = -10V, I _D = -0.75A ^④ |
| V _{GS(th)} | Gate Threshold Voltage | -2.0 | — | -4.0 | V | V _{DS} = V _{GS} , I _D = -250μA |
| g _{fs} | Forward Transconductance | 0.67 | — | — | S (r _s) | V _{DS} > -15V, I _{DS} = -0.5A ^④ |
| I _{DSS} | Zero Gate Voltage Drain Current | — | — | -25 -250 | μA | V _{DS} = -80V, V _{GS} = 0V V _{DS} = -80V V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Leakage Forward | — | — | -100 | nA | V _{GS} = -20V |
| I _{GSS} | Gate-to-Source Leakage Reverse | — | — | 100 | nA | V _{GS} = 20V |
| Q _g | Total Gate Charge | — | — | 15 | nC | V _{GS} = -10V, I _D = -0.75A V _{DS} = -50V |
| Q _{gs} | Gate-to-Source Charge | — | — | 7.0 | nC | |
| Q _{gd} | Gate-to-Drain ('Miller') Charge | — | — | 8.0 | nC | |
| t _{d(on)} | Turn-On Delay Time | — | — | 30 | ns | V _{DD} = -50V, I _D = -0.75A V _{GS} = -10V, R _G = 7.5Ω |
| t _r | Rise Time | — | — | 60 | | |
| t _{d(off)} | Turn-Off Delay Time | — | — | 40 | | |
| t _f | Fall Time | — | — | 40 | | |
| L _S + L _D | Total Inductance | — | 10 | — | nH | Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package) |
| C _{iss} | Input Capacitance | — | 200 | — | pF | V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz |
| C _{oss} | Output Capacitance | — | 85 | — | | |
| C _{rss} | Reverse Transfer Capacitance | — | 30 | — | | |

Source-Drain Diode Ratings and Characteristics

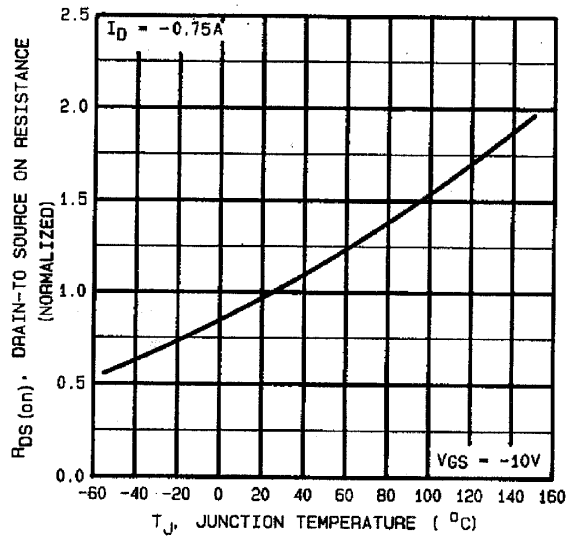
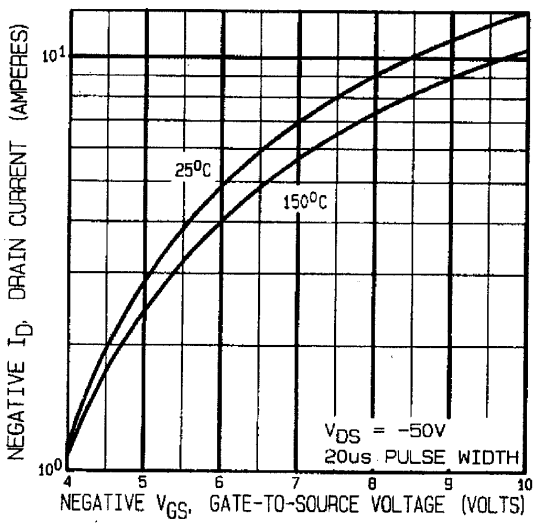
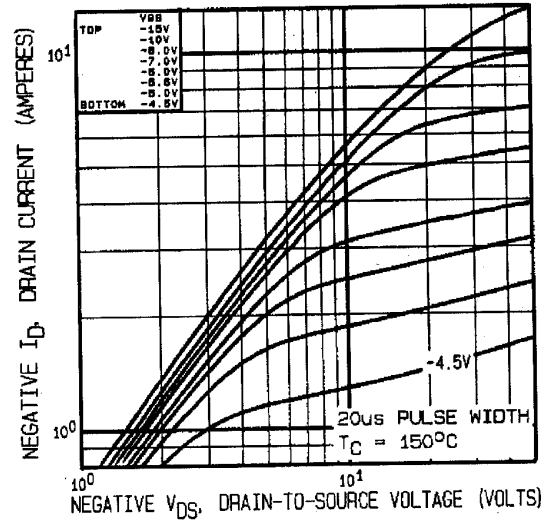
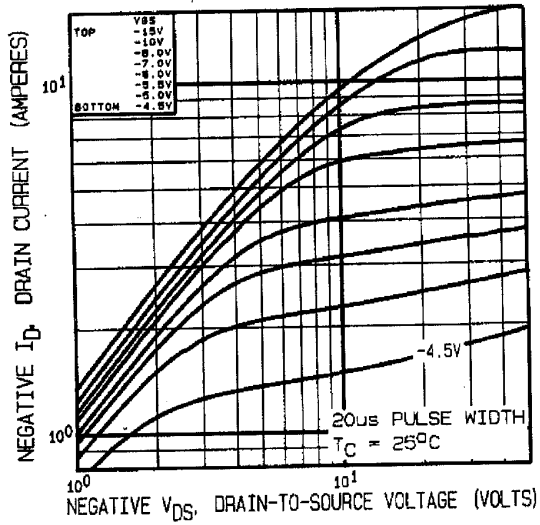
| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-----------------|--|--|-----|-------|-------|---|
| I _S | Continuous Source Current (Body Diode) | — | — | -0.75 | A | |
| I _{SM} | Pulse Source Current (Body Diode) ^① | — | — | -3.0 | | |
| V _{SD} | Diode Forward Voltage | — | — | -5.5 | V | T _j = 25°C, I _S = -0.75A, V _{GS} = 0V ^④ |
| t _{rr} | Reverse Recovery Time | — | — | 200 | nS | T _j = 25°C, I _F = -0.75A, di/dt ≤ 100A/μs |
| Q _{RR} | Reverse Recovery Charge | — | — | 9.0 | μC | V _{DD} ≤ -50V ^④ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D . | | | | |

Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------|---------------------|-----|-----|-----|-------|----------------------|
| R _{thJC} | Junction-to-Case | — | — | 17 | °C/W | Typical socket mount |
| R _{thJA} | Junction to Ambient | — | — | 90 | | |

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page



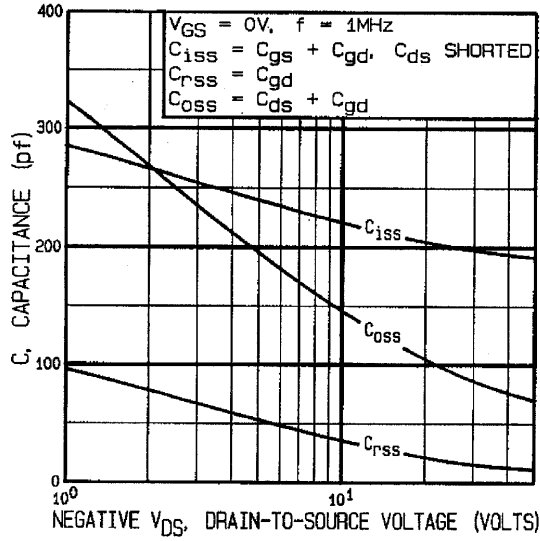


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

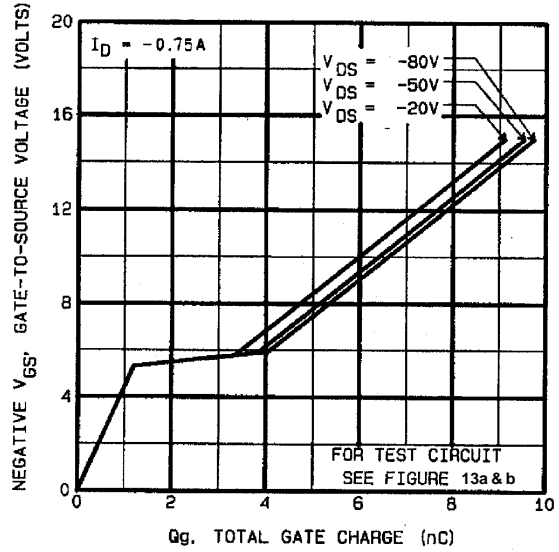


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

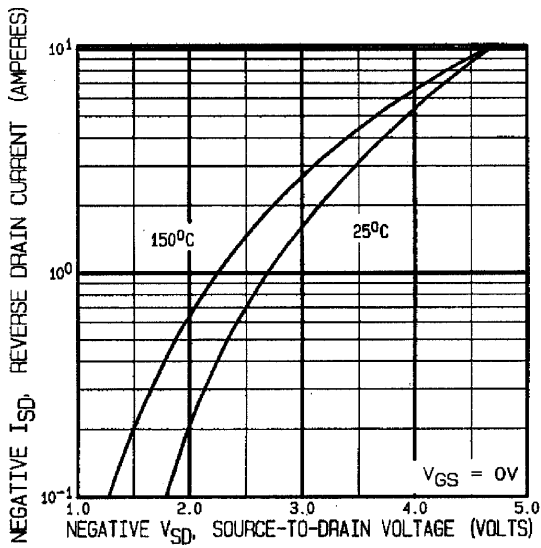


Fig 7. Typical Source-Drain Diode Forward Voltage

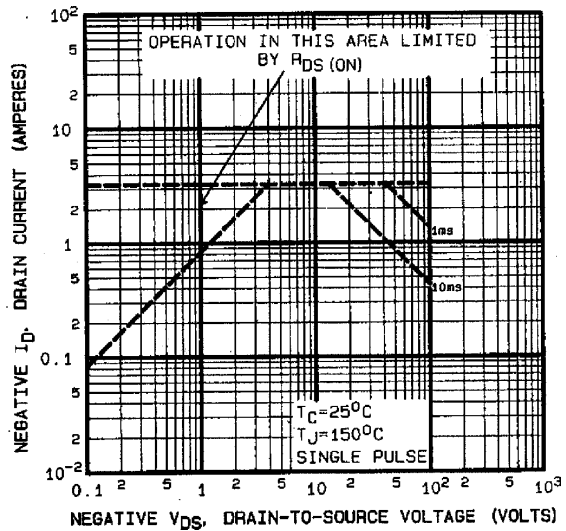


Fig 8. Maximum Safe Operating Area

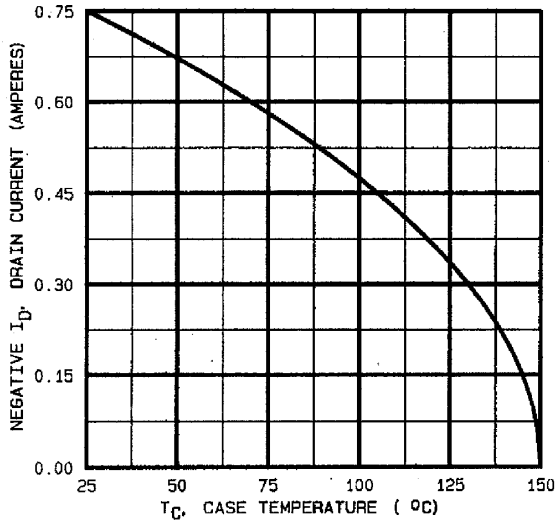


Fig 9. Maximum Drain Current Vs. Case Temperature

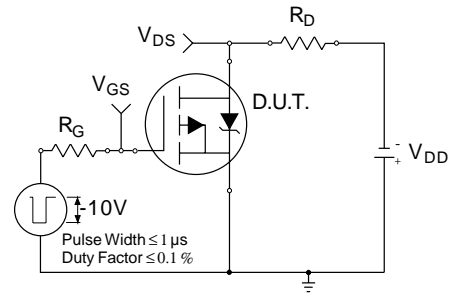


Fig 10a. Switching Time Test Circuit

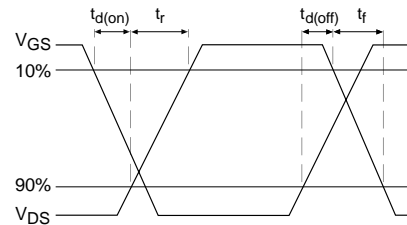


Fig 10b. Switching Time Waveforms

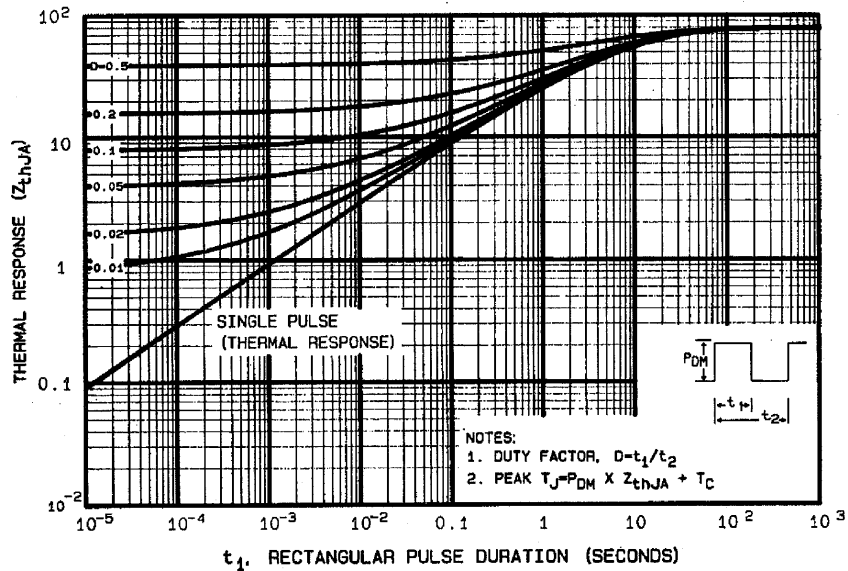


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

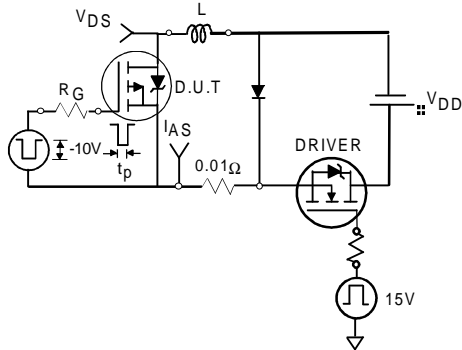


Fig 12a. Unclamped Inductive Test Circuit

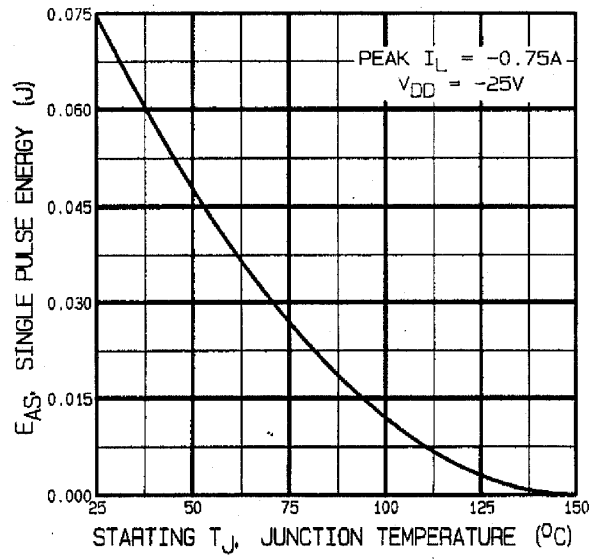


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

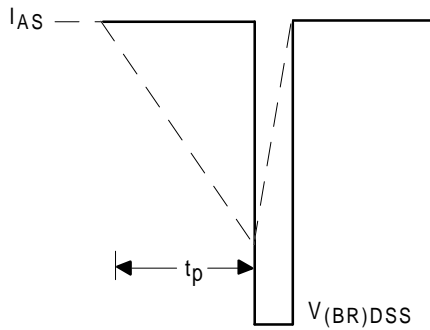


Fig 12b. Unclamped Inductive Waveforms

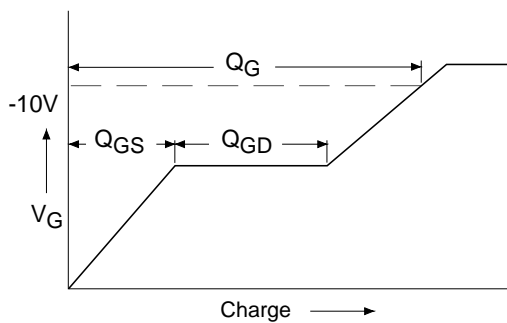


Fig 13a. Basic Gate Charge Waveform

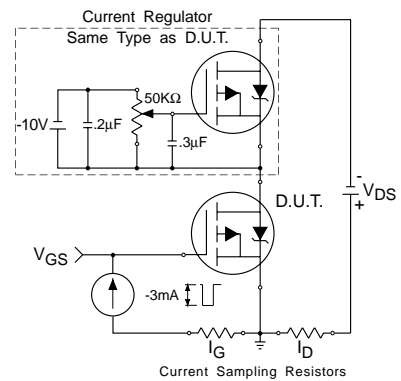
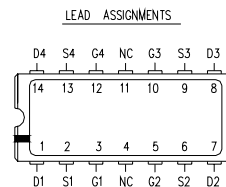
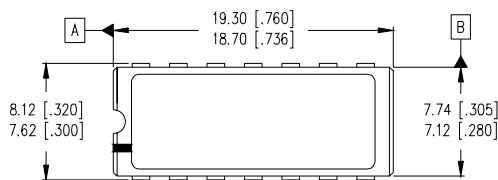


Fig 13b. Gate Charge Test Circuit

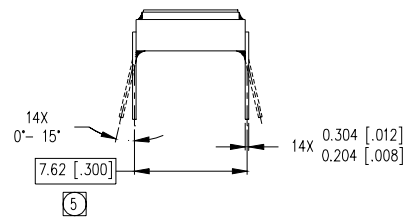
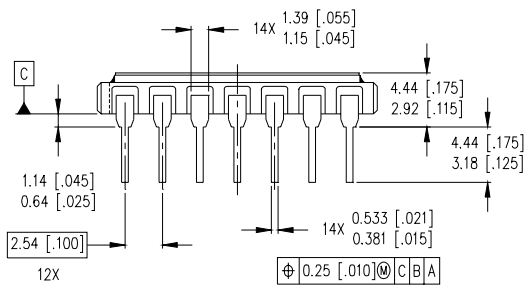
Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 266mH$
 Peak $I_L = -0.75A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -0.75A$, $di/dt \leq -75A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — MO-036AB



LEGEND
 G = GATE S = SOURCE
 D = DRAIN NC = NO CONNECTION



NOTES:

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.