TECHNICAL MANUAL

LSI53C770 Ultra SCSI I/O Processor

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This document describes the LSI Logic LSI53C770 Ultra SCSI I/O Processor and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This technical manual provides reference information on the LSI53C770 Ultra SCSI I/O Processor. It contains a complete functional description for the product and includes complete physical and electrical specifications for it.

Audience

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards.

Organization

This document has the following chapters and appendix:

- Chapter 1, **General Description**
- Chapter 2, **Functional Description**
- Chapter 3, **Signal Descriptions**
- Chapter 4, **Registers**
- Chapter 5, **Instruction Set of the I/O Processor**
- Chapter 6, **Electrical Characteristics**
- Appendix A, **Register Summary**

Related Publications

For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-199X (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253
(SCSI-3 Parallel Interface)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

LSI Logic World Wide Web Home Page
www.lsil.com

PCI Special Interest Group
2575 N. E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in a "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Revision Record

Version	Date	Remarks
1.0	9/94	Preliminary.
2.0	7/96	Changed Fast-20 to Ultra SCSI throughout document.
2.1	3/01	All product names changed from SYM to LSI.

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Chapter 1
General Description

This chapter contains the following sections:

The LSI53C770 Ultra SCSI I/O Processor is a member of the LSI53C7XX family of intelligent, single chip, third generation SCSI host adapters. A high-performance SCSI core and an intelligent 16- or 32-bit bus master DMA core are integrated with a SCSI SCRIPTS™ processor to accommodate the flexibility requirements of not only SCSI-1, SCSI-2, and future SCSI standards. The LSI53C770 solves the protocol overhead problems that have plagued all previous intelligent and nonintelligent adapter designs.

The LSI53C770 is designed to completely implement a multithreaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the LSI53C770 provides automatic relocation of SCRIPTS, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The LSI53C770 allows easy firmware upgrades and is SCRIPTS compatible with the LSI53C710 and the LSI53C8XX family.

The LSI53C770 supports four different host processor interfaces, or bus modes. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the Motorola 68040 interface. Bus Mode 3 closely resembles the Intel 80386SX interface; the 16-bit host interface should be enabled in this mode. Finally, Bus Mode 4 closely resembles the 80386DX interface. Bus Modes 1, 2, and 4 support both the big and

little endian byte ordering schemes and Bus Mode 3 supports little endian byte ordering, for a total of seven operating modes. Select the modes by using the bus mode select pins (BS[2:0]).

The LSI53C770 is a pin-for-pin replacement of the LSI53C720. It performs Ultra SCSI data transfers at 20 Mbytes/s (8-bit) or 40 Mbytes/s (16-bit). It is packaged in a 208-pin quad flat pack, and performs both Single-Ended (SE) and differential transfers.

1.1 Benefits of Ultra SCSI

Ultra SCSI is an extension of the SCSI-3 standard that expands the bandwidth of the SCSI bus and allows faster synchronous SCSI transfer rates. When enabled, Ultra SCSI performs 20 megatransfers during an I/O operation, resulting in approximately twice the synchronous transfer rates of fast SCSI-2. The LSI53C770 can perform 8-bit, Ultra SCSI synchronous transfers as fast as 20 Mbytes/s. This advantage is most noticeable in heavily loaded systems or large block size requirements, such as video on-demand and image processing.

An advantage of Ultra SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments. The LSI53C770 is compatible with all existing LSI53C720 and LSI53C720SE software; the only changes required are to enable the chip to perform synchronous negotiations for Ultra SCSI rates. The LSI53C770 can use the same board socket as an LSI53C720, with the addition of an 80/100 MHz SCLK or internal SCSI clock doubler (clock doubler works at 40 to 50 MHz input) which provides the correct frequency when transferring synchronous SCSI data at 50 ns transfer rates. Some changes to existing cabling or system designs may be needed to maintain signal integrity at Ultra SCSI synchronous transfer rates. These design issues are discussed in Chapter 2.

1.1.1 TolerANT® Technology

The LSI53C770 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives SCSI REQ, ACK, Data, and Parity signals HIGH by transistors on each pin. The 48 mA drivers actively force the SCSI bus signal to the HIGH (negated) state faster than

passive pull-up drivers. TolerANT receivers filter SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate the double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT technology improves data integrity in unreliable cabling environments where other devices would be subject to data corruption. The benefits of TolerANT technology include increased immunity to noise when the signal is going HIGH, increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. Setting bit 7 in the SCSI Test Register Three (STEST3) register enables active negation. It can be used in both SE and differential mode. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.2 LSI53C770 Features Summary

This section provides an overview of the LSI53C770 features and benefits. It contains information on Performance, Integration, Ease of Use, Flexibility, Reliability, and Testability.

1.2.1 Performance

To improve performance, the LSI53C770:

- Performs Ultra SCSI synchronous transfers as fast as 40 Mbytes/s (with wide SCSI)
- Includes 4 Kbytes internal RAM for SCRIPTS instruction storage
- Supports variable block size and scatter/gather data transfers
- Supports 16- and 32-bit data bursts with variable burst lengths
- Performs memory-to-memory DMA transfers in excess of 44 Mbytes/s
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces ISR overhead with unique interrupt status reporting
- Performs memory transfers in excess of 100 Mbytes/s (@ 33 MHz)

- Uses a 96-byte DMA FIFO to support cache line bursting
- Uses up to 16 levels of synchronous SCSI offset for optimum speed matching during Ultra SCSI transfers
- Provides an additional 32 scratch registers

1.2.2 Integration

Features of the LSI53C770 which ease integration include:

- Full 16- or 32-bit DMA bus master
- High-performance wide SCSI core
- RISC-based SCSI SCRIPTS processor
- Allows intelligent host adapter performance on a mainboard

1.2.3 Ease of Use

The LSI53C770:

- Reduces SCSI development effort
- Supports big and little endian environments
- Uses existing LSI53C720 SCRIPTS
- Includes development tools and sample SCSI SCRIPTS
- Supports maskable and pollable interrupts
- Supports wide SCSI, A or P cable, and up to 16 devices
- Interfaces with seven different host processor buses, including Motorola (680X0 family) and Intel (80X86 family)
- Supports odd byte block sizes in conjunction with wide SCSI
- Provides three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 1.6 seconds.
- The handshake-to-handshake and general purpose timers use a scale factor to increase the amount of time before expiration.
- The handshake-to-handshake timer has an optional mode that allows it to operate as a bus activity timer for all SCSI transfers.

1.2.4 Flexibility

The LSI53C770 provides:

- A high level programming interface (SCSI SCRIPTS)
- Tailored SCSI sequences to be executed from main memory or from a host adapter board's local memory
- Use of flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Changes in the logical I/O interface definition
- Low level programmability (register oriented)
- A target to disconnect and later reselect with no interrupt to the system processor
- A multithreaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching
- Relative jumps
- Indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Separate SCSI and system clocks
- Double the SCSI clock input during Ultra SCSI transfer modes
- A new SSAID (SCSI Selected as ID) register

1.2.5 Reliability

Enhanced reliability features of the LSI53C770 include:

- TolerANT SCSI driver and receiver technology
- 2 kV ESD protection on SCSI signals
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed-through protection (minimum leakage current through SCSI pads)

- 20% of pins power and ground
- Ground isolation of I/O pads and chip logic

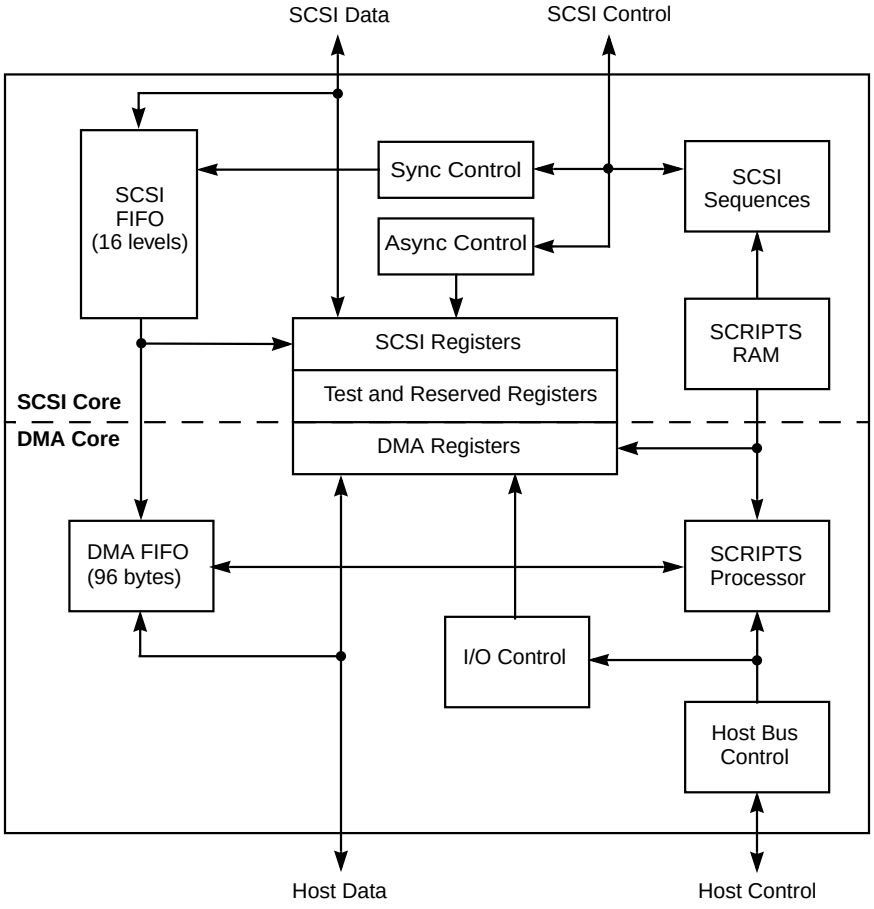
1.2.6 Testability

The LSI53C770 provides improved testability through:

- Access to all SCSI signals through programmed I/O
- SCSI loopback diagnostics
- Self-selection capability
- SCSI bus signal continuity checking
- Support for single step mode operation

Figure 1.1 illustrates the LSI53C770 Block Diagram.

Figure 1.1 LSI53C770 Block Diagram



1.3 Summary of New Features in the LSI53C770

For more information on enabling or using these new features, please refer to the chapter indicated with each topic.

- Support for Ultra SCSI data transfers (Chapter 2, Chapter 4, and Chapter 6)
- DMA FIFO increased to 96 bytes (Chapter 2)
- SCSI offset increased to 16 levels (Chapter 4, SCSI Transfer (SXFER) register description)
- Internal SCRIPTS RAM (Chapter 2, Chapter 4)
- Expanded timers (Chapter 4, SCSI Timer Register 0 (STIME0) and SCSI Timer Register One (STIME1) register descriptions)
- Expanded SCSI Longitudinal Parity (SLPAR) register (Chapter 4, SCSI Longitudinal Parity (SLPAR) register description)
- Additional Read-Modify-Write Instructions (Chapter 5, Read/Write instructions)
- SCSI Clock Doubler (Chapter 2, Chapter 4)
- SCSI Selector ID Register (SSID) register (Chapter 4)
- Fairness timer update (Chapter 4, DMA Mode (DMODE) register description)
- Additional 32 Scratch registers (Chapter 4)
- Vendor unique enhancements (Chapter 4, SCSI Control Register Two (SCNTL2) register description)
- DIFFSENSE Sense bit to detect a differential System (Chapter 5, SCSI Status Two (SSTAT2) register description)

Chapter 2
Functional Description

The LSI53C770 is composed of three interrelated functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor.

This chapter contains the following sections:

This chapter describes the major functional aspects of the chip. For detailed information on implementing or using specific features, refer to later chapters in this manual. Chapter 3 contains detailed information on the LSI53C770 pins. Chapter 4 describes all of the operating registers and bits. Chapter 5 describes the LSI53C770 instruction set, and Chapter 6 contains the chip electrical specifications and timing data.

2.1 SCSI Core

The SCSI core supports the SCSI-2 fast and wide bus. It supports synchronous transfer rates of up to 20 Mbytes/s or 40 Mbytes/s in Ultra SCSI, and asynchronous transfer rates up to 10 Mbytes/s. The programmable SCSI interface makes it easy to “fine tune” the system for specific mass storage devices or advanced SCSI requirements.

The SCSI core offers low level register access or a high level control interface. Like first generation SCSI devices, the LSI53C770 SCSI core can be accessed as a register oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. This can test all data paths in the chip. The LSI53C770 uses an "AND tree" to test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the SCRIPTS processor, a high level logical interface optimized for SCSI protocol. SCRIPTS routines controlling the SCSI core are fetched out of the main host memory or local PROM. These commands instruct the SCSI core to select, reselect, disconnect, wait for a disconnect, transfer information, change bus phases and in general, implement all aspects of the SCSI protocol.

2.1.1 DMA Core

The DMA core is a bus master DMA device that is made to attach to Intel (80386SX and 80386DX), and Motorola (68030 and 68040) processors.

The LSI53C770 supports 16- or 32-bit memory and automatically supports misaligned DMA transfers. A 96-byte FIFO allows the LSI53C770 to burst two, four, eight, or 16 Dwords across the memory bus interface. This DMA interface does not support dynamic bus sizing.

The DMA core communicates with the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

2.2 SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI commands to be fetched from host memory or internal SCRIPTS RAM. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores, which are executed from 16- or 32-bit system memory. The SCRIPTS processor executes complex SCSI bus sequences independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2–8 ms required for traditional intelligent host adapters. The SCRIPTS processor supports customized algorithms to tune SCSI bus performance, adjust to new bus device types (i.e. scanners, communication gateways, etc.), or incorporate changes in the SCSI logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are hardware independent, so they can be used interchangeably on any host or CPU system bus.

2.2.1 Internal SCRIPTS RAM

The LSI53C770 has 4 Kbytes (1000 x 32 bits) of internal, general purpose RAM. The RAM is designed for SCRIPTS program storage, but is not limited to this type of information. When the chip fetches SCRIPTS instructions or Table Indirect information from the internal RAM, these fetches remain internal to the chip and do not use the host bus. Other types of access to the RAM by the LSI53C770 use the host bus as if they were external accesses. When the internal RAM is enabled, the LSI53C770 uses the shadowed Scratch Register A (SCRATCHA) register as the base address of the RAM when bit 0 is set in the Chip Test Five (CTEST5) register.

The internal RAM can be enabled and used in the following ways:

- Register based through indexed addressing.
- Increased chip select address space that includes support for the chip registers and internal RAM with a single chip select pin.
- An additional chip select pin supporting only internal RAM with the original Chip Select pin supporting only the chip registers.

The register based method allows use of the SCRIPTS RAM in existing LSI53C720 designs without hardware changes. To use this method, clear Chip Test Five (CTEST5), bit 2 and set Chip Test Five (CTEST5), bit 1. The internal RAM is mapped into the chip registers using indexed addressing in a shadowed Scratch Register B (SCRATCHB) register. The RAM replaces the Scratch Registers C–J (SCRATCHC–J) registers, and may optionally be used as a block of scratchpad RAM. When the chip determines that a SCRIPTS address is in the internal RAM space, the opcode fetch sequence accesses the internal RAM without using the host bus. Indirect and table indirect functions also determine if the address is contained in internal RAM space and fetch data from the RAM

without host bus access. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running, but the host cannot access the RAM during SCRIPTS operation.

The increased chip select address space method defines 4 Kbyte address space for the chip registers and the 4 Kbyte space for the SCRIPTS RAM. To enable this mode, set Chip Test Five (CTEST5), bit 2 and clear Chip Test Five (CTEST5), bit 1. The registers are located at addresses 0x0000 through 0x007F, repeating at intervals of 128 bytes until the 4 K byte boundary. The RAM occupies addresses 0x1000 through 0x1FFF. The RAM is accessible by the host during SCRIPTS execution, but up to seven additional wait-states may be added to a slave read or write access if it occurs while an internal SCRIPTS access is in progress. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running.

An additional chip select pin, the RAMCS/ pin, can be used to define a 4 Kbyte address space for the internal RAM by setting bits 1 and 2 of the Chip Test Five (CTEST5) register. The RAM is accessible by the host during SCRIPTS execution, but up to seven additional wait-states may be added to a slave read or write access if it occurs while an internal SCRIPTS access is in progress. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running.

2.2.2 Designing an Ultra SCSI System

Migrating an existing SE SCSI design from SCSI-2 to Ultra SCSI requires minor software modifications as well as consideration for some hardware design guidelines. Since Ultra SCSI is based on existing SCSI standards, it can use existing software programs as long as the software is able to negotiate for Ultra SCSI synchronous transfer rates.

In the area of hardware, the primary area of concern in SE systems is to maintain signal integrity at high data transfer rates. To assure reliable operation at Ultra SCSI transfer speeds, follow the system design parameters recommended in the SCSI-3 Fast-20 Parallel Interface draft standard. Chapter 6 contains Ultra SCSI timing information. In addition to the guidelines in the draft standard, make the following software and hardware adjustments to accommodate Ultra SCSI transfers:

- Set the Ultra Enable bit to enable Ultra SCSI transfers. (SCSI Control Three (SCNTL3), bit 7).
- Set the TolerANT Enable bit, bit 7 in the SCSI Test Register Three (STEST3) register whenever the Ultra SCSI Enable bit is set.
- Do not extend the SREQ/SACK filtering period with SCSI Test Register Two (STEST2), bit 1.
- Use an 80/100 MHz SCSI clock or enable the SCSI clock doubler (clock doubler works at 40 to 50 MHz input) using bits 2 and 3 of the SCSI Test Register One (STEST1) register. Set the halt SCSI clock (HSC) bit in SCSI Test Register Three (STEST3) before switching to the doubled SCSI clock.

2.2.3 Using the SCSI Clock Doubler

The LSI53C770 can double the frequency of a 40–50 MHz SCSI clock, allowing the system to perform Ultra SCSI transfers in systems that do not have 80 MHz clock input. This option is user-selectable with bit settings in the SCSI Test Register One (STEST1), SCSI Test Register Three (STEST3), and SCSI Control Three (SCNTL3) registers. At power-on or reset, the doubler is disabled and powered down. Follow these steps to use the clock doubler:

1. Set the SCLK Doubler Enable bit (SCSI Test Register One (STEST1), bit 3).
2. Wait 20 µs.
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (SCSI Test Register Three (STEST3), bit 5).
4. Set the clock conversion factor using the SCF and CCF fields in the SCSI Control Three (SCNTL3) register.
5. Set the SCLK Doubler Select bit (SCSI Test Register One (STEST1), bit 2).
6. Clear the Halt SCSI Clock bit.

2.2.4 Big/Little Endian Support

The Bus Mode Select pin gives the LSI53C770 the flexibility of operating with either big or little endian byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified. The LSI53C770 supports byte, word, and Dword slave accesses in both big and little endian modes (word accesses must be word aligned).

When a Dword is accessed, no repositioning of the individual bytes is necessary, since Dwords are addressed by the address of the least significant byte. SCRIPTS always uses Dwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When a word is accessed, individual bytes must be repositioned. Internally, the LSI53C770 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lanes. The registers always appear on the same byte lane, but the address of the register are repositioned. Words are addressed by the address of the least significant byte. Big/little endian mode selection has the most effect on individual byte access, as illustrated in Table 2.1.

Table 2.1 Big and Little Endian Addressing

System Data Bus	[31:24]	[23:16]	[15:8]	[7:0]
LSI53C770 Pins	[31:24]	[23:16]	[15:8]	[7:0]
Register	SCNTL3	SCNTL2	SCNTL1	SCNTL0
Little Endian Address	0x03	0x02	0x01	0x00
Big Endian Address	0x00	0x01	0x02	0x03

Note: The LSI53C770 supports big endian addressing in 16-bit systems with Bus Modes 1 and 2 only.

Data to be transferred between system memory and the SCSI bus always start at address zero and continue through address ‘n’ - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS are generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instruction in the order that the SCRIPTS processor expects it.

Software drivers for the LSI53C770 should access registers by their logical name (i.e., “SCNTL0”) rather than by their address. The logical name should be equated to the register’s big endian address in big endian mode (SCNTL0 = 0x03), and its little endian address in little endian mode (SCNTL0 = 0x00). This way, there is no change to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed. Addressing of registers from within a SCRIPTS instruction is independent of bus mode. Internally, the LSI53C770 always operates in little endian mode.

2.2.5 Big Endian Mode

Big endian addressing is used primarily in designs based on Motorola processors. The LSI53C770 treats D[31:24] as the lowest physical memory address. The register map is left justified (Address 0x03 = SCNTL0).

2.2.6 Little Endian Mode

Little endian is used primarily in designs based on Intel processors. This mode treats D[7:0] as the lowest physical memory address. The register map is right justified (Address 0x00 = SCNTL0) as detailed in Table 2.1.

2.2.7 Loopback Mode

The LSI53C770 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip talk to itself. This allows diagnostic testing of the DMA and SCSI cores, the SCRIPTS processor, and all internal data paths. When the Loopback Enable bit is set in the SCSI Test Register Two (STEST2) register, the LSI53C770 allows control of all SCSI signals, whether it is operating in initiator or target mode.

2.2.8 Parity Options

The LSI53C770 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

Table 2.2 Bits Used in Parity Control and Generation

Bit Name	Location	Description
Assert ATN/ on Parity Errors	SCSI Control Zero (SCNTL0), bit 1	Causes the LSI53C770 to automatically assert SCSI ATN/ when it detects a parity error (on either the SCSI or the data bus) while operating as an initiator.
Enable Parity Generation	SCSI Control Zero (SCNTL0), bit 2	Determines whether the LSI53C770 generates parity sent to the SCSI bus or allows parity to “flow through” the chip to/from the SCSI bus and system bus.
Enable Parity Checking	SCSI Control Zero (SCNTL0), bit 3	Enables the LSI53C770 to check for parity errors. The LSI53C770 checks for odd parity.
Assert Even SCSI Parity	SCSI Control One (SCNTL1), bit 2	Determines the SCSI parity sense generated by the LSI53C770 being sent to the host. Parity generation must be enabled.
Disable Halt on ATN/ or a Parity Error (Target Mode Only)	SCSI Control One (SCNTL1), bit 5	Causes the LSI53C770 to halt operations when a parity error is detected in target mode.
Enable Parity Error Interrupt	SCSI Interrupt Enable Zero (SIEN0), bit 0	Determines whether the LSI53C770 will generate an interrupt when it detects a parity error.
Parity Error	SCSI Interrupt Status Zero (SIST0), bit 0	This status bit is set whenever the LSI53C770 has detected a parity error on either the SCSI bus or the system bus.
Status of SCSI Parity Signal	SCSI Status Zero (SSTAT0), bit 0 and SCSI Status Two (SSTAT2), bit 0	These status bits represent the live SCSI Parity Signal (SDP0 and SDP1).

Table 2.2 Bits Used in Parity Control and Generation (Cont.)

Bit Name	Location	Description
Latched SCSI Parity Signal	SCSI Status One (SSTAT1), bit 3 and SCSI Status Two (SSTAT2), bit 3	These status bits contain the SCSI parity of the bytes latched in the SCSI Input Data Latch (SIDL).
DMA FIFO Parity	Chip Test Two (CTEST2), bit 3	This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the Chip Test Six (CTEST6) register.
DMA FIFO Parity	Chip Test Zero (CTEST0), bit 3	This write only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the Chip Test Six (CTEST6) register.
SCSI FIFO Parity	SCSI Test Register One (STEST1), bit 0	This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the SCSI Output Data Latch (SODL) register, once bit 0 in SCSI Test Register Three (STEST3) is asserted.
Generate Receive Parity	Chip Test Zero (CTEST0), bit 4	When this bit is set and the LSI53C770 is in parity pass-through mode (bit 2 in the SCSI Control Zero (SCNTL0) register is clear), parity received on the SCSI bus will not pass through the DMA FIFO. New parity will be generated. When this bit is cleared, and parity pass through mode is enabled (Bit 2 of SCSI Control Zero (SCNTL0) is clear), parity received on the SCSI bus will pass through the LSI53C770 unmodified.
Enable Host Parity Checking	Chip Test Four (CTEST4), bit 3	Setting this bit enables parity checking during slave write and DMA read execution, if the Enable Parity Generation bit is cleared (SCSI Control Zero (SCNTL0), bit 2).

Table 2.3 describes the SCSI Parity Control functions.

Table 2.3 SCSI Parity Control

EPG[1]	EPC[2]	AESP[3]	Description
0	0	0	Does not check for parity errors. Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	0	1	Does not check for parity errors. Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	0	Checks for odd parity on both host and SCSI data when received. Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	Checks for odd parity on both host and SCSI data when received. Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.
1	0	0	Does not check for parity errors. Parity on DP[3:0] is ignored. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	0	1	Does not check for parity errors. Parity on DP[3:0] is ignored. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	0	Checks for odd parity on SCSI data received. Parity on DP[3:0] is ignored. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	Checks for odd parity on SCSI data received. Parity on DP[3:0] is ignored. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.

1. Enable Parity Generation.
2. Enable Parity Checking.
3. Assert SCSI Even Parity.

Table 2.4 describes the options available when a parity error occurs. Table 2.4 only applies when the Enable Parity Checking bit is set.

Table 2.4 Parity Errors and Interrupts

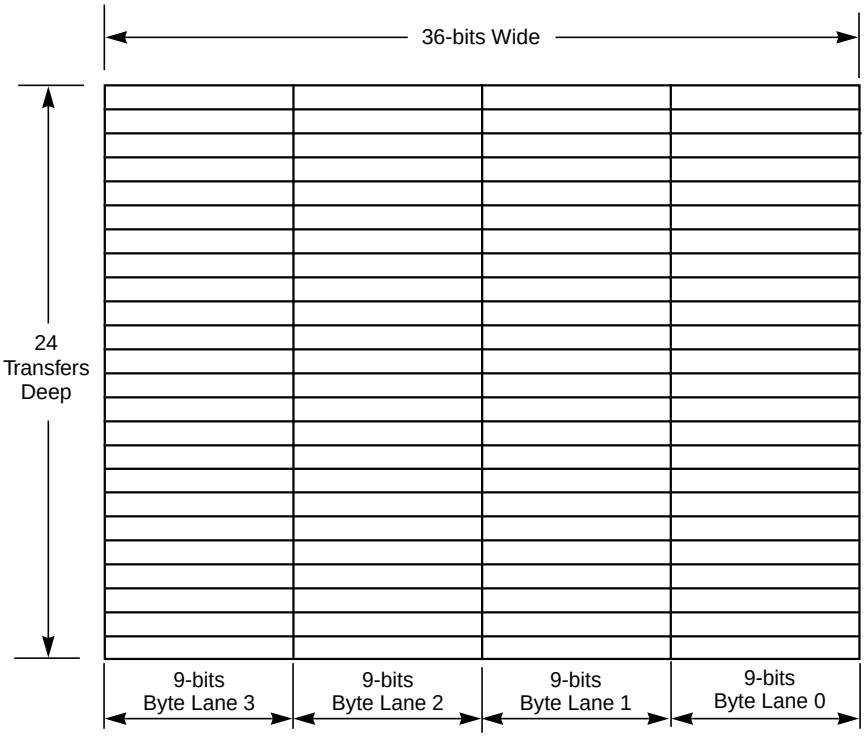
DHP	PAR	Description
0	0	Does not halt when a parity error occurs in target or initiator mode.
0	1	Does not halt when a parity error occurs in target or initiator mode. [1]
1	0	Does not halt when a parity error occurs in target or initiator mode.
1	1	Halts when a parity error occurs in target mode and will generate an interrupt in target or initiator mode

1. Initiator mode parity error interrupts are generated at the end of a block move.

2.3 DMA FIFO

The LSI53C770 DMA FIFO is a 36 x 24 bit FIFO. It is divided into 4 byte lanes, each 9 bits wide and 24 transfers deep, as shown in Figure 2.1.

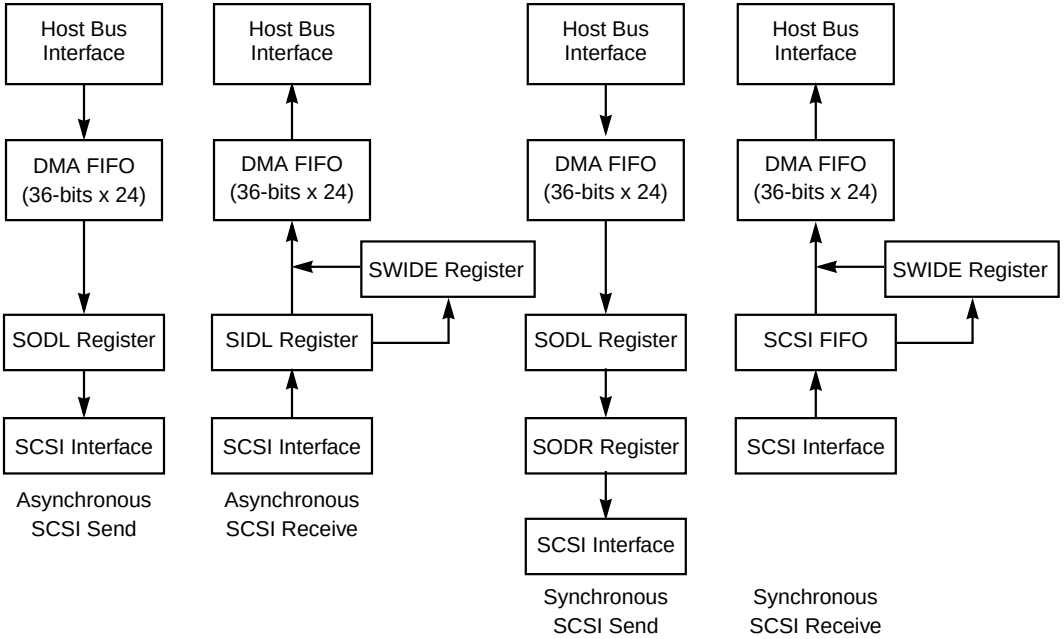
Figure 2.1 DMA FIFO Byte Lanes



2.3.1 Data Path

When the LSI53C770 halts a data transfer operation, check the data path to determine if any bytes remain that have not been transferred. The data path through the LSI53C770 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously. Figure 2.2 shows how data is moved to/from the SCSI bus in each of the different modes.

Figure 2.2 LSI53C770 Data Paths



2.3.2 DMA FIFO

In all types of transfers, the DMA FIFO is used in the data path. The DFE bit in the DMA Status (DSTAT) register indicates whether there is any data in the DMA FIFO. To check the DMA FIFO, use the following procedure. The other parts of the data path may contain data. To check the data path, follow the steps indicated for each type of transfer.

2.3.2.1 Checking the Data Path

When transferring data from the host bus to the SCSI bus, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F for the byte count between zero and 96.

When transferring data from the SCSI bus to the host bus, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F and take the 2's complement to obtain the byte count between zero and 96.

2.3.3 Asynchronous SCSI Send –

1. Read the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers to determine if any bytes are left in the SCSI Output Data Latch (SODL) register. If bit 5 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SCSI Output Data Latch (SODL) register is full, respectively. Checking this bit also reveals bytes left in the SCSI Output Data Latch (SODL) register from a Chained Move operation with an odd byte count.

2.3.4 Synchronous SCSI Send –

1. Read bit 5 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers to determine if any bytes are left in the SCSI Output Data Latch (SODL) register. If bit 5 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SCSI Output Data Latch (SODL) register is full, respectively. Checking this bit also reveals bytes left in the SCSI Output Data Latch (SODL) register from a Chained Move operation with an odd byte count.
2. Read bit 6 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers to determine if any bytes are left in the SODR register. If bit 6 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SODR register is full, respectively.

2.3.5 Asynchronous SCSI Receive –

1. Read bit 7 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) register to determine if any bytes are left in the SCSI Input Data Latch (SIDL) register. If bit 7 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte is full, respectively.
2. If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCSI Control Register Two (SCNTL2), bit 0) to determine whether a byte is left in the SCSI Wide Residue Data (SWIDE) register.

2.3.6 Synchronous SCSI Receive –

1. Read the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers and examine bits [7:4], the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.
2. If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCSI Control Register Two (SCNTL2), bit 0) to determine whether a byte is left in the SCSI Wide Residue Data (SWIDE) register.

2.4 Host Interface

The LSI53C770 can be interfaced with both 680X0-type and 80X86-type host processors using big or little endian byte ordering, for a total of seven host bus interface modes. The modes are selected with the Bus Mode Select pins, defined in Chapter 3.

2.4.1 Misaligned Transfers

The LSI53C770 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such addresses are termed “misaligned.” An odd byte is defined as one in which the address contains A0 = 1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer and whether they occur at the start or end of the transfer. The LSI53C770 does not perform 24-bit transfers.

2.4.2 Transfer Size Throttling

The burst control logic in the LSI53C770 includes an optional throttling technique which does not allow a size change to occur within a bus ownership. When size throttling is enabled, a new bus ownership occurs each time the transfer changes size. When size throttling is enabled, bit 0 (Snoop Pins Mode) of the Chip Test Three (CTEST3) register should be clear. Size throttling can be enabled or disabled using the Size Throttle Enable bit, bit 7 in the DMA Control (DCNTL) register. Cache line bursting is controlled with the Cache Burst Disable bit, bit 7 in the Chip Test Zero (CTEST0) register.

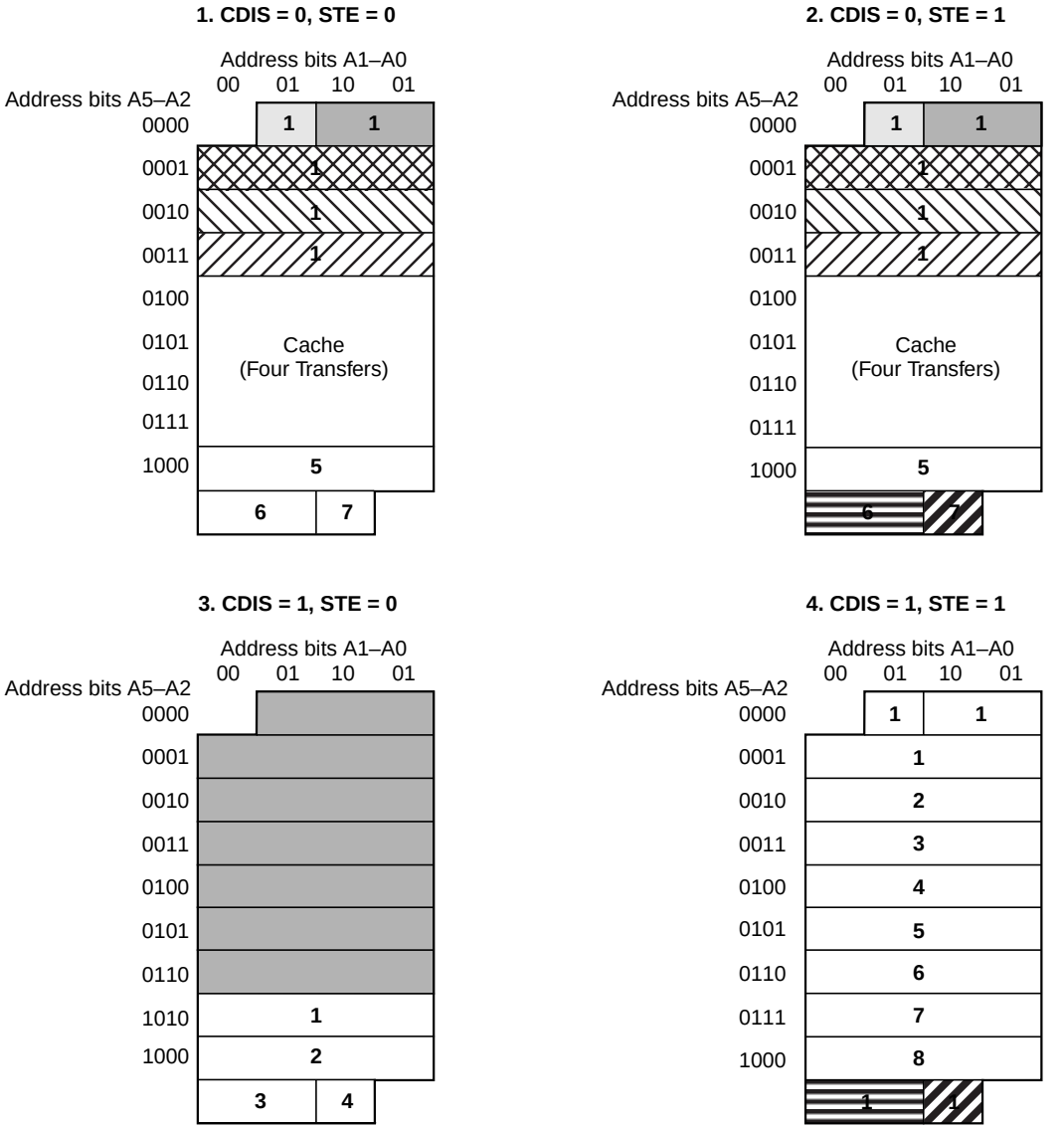
Figure 2.3 illustrates the function of the CDIS and STE bits. In Item 1, cache line bursting is enabled and size throttling is disabled. Since the starting address is at an odd byte boundary, the LSI53C770 lines up to a word boundary by performing a single byte transfer in a single bus ownership. Then, since the address is at an odd word boundary (bit A1 = 1), the LSI53C770 lines up to a Dword boundary by performing a single word transfer in a single bus ownership. At this point, one Dword transfer is performed per bus ownership until the address bits line up to a cache line boundary A(3) = A(2) = A(1) = A(0) = 0. Once aligned, the cache line, Dword, word, and byte are transferred in a single bus ownership to complete the transfer.

In Item 2, cache line bursting and size throttling are enabled. The LSI53C770 lines up to a cache line boundary as described for Figure 2.3. Once aligned, the cache line and Dword are transferred in the same bus ownership since the two are considered the same size. The remaining word and byte are transferred in two separate bus ownerships to complete the transfer.

In Item 3, cache line bursting and size throttling are disabled. The LSI53C770 completes eight transfers in one bus ownership, since the burst length is set to eight. The remaining four transfers are transferred in one bus ownership to complete the transfer.

In Item 4, cache line bursting is disabled and size throttling is enabled. The LSI53C770 lines up to a Dword boundary. Since the address starts on an odd byte boundary, the LSI53C770 lines up to a word boundary by performing a single byte transfer in a single bus ownership. Then, since the address is at an odd word boundary, the LSI53C770 lines up to a Dword boundary by performing a single word transfer in a single bus ownership. Once aligned, Dwords are transferred in the same bus ownership. The remaining word and byte are transferred in separate bus ownerships to complete the transfer.

Figure 2.3 Transfer Size Throttling



Note:

1. CDIS – Cache Burst Disable bit; STE = Size Throttle Enable bit.
2. At the start of the diagram, 38 bytes remain to be transferred.
3. The programmable burst length is 8.
4. Each of the shaded areas represents a new bus ownership.
5. The numbers within the shaded areas represent the number of transfers performed in the bus ownership.
6. For each alignment and bursting to be attempted, the entire transfer must be at least 31 bytes, this is dictated by chip architecture.

2.4.3 BERR/_TEA/ Pin Function

This section describes the function of the BERR/_TEA/ pin on the LSI53C770 SCSI I/O Processor.

2.4.4 Functionality of BERR/_TEA/ in Master Mode

In Master Mode, BERR/_TEA/ is used in conjunction with TA/ to indicate to the LSI53C770 that one of the following conditions has occurred:

TEA/	TA/	Condition[1]
1	1	Execute a wait-state
1	0	Normal cycle acknowledge
0	1	Bus error condition has occurred
0	0	Retry the current cycle after relinquishing the bus[2]

1. In Bus Mode 1, the chip attempts a bus retry operation only if BERR/ asserts in conjunction with HALT/.
2. In Bus Mode 2, the chip attempts a bus retry operation if TEA/ asserts in conjunction with TA/.

2.4.5 Functionality of BERR/_TEA/ in Slave Mode

In Slave Mode the LSI53C770 responds to requests from an external master in one of the following ways:

TEA/	SLACK/	TA/ [1]	Condition
1	1	1	Requests the bus master to insert a wait-state
1	0	0	Normal cycle acknowledge
0	1	1	Access exception has occurred
0	0	0	Reserved

1. TA/ does not assert during slave cycles unless the Enable Ack bit in the DMA Control (DCNTL) register is set.

Address exceptions are:

Bus Mode 1:	All of the cases mentioned above plus any 3 byte transfer.
Bus Mode 2:	• any misaligned 2-byte transfer (A0 = 1) • any misaligned Dword (A1–A0 not equal to 00) • any 2-byte transfer in big endian mode
Bus Mode 3 and 4:	No bus exceptions will occur and the TEA/ pin will never be asserted. One-, two-, three-, and four-byte operations are allowed.

2.4.6 Bus Retry

Bus Retry allows the LSI53C770 to retry the previous cycle using the same address, size, and other information. Bus retry occurs when an external device asserts the appropriate bus signals, forcing the chip to release the host bus. It tries to regain control of the host bus immediately, without a fairness delay. Once the chip regains control of the host bus, it retries the previous cycle.

2.4.7 Noncache Line Burst

In Bus Mode 1, an external device initiates a bus retry by asserting the HALT/ and BERR/ signals. In Bus Mode 2, the TA/ and TEA/ signals are used to initiate a bus retry. In Bus Modes 3 and 4, a bus retry is initiated by asserting the TEA/ and READYI/ signals. When an external device asserts these signals, the LSI53C770 asserts the Bus Request (BR/) signal (Bus Modes 1 and 2) or the HOLD/ signal (Bus Modes 3 and 4). This is done without a fairness delay to try to regain control of the host bus. This repeats indefinitely (as long as the signals remain asserted) until the cycle completes normally, or a bus error occurs. During a noncache line burst, a bus retry can be executed in any cycle.

2.4.8 Cache Line Burst

During a cache line burst, the bus retry must be executed during the first cycle for the Bus Retry to execute properly in all bus modes.

In Bus Mode 1, if the LSI53C770 is attempting a cache line burst, it will retry the bus cycle and assert Cache Burst Request (CBREQ/) again. If a bus retry is attempted during one of the subsequent cycles of the

cache line burst, the LSI53C770 halts the transfer until the HALT/ signal is deasserted. If the Bus Error (BERR/) signal is still asserted at this time, the transfer will abort.

In Bus Mode 2, if the LSI53C770 is attempting a cache line burst, it will retry the bus cycle and asserts SIZ0 and SIZ1 again. If a bus retry is attempted during one of the subsequent cycles of the cache line burst, the transfer will abort. If the Transfer Error (TEA/) signal is still asserted at this time, the LSI53C770 will abort the transfer.

In Bus Mode 4 (Bus Mode 3 does not support cache line bursting), if the LSI53C770 is attempting a cache line burst, it will retry the bus cycle and assert Cache Burst Request (CBREQ/) again. If a bus retry is attempted during one of the subsequent cycles of the cache line burst, the LSI53C770 will halt the transfer until the READYI/ signal is asserted. If the TEA/ signal is still asserted at this time, the LSI53C770 will abort the transfer.

If the BERR/ or TEA/ signal is asserted without HALT/, TA/, or READYI/, a Bus Fault interrupt will be generated, which sets bit 5 in the DMA Status (DSTAT) register (0x0C). The LSI53C770 will not automatically attempt to regain control of the host bus. A bus retry cannot be attempted during a Preview of Address (PA). For more information on the PA/ signal, refer to Chapter 3 and Chapter 4.

2.4.9 Using the Back Off Signal to Relinquish the Bus

The LSI53C770 may also relinquish the host bus when the Back Off (BOFF/) signal is asserted. For more information on the operation of this signal, refer to Chapter 3, “Signal Descriptions.” BOFF/ causes the LSI53C770 to release the bus and stay off in accordance with the timing data in Chapter 6, “Electrical Characteristics.” Because BOFF/ is sampled only at the beginning and end of each cycle, the LSI53C770 may get off the bus by executing a bus retry, then assert BOFF/ at the end of the cycle to prevent the chip from immediately trying to regain control of the bus. During a backoff or retry, register access functions normally. When the device resumes DMA operation, retried data is transferred.

2.5 Bidirectional STERM/-TA/-ReadyIn/

The STERM/_TA/_ReadyIn/ (referred to in this section as STERM/) signal terminates a read or write cycle. In a typical system, STERM/ is a wired-OR signal driven by slave devices and monitored by bus masters. When the master is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices that are faster than the master present a special problem in that they are required to insert wait-states to allow the master to catch up. The LSI53C770 can accommodate both situations.

During slave accesses, the SLACK/-ReadyO/ (Referred to as SLACK/) output provides an indication that the LSI53C770 is ready to terminate a read or write cycle. After asserting SLACK/, the LSI53C770 samples STERM/ on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle terminates. Any time between SLACK/ and STERM/ is treated as a wait-state; a read/write cycle may be stretched indefinitely. However on a write cycle, data is taken into the LSI53C770 before the SLACK/ signal is asserted. Wait states may not be added to allow for late write data.

Typically, SLACK/ is tied back to STERM/ as in Figure 2.4. If the system CPU is not capable of completing a slave cycle in the minimum time required by the LSI53C770, SLACK/ must be delayed before asserting STERM/. If the system CPU is capable of running slave write cycles with zero additional wait-states, no delay is necessary.

In systems where the CPU is faster than the LSI53C770, SLACK/ may be connected to STERM/ with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DMA Control (DCNTL) register to internally connect SLACK/ to STERM. When the EA bit is set, the STERM/ pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing for zero wait-state operation is guaranteed. Setting the EA bit must be the first slave I/O access to the LSI53C770. In addition, when the Enable Acknowledge bit is set, a signal with the same timing characteristics as SLACK/ is driven onto the STERM/_TA/ pin, as illustrated in Figure 2.4. The external timing on this signal is the same as the signal generated if

EA was not used, as illustrated in Figure 2.5. The additional control logic 3-states STERM/_TA/ for 5 ns after it is deasserted. The SLACK/ signal is always driven.

Figure 2.4 SLACK/ Tied Back to STERM/, EA Bit Not Set

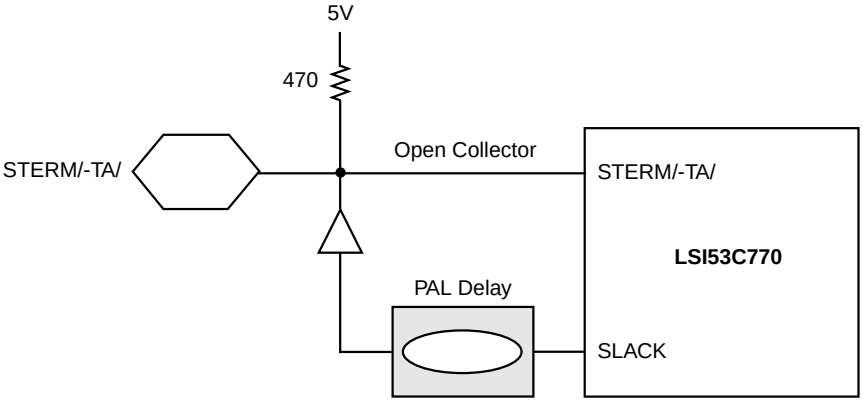
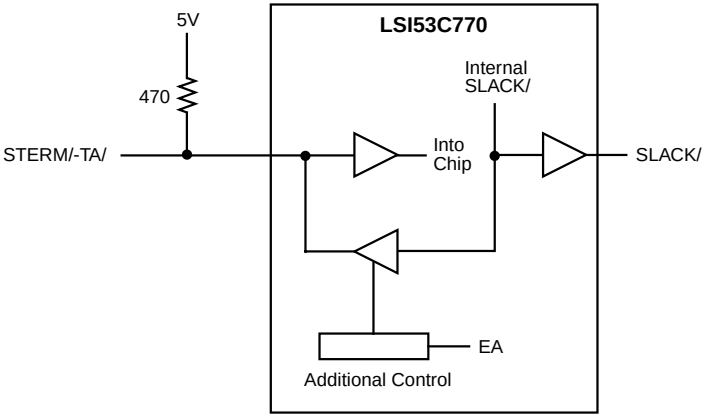


Figure 2.5 Bidirectional STERM/, EA Bit Set



2.6 SCSI Bus Interface

The LSI53C770 contains open drain output drivers that can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down LSI53C770 has no effect on an active SCSI bus (CMOS “voltage feed-through”). Additionally, TolerANT technology provides signal filtering at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In differential mode, the SDIR [15:0], SDIRP [1:0], IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential pair transceivers. See Figure 2.6 for the suggested differential wiring diagram. The suggested value for the 15 pull-up resistors in the diagram is 1.5 K. The pull-up value should be no lower than the transceiver I_{OL} can tolerate, but not so high as to cause RC timing problems.

2.6.1 SCSI Termination

SCSI terminators provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both SE and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than two sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed. SE cables are terminated differently from differential cables. SE cables use a 220 Ω pull-up to the termination power supply (Term-Power) line and a 330 Ω pull-down to ground. Differential cables use a 330 Ω pull-up from “– SIG” to Term-Power, a 330 Ω pull-down from “+ SIG” to ground, and a 150 Ω resistor from “– SIG” to “+ SIG”.

Because of the high-performance nature of the LSI53C770, Regulated (or Active) termination is recommended. Figure 2.7 shows a Unitrode active terminator. For additional information, refer to the SCSI-2 Specification. TolerANT technology active negation can be used with any type of termination.

Note: If the LSI53C770 is used in a design with a 8-bit SCSI bus, all 16 data lines must be terminated or pulled HIGH.

Note: Active termination is required in SE Ultra SCSI systems.

Figure 2.6 LSI53C770 Differential Wiring Diagram

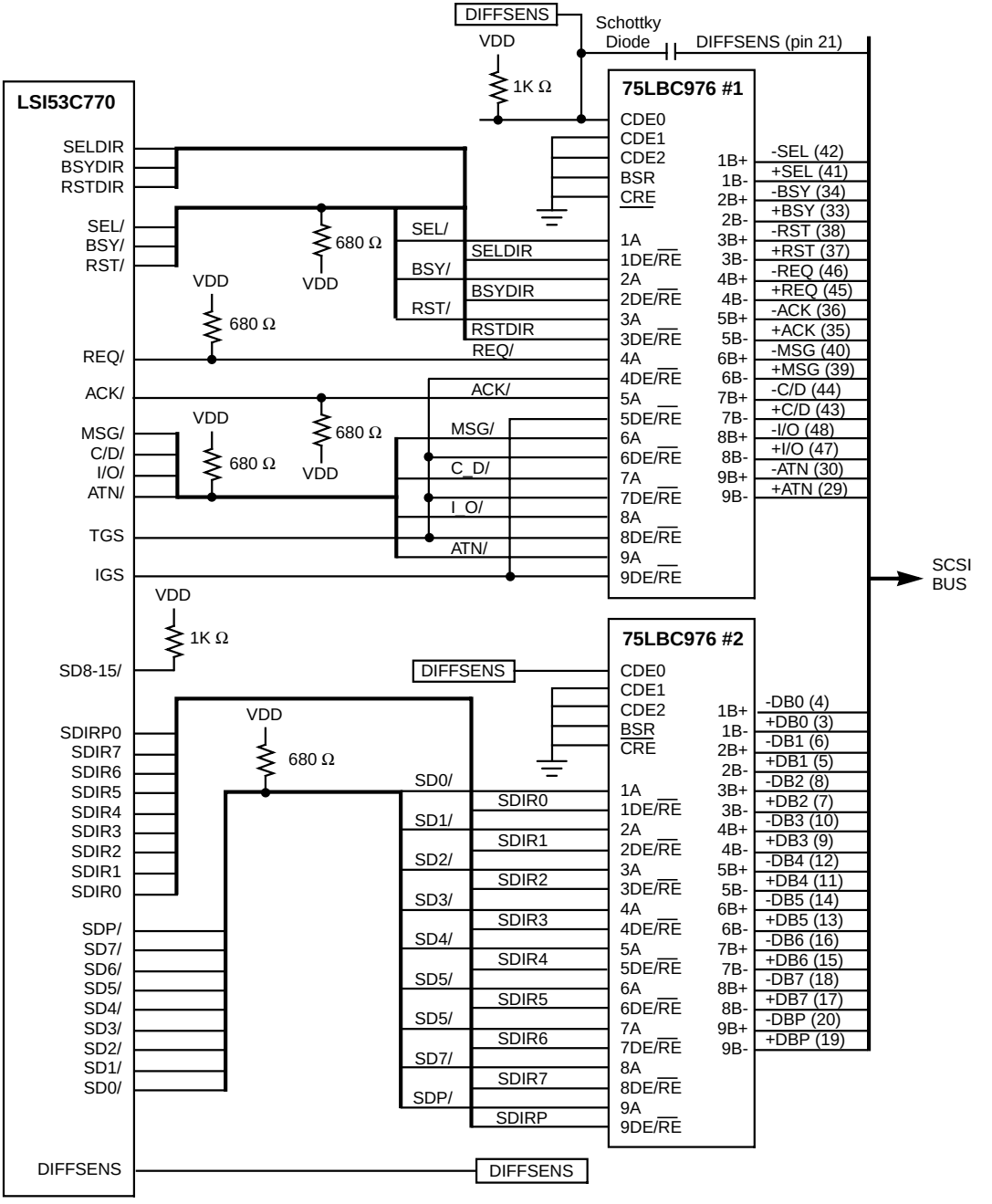
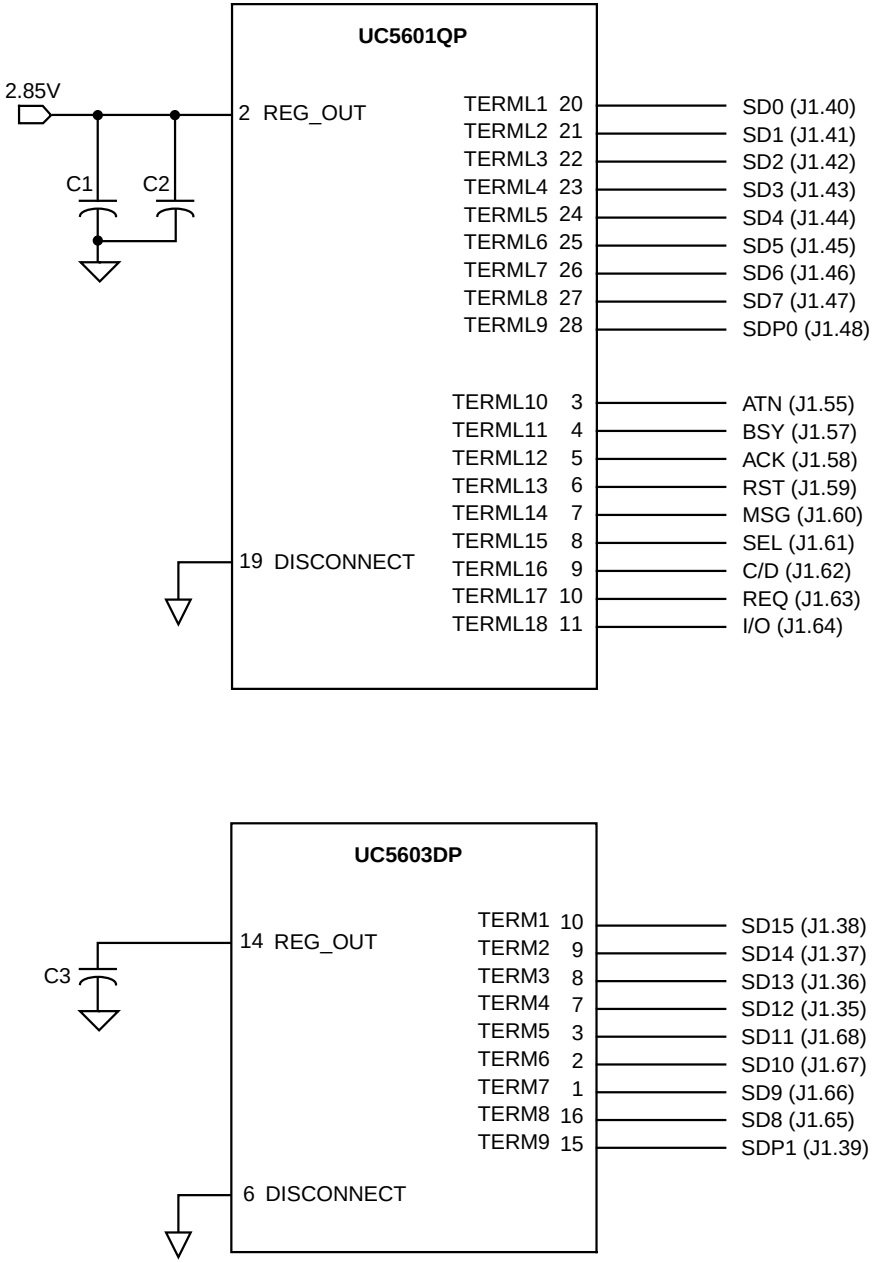


Figure 2.7 Regulated Termination



2.6.2 Select/Reselect During Selection/Reselection

In multithreaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in the initiator mode) tries to select one target and gets reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection. The SCSI SCRIPTS language allows interrupt free handling of multithreaded operations.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a Set Initiator instruction or the target SCRIPTS should start with a Set Target instruction. The Enable Response to Selection and Enable Response to Reselection bits (SCSI Chip ID (SCID) bits 5 and 6, respectively) should both be asserted so that the LSI53C770 may respond as an initiator or as a target.

The selection or reselection enable bits allow the LSI53C770 to respond as either a target or an initiator. For example, if only selection is enabled, the LSI53C770 cannot be reselected as an initiator. There are also interrupt status and interrupt enable bits in the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Enable Zero (SIEN0) registers respectively, indicating if the LSI53C770 has been selected (bit 5) or reselected (bit 4).

2.6.3 Synchronous Operation

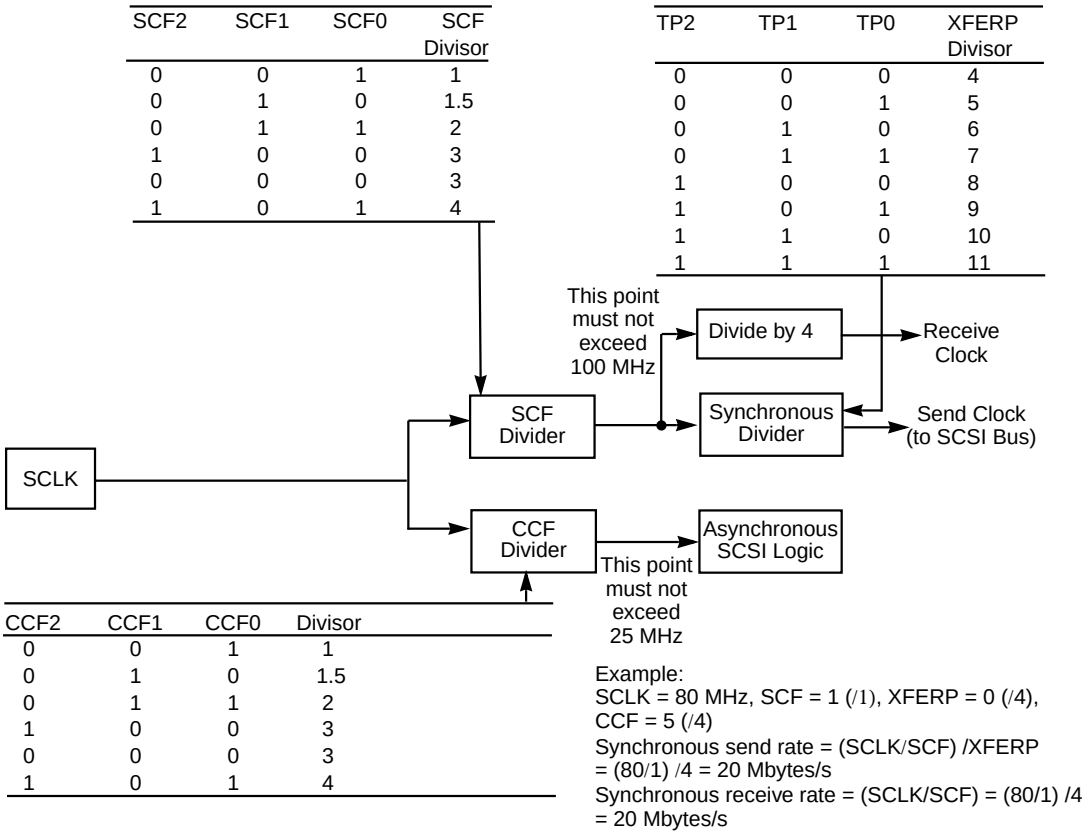
The LSI53C770 transfers synchronous SCSI data in both initiator and target modes. The SCSI Transfer (SXFER) register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPTS execution begins or from within a SCRIPTS program. The LSI53C770 can always receive data from the SCSI bus at a synchronous transfer period as short as 160 ns for SCSI-1 or 80 ns for SCSI-2, regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 80 or 160 ns. Depending on the SCLK frequency and the synchronous clock divider, the LSI53C770 can send synchronous data at intervals as short as 100 or 200 ns.

2.6.4 Determining the Data Transfer Rate

This section is an overview of how the LSI53C770 controls synchronous data transfers. For more information, refer to the full bit descriptions in Chapter 4. Synchronous data transfer rates are controlled by bits in two different registers of the LSI53C770. A brief description of the bits is provided below.

Figure 2.8 illustrates the clock division factors used in each register, and the role of the register bits in determining the transfer rate.

Figure 2.8 Determining the Synchronous Transfer Rate



Example:
SCLK = 80 MHz, SCF = 1 (/1), XFERP = 0 (/4), CCF = 5 (/4)
Synchronous send rate = (SCLK/SCF) /XFERP = (80/1) /4 = 20 Mbytes/s
Synchronous receive rate = (SCLK/SCF) = (80/1) /4 = 20 Mbytes/s

2.6.4.1 SCSI Control Three (SCNTL3) Register, Bits [6:4] (SCF[2:0])

The SCF[2:0] bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider must not exceed 80 MHz. The receive rate is one-fourth of the divider output. For example, if SCLK is 80 MHz and the SCF value is set to divide by two, then the maximum rate at which data can be received is 10 MHz (80/2)/4 = 10.

2.6.4.2 SCNTL3 Register, Bits [2:0] (CCF[2:0])

The CCF[2:0] bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI core logic. This divider must be set according to the input clock frequency in the table.

2.6.4.3 SXFER Register, Bits [7:5] (TP[2:0])

The TP[2:0] bits determine the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode.

2.6.5 Ultra SCSI Synchronous Data Transfers

Ultra SCSI is simply an extension of current Fast SCSI-2 synchronous transfer specifications. It allows synchronous transfer periods to be negotiated to as low as 50 ns, which is half the 100 ns period allowed under Fast SCSI-2. This will allow a maximum transfer rate of 40 Mbytes/s on a 16-bit SCSI bus. The LSI53C770 requires an 80 MHz SCSI clock input to perform Ultra SCSI transfers. In addition, the following bit values affect the chip's ability to support Ultra SCSI synchronous transfer rates:

- Clock Conversion Factor bits, SCSI Control Three (SCNTL3) register, bits [2:0] and Synchronous Clock Conversion Factor bits, SCSI Control Three (SCNTL3) register, bits [6:4].

  These fields support a value of 101 (binary), allowing the SCLK frequency to be divided down by 4. This allows systems using an 80/100 MHz clock or the internal clock doubler (clock doubler works at 40 to 50 MHz input), to operate at Fast SCSI-2 transfer rates as well as Ultra SCSI rates, if needed.

- Ultra Enable bit, SCSI Control Three (SCNTL3) register, bit 7.

  Setting this bit enables Ultra SCSI synchronous transfers in systems that have an 80 MHz clock or that use the SCSI clock doubler.

2.7 Interrupt Handling

The SCRIPTS processor in the LSI53C770 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the LSI53C770.

2.7.1 Polling vs. Hardware Interrupts

The external microprocessor is informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit that is set indicating an interrupt. This method is the fastest, but it wastes CPU time that could be used for other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the LSI53C770 asserts the Interrupt Request (IRQ/) line that interrupts the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware for long waits, and use polling for short waits.

2.7.2 Registers

The registers in the LSI53C770 that are used for detecting or defining interrupts are the Interrupt Status (ISTAT), SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), DMA Status (DSTAT), SCSI Interrupt Enable Zero (SIEN0), SCSI Interrupt Enable One (SIEN1), and DMA Interrupt Enable (DIEN).

ISTAT – Interrupt Status (ISTAT) is the only register that can be accessed as a slave during SCRIPTS operation. Therefore, it is the register that is polled when polled interrupts are used. It is also the first register that should be read after the IRQ/ pin is asserted in association with a hardware interrupt. The INTF (Interrupt-on-the-Fly) bit should be the first interrupt serviced. To service this interrupt, write a one to the INTF bit. If the SIP bit in the Interrupt Status (ISTAT) register is set, then a SCSI-type interrupt has occurred and the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers should be read. If the DIP bit in the Interrupt Status (ISTAT) register is set, then a

DMA-type interrupt has occurred and the DMA Status (DSTAT) register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

SIST0 and SIST1 – The SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers contain the SCSI-type interrupt bits. Reading these registers determines which condition or conditions caused the SCSI-type interrupt, and clears that SCSI interrupt condition. If the LSI53C770 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the chip attempts to send the contents of the DMA FIFO to memory before generating the interrupt. If the LSI53C770 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DMA FIFO Empty (DFE) bit in DMA Status (DSTAT) should be checked. If this bit is cleared, set the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits before continuing.

DSTAT – The DMA Status (DSTAT) register contains the DMA-type interrupt bits. Reading this register determines which condition or conditions caused the DMA-type interrupt, and clears that DMA interrupt condition. Bit 7 in DMA Status (DSTAT), DFE, is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts flush neither the DMA nor SCSI FIFO before generating the interrupt, so the DFE bit in the DMA Status (DSTAT) register should be checked after any DMA interrupt. If the DFE bit is cleared, then the FIFOs must be cleared by setting the CLF and CSF bits, or flushed by setting the FLF (Flush DMA FIFO) bit. The CLF bit is bit 2 in Chip Test Three (CTEST3). The FLF bit is bit 3 in Chip Test Three (CTEST3). The CSF bit is bit 1 in SCSI Test Register Three (STEST3).

SIEN0 and SIEN1 – The SCSI Interrupt Enable Zero (SIEN0) and SCSI Interrupt Enable One (SIEN1) registers are the interrupt enable registers for the SCSI interrupts in SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1).

DIEN – The DMA Interrupt Enable (DIEN) register is the interrupt enable register for DMA interrupts in DMA Status (DSTAT).

2.7.3 Fatal vs. Nonfatal Interrupts

A fatal interrupt, as the name implies, always causes the SCRIPTS to stop running. A nonfatal interrupt causes the SCRIPTS to stop running only if the interrupt is enabled. Interrupt enabling and masking are discussed later in this section.

All DMA interrupts (indicated by the DIP bit in Interrupt Status (ISTAT) and one or more bits in DMA Status (DSTAT) being set) are fatal. Some SCSI interrupts (indicated by the SIP bit in the Interrupt Status (ISTAT) and one or more bits in SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) being set) are nonfatal. When the LSI53C770 is operating in the Initiator mode, only the CMP (Function Complete) and SEL (Selected or Reselected) interrupts are nonfatal.

When operating in Target mode CMP, SEL, and M/A (Target mode: ATN/ active) are nonfatal. Refer to the description for the DHP (Disable Halt on a Parity Error or ATN/ active (Target Mode Only)) bit in the SCSI Control One (SCNTL1) register to configure the chip's behavior when the ATN/ interrupt is enabled during Target mode operation. The Interrupt-on-the-Fly interrupt is also nonfatal, since SCRIPTS can continue when it occurs.

The reason for nonfatal interrupts is to prevent the SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the LSI53C770 is selected or reselected (SEL set), when there is a general purpose or handshake to handshake time-out, or when the initiator has asserted ATN (target mode: ATN/ active). These interrupts are not needed for events that occur during high-level SCRIPTS operation.

2.7.4 Enabling Interrupts

In the LSI53C770, the SCSI and DMA Interrupt Enable registers (SIEN and DIEN) are used to enable the various interrupting conditions. The default value of these registers is to disable, or mask, all interrupts. Masking an interrupt means ignoring that interrupt. To mask any of these interrupts, clear the appropriate bits in the SIEN (for SCSI interrupts) registers or DIEN (for DMA interrupts) registers. How the chip responds

to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or nonfatal; and whether the chip is operating in Initiator or Target mode.

If a nonfatal interrupt is masked and that condition occurs, the SCRIPTS do not stop, the appropriate bit in the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) is still set, the SIP bit in the Interrupt Status (ISTAT) is not set, and the IRQ/ pin is not asserted. See the Section 2.7.3, “Fatal vs. Nonfatal Interrupts,” for a list of the nonfatal interrupts.

If a fatal interrupt is masked and that condition occurs, then the SCRIPTS still stops, the appropriate bit in the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), or SCSI Interrupt Status One (SIST1) register is set, the SIP or DIP bits in the Interrupt Status (ISTAT) is set, but the IRQ/ pin is not asserted. When the chip is initialized, enable all fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, the SCRIPTS halts and the system will never know it unless it times out and checks the Interrupt Status (ISTAT) after a certain period of inactivity.

If you are polling the Interrupt Status (ISTAT) instead of using hardware interrupts, then masking a fatal interrupt makes no difference since the SIP and DIP bits in the Interrupt Status (ISTAT) inform the system of interrupts, not the IRQ/ pin. Masking an interrupt after IRQ/ is asserted does not cause deassertion of IRQ/.

2.7.5 Stacked Interrupts

The LSI53C770 will stack interrupts if they occur one after the other. If the SIP or DIP bits in the Interrupt Status (ISTAT) register are set (first level), then there is already at least one pending interrupt, and any future interrupts are stacked in extra registers behind the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts set additional bits in the extra registers behind SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT). When the first level of interrupts are cleared, all the interrupts that came in afterward move into the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT). After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin is

deasserted for a set time as published in Chapter 6; the stacked interrupt(s) move into the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), or DMA Status (DSTAT); and the IRQ/ pin is asserted once again.

Since a masked nonfatal interrupt does not set the SIP or DIP bits, interrupt stacking does not occur as a result of a masked, nonfatal interrupt. A masked, nonfatal interrupt still posts the interrupt in SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1), but does not assert the IRQ/ pin. Since no interrupt is generated, future interrupts move into the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked nonfatal interrupt is still set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but are not stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or a combination of SCSI and DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts do not attempt to flush the FIFOs before generating the interrupt. It is important to set either the CLF (Clear DMA) or CSF (SCSI FIFO) bit if a DMA interrupt occurs and the DFE (DMA FIFO Empty) bit is not set. This is because any future SCSI interrupts are not posted until the DMA FIFO is clear of data. These ‘locked out’ SCSI interrupts are posted as soon as the DMA FIFO is empty.

2.7.6 Halting in an Orderly Fashion

When an interrupt occurs, the LSI53C770 attempts to halt in an orderly fashion. All instructions may halt before completion, except for the ones described below.

- If an interrupt occurs in the middle of an instruction fetch, the fetch is completed, except in the case of a Bus Fault or Watchdog Time-out. Execution does not begin, but the DMA SCRIPTS Pointer (DSP) points to the next instruction since it is updated when the current SCRIPTS routine is fetched.

- If the DMA direction is a write to memory and a SCSI interrupt occurs, the LSI53C770 attempts to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle is completed before halting, so the DFE bit in DMA Status (DSTAT) should be checked to see if any data remains in the DMA FIFO.
- SCSI REQ/ACK handshakes that have begun are completed before halting.
- The LSI53C770 attempts to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it continues to completion before halting.
- If the instruction is a JUMP/CALL WHEN <phase>, the DMA SCRIPTS Pointer (DSP) is updated to the transfer address before halting.

2.7.7 Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the LSI53C770. It can be repeated during if polling or should be called when the IRQ/ pin is asserted during hardware interrupts.

1. Read Interrupt Status (ISTAT).
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) tell which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).
4. If only the DIP bit is set, read the DMA Status (DSTAT) to clear the interrupt condition and get the DMA interrupt status. The bits in DMA Status (DSTAT) tells which DMA interrupts occurred and determine what action is required to service the interrupts.
5. If both the SIP and DIP bits are set, read SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) registers to clear interrupts, insert 12 BCLKs between the

consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the interrupt service routine. It is recommended that the DMA interrupt is serviced before the SCSI interrupt, because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.

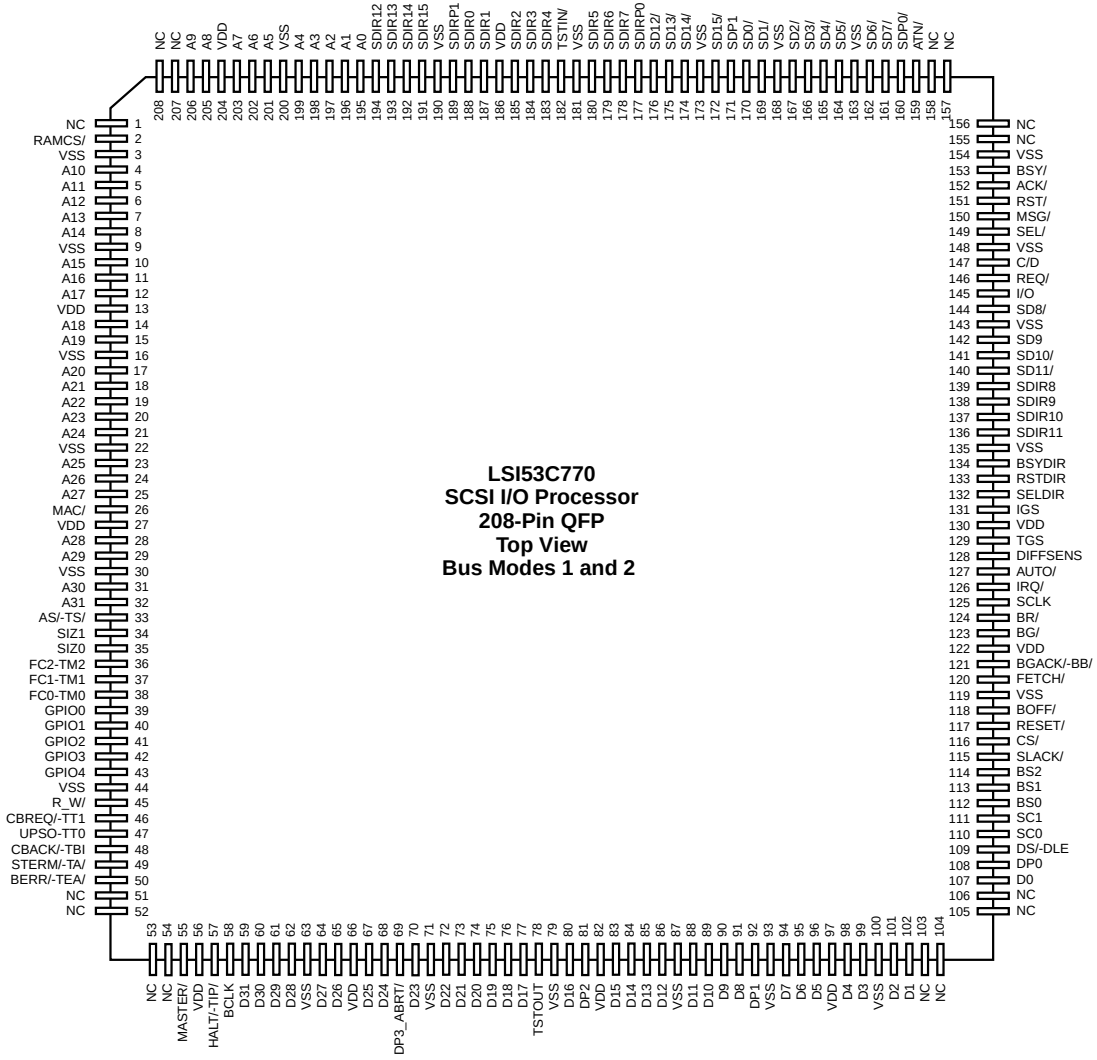
6. When using polled interrupts, go back to Step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin is asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

Chapter 3
Signal Descriptions

The LSI53C770 host bus can operate in one of four modes: Bus Mode 1 (68030-like), Bus Mode 2 (68040-like), Bus Mode 3 (80386SX-like), and Bus Mode 4 (80386DX-like). Both big and little endian byte ordering are supported in Bus Modes 1, 2, and 4. The bus mode is selected by using the BS[2:0] pins. A function is listed on the table as NC (not connected) if it is not active for a given bus mode. A slash (/) indicates an active LOW signal. All pins have a totem pole (push-pull) architecture unless otherwise noted.

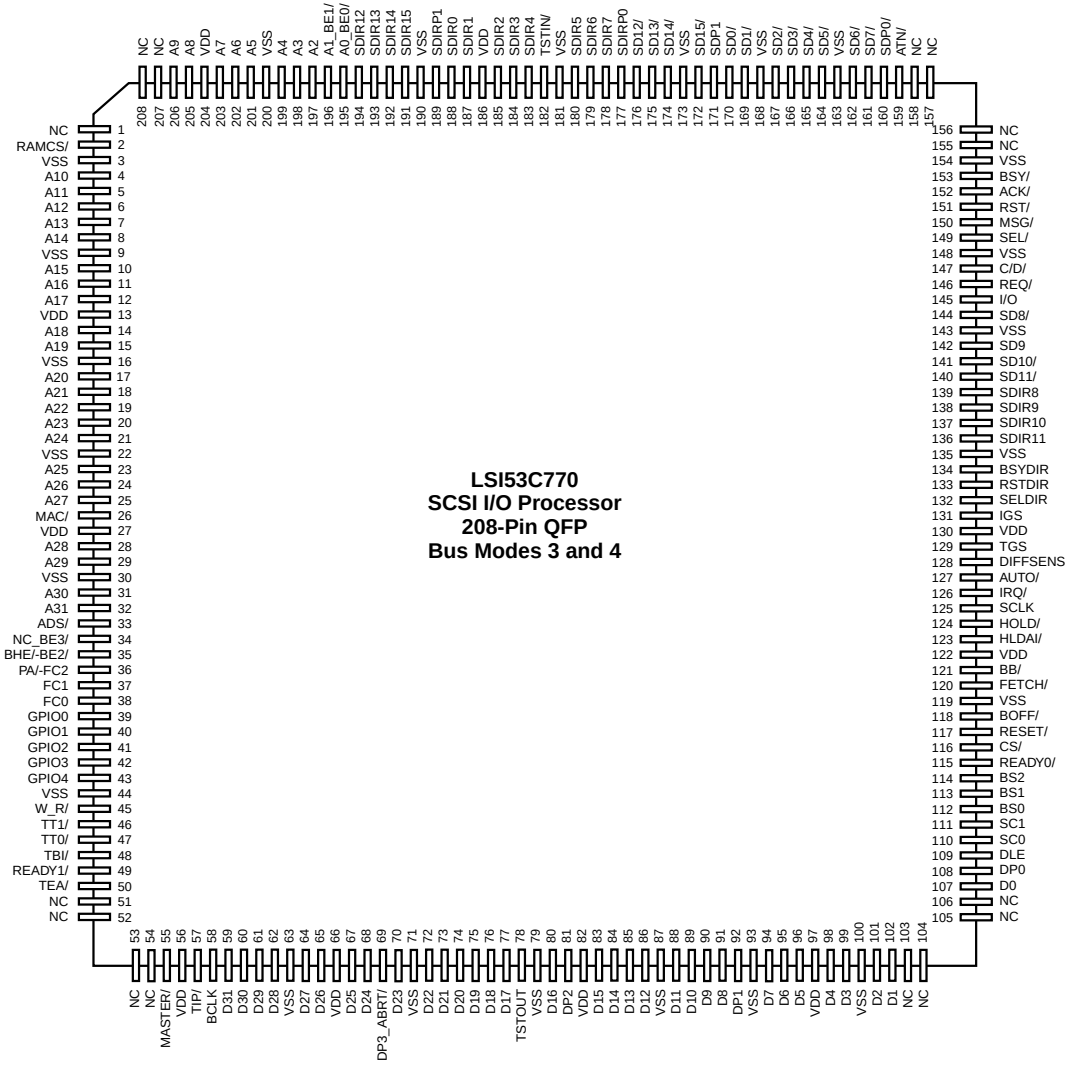
Figure 3.1 illustrates the LSI53C770 pin diagram for Bus Modes 1 and 2. Figure 3.2 illustrates the LSI53C770 pin diagram for Bus Modes 3 and 4.

Figure 3.1 LSI53C770 Pin Diagram, Bus Modes 1 and 2



Note: NC pins are not connected.

Figure 3.2 LSI53C770 Pin Diagram, Bus Modes 3 and 4



Note: The decoupling capacitor arrangements shown above are recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the LSI53C770, a multilayer PC board with power and ground planes is required.

Table 3.1 describes the Power and Ground Signals group.

Table 3.1 Power and Ground Signals

Symbol	Pin No.	Description
V_{SS}	3, 9, 16, 22, 30, 44, 63, 71, 79, 87, 93, 100, 119, 135, 143, 148, 154, 163, 168, 173, 181, 190, 200	–
V_{DD}	13, 27, 56, 66, 82, 97, 122, 130, 186, 204	–

Table 3.2 describes the Address and Data Signals group.

Table 3.2 Address and Data Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
D[31:0]	D[31:0]	D[31:0]	D[31:0]	59–62, 64–65, 67–68, 70, 72–77, 80, 83–86, 88–91, 94–96, 98, 99, 101, 102, 107	**Host Data Bus** (I/O, I/O). Main data path into host memory for all bus modes. Note: To interface to a 16-bit bus, Bit 3 in the DMA Control (DCNTL) register should be set and data lines 31 through 16 should be tied to data lines 15 through 0, respectively.
DP[2:0]	DP[2:0]	DP[2:0]	DP[2:0]	81, 92, 108	**Host Bus Data Parity** (I/O, I/O). In all bus modes: DP0 provides parity for D[7:0] DP1 provides parity for D[15:8] DP2 provides parity for D[23:16] Note: To interface to a 16-bit bus and to support parity, DP3 and DP2 should be tied to DP1 and DP0, respectively.
DP3_ Abort/	DP3_ Abort/	DP3_ Abort/	DP3_ Abort/	69	**Host Bus Data Parity** (I/O, I/O). In all bus modes, DP3 provides parity for D[31:24]. Parity is valid on all byte lanes, including unused lanes. To disable Parity Through mode, set bit 2 in the SCSI Control Zero (SCNTL0) register. DP3 becomes a hardware abort input (ABRT/) when Parity Through mode is disabled. When Abort/ is asserted, the LSI53C770 finishes the current transfer, then gets off the bus. An abort leaves data in an undetermined state and does not flush the FIFOs.

Table 3.2 Address and Data Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
DS/	DLE	DLE	DLE	109	**Data Strobe** (Z, O). In Bus Mode 1, this signal indicates that valid data has been or should be placed on the data lines. It is typically used when data becomes valid asynchronously to the clock. DLE—*Data Latch* Enable (I, I) In Bus Modes 2, 3, and 4, this signal transparently latches read data into the LSI53C770 prior to an Acknowledge. It is typically used when data becomes valid asynchronously to the clock. Tie this signal HIGH if it is not used.
A[31:2]	A[31:2]	A[31:2]	A[31:2]	32, 31, 29, 28, 25–23, 21–17, 15, 14, 12–10, 8–4, 206, 205, 203–201, 199–195	**Address Bus** (I, O). In all bus modes, this signal provides an address bus to the host memory.
A[1:0]	A[1:0]	A[1:0]	BE/[1:0]	196, 1950	**A[1:0]**. In Bus Modes 1, 2, and 3, these pins are part of the address bus. **BE/[1:0].** In Bus Mode 4, this signal enables data transfer on the byte lane D[15:8] and D[7:0].
AS/	TS/	ADS/	ADS/	33	**Address Strobe** (I, O). In Bus Mode 1, this signal indicates that a valid address is on A[31:0]. **Transfer Start** (I, O). In Bus Mode 2, Transfer Start indicates that a bus cycle is starting and all of the status and address lines are valid. **Address Status** (I, O). In Bus Modes 3 and 4, this signal indicates that a valid bus cycle definition and address are being driven.

Table 3.3 describes the Arbitration Signals group.

Table 3.3 Arbitration Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
BR/	BR/	HOLD/	HOLD/	124	**Bus Request** (O, O). In Bus Modes 1 and 2, this signal indicates there is a request to use the host bus. **Hold** (O, O). In Bus Modes 3 and 4, this signal indicates there is a request to use the host bus.
BG/	BG/	HLDAI/	HLDAI/	123	**Bus Grant** (I, I). In Bus Modes 1 and 2, this signal indicates that the host bus has been granted to the LSI53C770. **Hold Acknowledge** (I, I). In Bus Modes 3 and 4, this signal indicates that the previous bus master has given up use of the host bus.
BGACK/	BB/	BB/	BB/	121	**Bus Grant Acknowledge** (Z, I/O). In Bus Mode 1, this signal indicates that the LSI53C770 or another device has taken control of the host signals. **Bus Busy** (wire-OR) (Z, I/O). In Bus Modes 2, 3, and 4, this signal indicates that the LSI53C770 or another device has taken control of the host bus signals.
BOFF/	BOFF/	BOFF/	BOFF/	118	**Back Off** (I, I). In all bus modes, this forces the LSI53C770 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF/ deasserts, a new arbitration takes place and the cycles resume. BOFF/ is sampled at every start cycle. During worst case operation, if timing is not met it takes the LSI53C770 two clocks to get off the host bus. The start cycle becomes a release cycle. If BOFF/ asserts during arbitration, the LSI53C770 completes arbitration and gets off the bus at the first start cycle.

Table 3.4 describes the System Signals group.

Table 3.4 System Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
BCLK	BCLK	BCLK	BCLK	58	**Bus Clock** (I, I). This clock controls all host related activity in all bus modes.
RESET/	RESET/	RESET/	RESET/	117	**Chip Reset** (I, I). Forces a full chip reset in all bus modes.
CS/	CS/	CS/	CS/	116	**Chip Select** (I, I). Selects the LSI53C770 as a slave I/O device in all bus modes. When CS/ is detected: Bus Mode 1—CBACK/ is deasserted Bus Modes 2, 3, 4—TBI/ is asserted
RAMCS/	RAMCS/	RAMCS/	RAMCS/	2	**SCRIPTS RAM Chip Select** (I, I). When enabled, defines a 4K byte address space for the 4K bytes SCRIPTS RAM. This type of SCRIPTS RAM access is enabled by setting bits 1 and 2 of the Chip Test Five (CTEST5) register.
IRQ/	IRQ/	IRQ/	IRQ/	126	**Interrupt** (O, O). In all bus modes, this signal indicates that service is required from the host CPU.
UPSO	TT0/	TT0/	TT0/	47	**User Programmable Status** (Z, O). General purpose line in Bus Mode 1. The value in the register bit is asserted while the chip is bus master. **Transfer Type Zero** (Z, O). In Bus Modes 2, 3, and 4 this signal indicates the current bus transfer type. This pin can be programmed from a register bit (default = 0). It is asserted only when the LSI53C770 is bus master.
SIZ0	SIZ0	BHE/	BE2/	35	**Transfer Size Zero** (I, O). In Bus Modes 1 and 2, SIZ0 indicates the current transfer size in combination with SIZ1 (see table under the SIZ1 pin description). **Byte High Enable** (I, O). In Bus Mode 3, this signal enables data transfer on the high order byte lane D[15:8]. **Byte Enable Two** (I, O). In Bus Mode 4, this signal enables data transfer on byte lane D[23:16].

Table 3.4 System Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
SIZ1	SIZ1	NC	BE3/	34	**Transfer Size One** (I, O). In Bus Modes 1 and 2, SIZ1 indicates the current transfer size in combination with the SIZ0 pin, as shown in the table below: **SIZ1, SIZ0** 0,0 Dword (4 bytes) 0,1 Byte (1 byte) 1,0 Word (2-byte slave accesses are allowed, if word-aligned) 1,1 Bus Mode 1, Illegal; Bus Mode 2, Cache Line Burst (since cache line bursts are not supported in slave mode, this size request will result in standard Dword slave access). **Byte Enable Three** (I, O). In Bus Mode 4, this signal enables data transfer on byte lane D[31:24].
STERM/	TA/	READYI/	READYI/	49	**Synchronous Cycle Termination** (I/O, I). In Bus Mode 1, this signal acknowledges transfer to a 32-bit wide port. **Transfer Acknowledge** (I/O, I). In Bus Mode 2, this signal acknowledges transfer to a 32-bit wide port. **Ready In** (I, I). In Bus Modes 3 and 4 during master mode operation, this signal indicates that the slave device is ready to transfer or receive data. During slave mode, this signal is monitored by the LSI53C770 to determine when to stop driving the bus.

Table 3.5 describes the Interface Control Signals group.

Table 3.5 Interface Control Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
R_W/	R_W/	W_R/	W_R/	45	**Read/Write** (I, O). Indicates the current direction of the data transfer relative to the current master.
SLACK/	SLACK/	READYO/	READYO/	115	**Slave Acknowledge** (O, O). Asserted in Bus Modes 1 and 2 to indicate the internal end of a valid slave mode cycle. The external slave cycle ends when the LSI53C770 observes either STERM/-TA/ or BERR/-TEA. **Ready Out** (O, O). Asserted in Bus Modes 3 and 4 to indicate the end of a slave mode cycle.
FC2_PA/	TM2	FC2_PA/	FC2_PA/	36	**Function Codes/Preview of Address, Transfer Modifier.** **FC2, TM2** (Z, O). User definable from bit 5 in the DMA Mode (DMODE) register in conjunction with the Bus Mode bit (bit 6) in the DMA Control (DCNTL) register. **PA/** (I, I). This input signal is used to tell the LSI53C770/SE that the system is ready for the next address/value and byte enable signal. FC2 becomes PA/ when the Bus Mode bit (DMA Control (DCNTL), bit 6) is set.
FC[1:0]	TM[1:0]	FC[1:0]	FC[1:0]	37–38	**Function Codes and Transfer Modifiers.** For all bus modes: **FC0–TM0** (Z, O). Indicates the status of the current bus cycle. For more information on the operation of this pin, refer to description of the the Program Data bit (DMA Mode (DMODE), bit 3) in Chapter 4. **FC(1)–TM(1)** (Z, O). User definable from bit 4 in the DMA Mode (DMODE) register in conjunction with bit 6 in the DMA Control (DCNTL) register. For more information, refer to the description of the Function Code 1 bit (DMA Mode (DMODE), bit 4) in Chapter 4.

Table 3.5 Interface Control Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
SC[1:0]	SC[1:0]	SC[1:0]	SC[1:0]	111–110	**Snoop Control** (Z(O), O). Indicates the bus snooping level in all bus modes. The bits are user programmable through register bits. They are asserted when the LSI53C770 is bus master. SC[1:0] may be optionally used as pure outputs, active in both master and slave modes.
MASTER/	MASTER/	MASTER/	MASTER/	55	**Master Status** (O, O). Driven LOW when the LSI53C770 becomes bus master. This signal is valid in all bus modes. This signal is driven at all times except when the LSI53C770 is in ZMODE.
FETCH/	FETCH/	FETCH/	FETCH/	120	**Fetching OpCode** (O, O). In all bus modes, this signal indicates that the next bus request will be for an opcode fetch.
CBREQ/	TT1/	TT1/	CBREQ/	46	**Cache Burst Request** (Z, O). In Bus Modes 1 and 4, Cache Burst Request indicates an attempt to execute a line transfer of four Dwords. CBREQ/ is valid in Mode 4 only when 386 Cache Mode is enabled (Cache 386 bit, Chip Test Zero (CTEST0) register). **Transfer Type Bit One** (Z, O). Transfer Type bit one is a 3-state output line indicating the current bus transfer type in all four bus modes. TT1/ is not valid in Bus Mode 4 if Cache 386 mode is enabled. This bit can be programmed from bit 1 in the Chip Test Zero (CTEST0) register. It is only asserted when the LSI53C770 is bus master.
CBACK/	TBI/	TBI/	TBI/	48	**Cache Burst Acknowledge** (O, I). In Bus Mode 1 this signal indicates that the memory system or LSI53C770 can handle a burst request. In slave mode this signal is deasserted in response to CS/. **Transfer Burst Inhibit** (O, I). In Bus Modes 2, 3, and 4 Transfer Burst Inhibit indicates that the memory or the LSI53C770 cannot handle a burst request at this time. In slave mode this signal is asserted in response to CS/.

Table 3.5 Interface Control Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
BS[2:0]	BS[2:0]	BS[2:0]	BS[2:0]	114–112	**Bus Mode Select** (I, I) These signals are active in all four bus modes. They select between Motorola/Intel (BS2), Big/Little Endian (BS1), and 386SX/_030 and 386DX/_040 (BS0). **BS2 BS1 BS0 Bus Mode** 0 0 0 80386DX-like, Little Endian, Bus Mode 4 0 0 1 80386SX-like, Little Endian, Bus Mode 3 0 1 0 80386DX-like, Big Endian, Bus Mode 4 0 1 1 Reserved 1 0 0 68040-like, Little Endian, Bus Mode 2 1 0 1 68030-like, Little Endian, Bus Mode 1 1 1 0 68040-like, Big Endian, Bus Mode 2 1 1 1 68030-Like, Big Endian, Bus Mode 1

Table 3.6 describes the Additional Interface Signals group.

Table 3.6 Additional Interface Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
MAC/	MAC/	MAC/	MAC/	26	**Memory Access Control** (O, O). This signal indicates if the next access will be to local (onboard) or far (system) memory. When MAC/=1, the memory access is to local memory. When MAC/ = 0, the access is to far memory. The default setting is zero; all accesses are far.
TSTOUT	TSTOUT	TSTOUT	TSTOUT	78	**Test Out** (O, O). This signal is used to test the connectivity of the LSI53C770 signals using an "AND tree" scheme. The Test Out pin is only driven when the Test In pin is driven LOW; otherwise the signal is 3-stated.
TSTIN/	TSTIN/	TSTIN/	TSTIN/	182	**Test In** (I, I). When this pin is driven LOW, the LSI53C770 connects all input and outputs (excluding certain SCSI bus signals) to an "AND tree." The SCSI control signals and data lines (SD[15:0], SDP[1:0], CD/, IO/, MSG/, REQ/, ACK/, BSY/, SEL/, ATN/, RST/, and DIFFSENS) are not connected to the "AND tree." The output of the "AND tree" is connected to the Test Out pin. This allows manufacturers to verify chip connectivity to the board, and to determine exactly which pins are not properly attached. When the TSTIN pin is driven LOW, internal pull-ups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be 3-stated, and the TSTOUT pin will be enabled. Connectivity can be tested by driving one of the LSI53C770 pins LOW. The TSTOUT pin should respond accordingly by driving LOW.
BERR/	TEA/	TEA/	TEA/	50	**Bus Error Acknowledge** (O, I). In Bus Mode 1, this indicates that a bus fault has occurred. Used with HALT/ to force a bus retry. Will be asserted on an illegal slave access. **Transfer Error Acknowledge** (O, I). Indicates that a bus fault has occurred in Bus Modes 2, 3, or 4. Used in conjunction with TA/-READYI/ to force a bus retry. Will be asserted on an illegal slave access.

Table 3.6 Additional Interface Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
HALT/	TIP/	TIP/	TIP/	57	**Halt** (Z, I). Input only in Bus Mode 1, used with BERR/ to indicate a bus retry cycle. **Transfer in Progress** (Z, O). Output signal for Bus Modes 2, 3, and 4, indicating that bus activity is in progress.
AUTO/	AUTO/	AUTO/	AUTO/	127	**SCRIPTS Autostart Mode** (I, I). In all bus modes, this signal selects between automatic SCRIPTS and manual SCRIPTS start modes. AUTO/ = 0 Auto start. The DMA SCRIPTS Pointer (DSP) register will point to an address of all zeros following a chip reset. This address is the starting address of the SCRIPTS instructions. The SCRIPTS instructions will be automatically fetched and executed until an Interrupt instruction occurs. AUTO/ = 1 Manual start. The DMA SCRIPTS Pointer (DSP) must be written to so that it points to the starting address of the SCRIPTS instructions. The SCRIPTS instructions will be automatically fetched and executed until an interrupt condition occurs.
GPIO[4:0]	GPIO[4:0]	GPIO[4:0]	GPIO[4:0]	43–39	**General Purpose Input/Output** (I/O, I/O). In all bus modes, these signals are user programmable inputs/outputs. GPIO[3:0] power up as inputs, and GPIO4 powers up as an output.

Table 3.7 describes the SCSI Signals group.

Table 3.7 SCSI Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
DIFFSENS	DIFFSENS	DIFFSENS	DIFFSENS	128	**Differential Sense** (I, I). This pin detects the presence of a SE device on a differential system. When using external differential transceivers and a zero is detected on this pin, all chip SCSI outputs will be 3-stated to avoid damage to the transceivers. When running in SE mode, this pin should be tied HIGH. The normal value of this pin is 1.
SCLK	SCLK	SCLK	SCLK	125	**SCSI Clock** (I, I). SCLK is used to derive all SCSI related timings. The speed of this clock will be determined by the application requirements; in some applications, SCLK and BCLK may be tied to the same source.
SDATA/	SDATA/	SDATA/	SDATA/	172, 174–176, 140–142, 144, 161, 162, 164–167, 169, 170, 171, 160	**SCSI Data** (I/O, I/O). These open collector signals include the following data lines and parity signals for all bus modes. SD[15:0]/ 16-bit SCSI data bus SDP[1:0]/ SCSI data parity pins
SCTRL/	SCTRL/	SCTRL/	SCTRL/	147, 145, 150, 146, 152, 153, 149, 159, 151	Open Collector **SCSI Control** signals (I/O, I/O): C_D/ SCSI phase line, command/data I_O/ SCSI phase line, input/output MSG/ SCSI phase line, message REQ/ Data handshake signal from target device ACK/ Data handshake signal from initiator device BSY/[1] SCSI bus arbitration signal, signal busy SEL/[1] SCSI bus arbitration signal, select device ATN/ Attention, the initiator is requesting a message out phase RST/[1] SCSI bus reset

Table 3.7 SCSI Signals (Cont.)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
SDIR[15:0]	SDIR[15:0]	SDIR[15:0]	SDIR[15:0]	191–194, 136–139, 178–180, 183–185, 187, 188	**SCSI Data Direction Control** (O, O). Differential driver direction control for SCSI data lines.
SDIRP0	SDIRP0	SDIRP0	SDIRP0	177	**SCSI Parity Direction Control** (O, O). Differential driver direction control for SCSI parity signal (bits [7:0]).
SDIRP1	SDIRP1	SDIRP1	SDIRP1	189	**SCSI Parity Direction Control** (O, O). Differential driver direction control for SCSI parity signal (bits [15:8]).
BSYDIR	BSYDIR	BSYDIR	BSYDIR	134	**SCSI BSY/ Control** (O, O). Differential driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	SELDIR	SELDIR	132	**SCSI SEL/ Control** (O, O). Differential driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	RSTDIR	RSTDIR	133	**SCSI RST/ Control** (O, O). Differential driver enable control for SCSI RST/ signal.
IGS	IGS	IGS	IGS	131	**Initiator Direction Control** (O, O). Differential driver direction control for initiator driver group.
TGS	TGS	TGS	TGS	129	**Target Direction Control** (O, O). Differential driver direction control for target driver group.

1. Input only in differential mode

Chapter 4
Registers

Throughout this chapter, registers are referenced by their little endian addresses, with big endian addresses in parentheses. The terms “set” and “assert” are used to refer to bits that are programmed to a binary one. Similarly, the terms “deassert,” “clear,” and “reset” are used to refer to bits that are programmed to a binary zero. Reserved bits should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active HIGH; the feature is enabled by setting the bit.

4.1 Register Descriptions

The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Registers can be addressed as bytes, words, or Dwords. Other access sizes will result in bus errors.

Warning: The only register that the host CPU can access while the LSI53C770 is executing SCRIPTS is the Interrupt Status (ISTAT) register; attempts to access other registers will interfere with the operation of the chip. However, all registers are accessible using SCRIPTS.

Table 4.1 is the register address map.

Table 4.1 LSI53C770 Register Address Map

31 16	15 0			
SCNTL3	SCNTL2	SCNTL1	SCNTL0	0x00
GPREG	SDID	SXFER	SCID	0x04
SBCL	SSID	SOCL	SFBR	0x08
SSTAT2	SSTAT1	SSTAT0	DSTAT	0x0C
DSA				0x10
RESERVED			ISTAT	0x14
CTEST3	CTEST2	CTEST1	CTEST0	0x18
TEMP				0x1C
CTEST6	CTEST5	CTEST4	DFIFO	0x20
DCMD	DBC			0x24
DNAD				0x28
DSP				0x2C
DSPS				0x30
SCRATCHA				0x34
DCNTL	DWT	DIEN	DMODE	0x38
ADDER				0x3C
SIST1	SIST0	SIEN1	SIEN0	0x40
GPCNTL	MACNTL	SWIDE	SLPAR	0x44
RESPID1	RESPID0	STIME1	STIME0	0x48
STEST3	STEST2	STEST1	STEST0	0x4C
RESERVED		SIDL		0x50
RESERVED		SODL		0x54
RESERVED		SBDL		0x58
SCRATCHB				0x5C
SCRATCHC				0x60
SCRATCHD				0x64
SCRATCHE				0x68
SCRATCHF				0x6C
SCRATCHG				0x70
SCRATCHH				0x74
SCRATCHI				0x78
SCRATCHJ				0x7C

Register: 0x00 (0x03)
SCSI Control Zero (SCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ARB[1:0]		START	WATN/	EPC	EPG	AAP	TRG
1	1	0	0	0	0	0	0

ARB[1:0] Arbitration Mode Bits 1 and 0 [7:6]

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection/reselection

Simple Arbitration

1. The LSI53C770 waits for a bus free condition to occur.
2. It asserts BSY/ and its SCSI ID (contained in the SCSI Chip ID (SCID) register) onto the SCSI bus. If the SEL/ signal is asserted by another SCSI device, the LSI53C770 deasserts BSY/, deasserts its ID and sets the Lost Arbitration bit (bit 3) in the SCSI Status Zero (SSTAT0) register.
3. After an arbitration delay, the CPU reads the SCSI Bus Data Lines (SBDL) register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the LSI53C770 wins arbitration.
4. Once the LSI53C770 wins arbitration, SEL is asserted using the SCSI Output Control Latch (SOCL) register for a bus clear plus a bus settle delay (1.2 µs) before a low level selection is performed.

Full Arbitration, Selection/Reselection

1. The LSI53C770 waits for a bus free condition.
2. It asserts BSY/ and its SCSI ID (the ID stored in the SCSI Chip ID (SCID) register) onto the SCSI bus.
3. If the SEL/ signal is asserted by another SCSI device or if the LSI53C770 detects a higher priority ID, the LSI53C770 deasserts BSY/, deasserts its ID, and waits until the next bus free state to try arbitration again.
4. The LSI53C770 repeats arbitration until it wins control of the SCSI bus. When it wins, the Won Arbitration bit is set in the SCSI Status Zero (SSTAT0) register, bit 2.
5. The LSI53C770 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SCSI Destination ID (SDID) register) and the LSI53C770 ID (the highest priority ID stored in the SCSI Chip ID (SCID) register).
6. After a selection is complete, the Function Complete bit is set in the SCSI Interrupt Status Zero (SIST0) register, bit 6.
7. If a selection time-out occurs, the Selection Time-out bit is set in the SCSI Interrupt Status One (SIST1) register, bit 2.

START **Start Sequence** **5**

When this bit is set, the LSI53C770 starts the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low level mode; during SCSI SCRIPTS operations, this bit is controlled by the SCRIPTS processor. Do not start an arbitration sequence if the Connected bit, bit 4 in the SCSI Control One (SCNTL1) register indicates that LSI53C770 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, check the connected bit in the in the SCSI Control One (SCNTL1) register to verify that the LSI53C770 is not connected to the SCSI bus.

WATN/ **Select with ATN/ on a Start Sequence** **4**

When this bit is set and the LSI53C770 is in initiator mode, the SCSI ATN/ signal is asserted during LSI53C770 selection of a target device. This is to inform the target that the LSI53C770 has a message to send. If a selection time-out occurs while attempting to select a target device, ATN/ is deasserted at the same time SEL/ is deasserted. When this bit is clear, the ATN/ signal is not asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but manual setting is possible in low level mode.

EPC **Enable Parity Checking** **3**

When this bit is set, the LSI53C770 checks the SCSI data bus for odd parity when data is received from the SCSI bus in either initiator or target mode. It also checks the host data bus for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SCSI Output Data Latch (SODL) register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SCSI Status Zero (SSTAT0) register is set and an interrupt may be generated.

If the LSI53C770 is operating in initiator mode and a parity error is detected, assertion of ATN/ is optional, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.

EPG **Enable Parity Generation/Parity Through** **2**

When this bit is set, the LSI53C770 generates SCSI parity. The host data bus parity lines DP[3:0] are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines flows through the LSI53C770 internal FIFOs and is driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus). This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

AAP **Assert ATN/ on Parity Error** **1**

When this bit is set, the LSI53C770 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal

is asserted before deasserting ACK/ during the transfer of the byte with the parity error. The Enable Parity Checking bit must also be set for the LSI53C770 to assert ATN/ in this manner. The following parity errors can occur:

- A parity error detected on data received from the SCSI bus.
- A parity error detected on data transferred to the LSI53C770 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ is not automatically asserted on the SCSI bus when a parity error is received.

TRG **Target Mode** **0**

This bit determines the default operating mode of the LSI53C770. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target). When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the LSI53C770 is an initiator device by default. Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator roles.

Register: 0x01 (0x02)

SCSI Control One (SCNTL1)

Read/Write

7	6	5	4	3	2	1	0
EXC	ADB	DHP	CON	RST	AESP	IARB	SST
0	0	0	0	0	0	0	0

EXC **Extra Clock Cycle of Data Setup** **7**

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design flexibility, though it affects the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

ADB **Assert SCSI Data Bus** **6**

When this bit is set, the LSI53C770 drives the contents of the SCSI Output Data Latch (SODL) register onto the SCSI data bus. When the LSI53C770 is an initiator, the SCSI I/O signal must be inactive to assert the SCSI Output Data Latch (SODL) contents onto the SCSI bus. The low order data and parity signal is always asserted onto the SCSI bus, whereas the high order data and parity signal is only asserted onto the SCSI bus if the Enable Wide SCSI bit (SCSI Control Three (SCNTL3), bit 3) is asserted and a data phase is specified by the SCSI phase signals. When the LSI53C770 is a target, the SCSI I/O signal must be active to assert the SCSI Output Data Latch (SODL) contents onto the SCSI bus. The contents of the SCSI Output Data Latch (SODL) register can be asserted at any time, even before the LSI53C770 is connected to the SCSI bus. Clear this bit when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

DHP **Disable Halt on Parity Error or ATN (Target Only)** **5**

The DHP bit is only defined for target mode operation. When this bit is clear, the LSI53C770 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the LSI53C770 may transfer up to three additional bytes (or words, if wide SCSI is enabled) before halting to synchronize between internal core cells. During synchronous operation, the LSI53C770 halts when there are no more outstanding synchronous offsets. If the LSI53C770 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error is not sent across the SCSI bus. When this bit is set, the LSI53C770 does not halt the SCSI transfer when ATN/ or a parity error is received.

CON **Connected** **4**

This bit is automatically set any time the LSI53C770 is connected to the SCSI bus as an initiator or as a target. It is set after the LSI53C770 successfully completing arbitration or when it responds to a bus-initiated selection or reselection. This bit is also set after the chip wins

simple arbitration when operating in low level mode. When this bit is clear, the LSI53C770 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature is used primarily during loopback mode.

RST **Assert SCSI RST/ Signal** **3**

Setting this bit asserts the SCSI RST/ signal. The RST/ signal remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor. In differential mode, RST/ becomes an input, and setting this bit causes RSTDIR to be asserted.

Note: Setting this bit in SCRIPTS causes a fatal interrupt, which halts SCRIPTS execution.

AESP **Assert Even SCSI Parity (force bad parity)** **2**

When this bit is set and the Enable Parity Generation bit is set (bit 2 in the SCSI Control Zero (SCNTL0) register), the LSI53C770 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the LSI53C770. If parity checking is enabled, then the LSI53C770 checks data received for odd parity. This bit is used for diagnostic testing and is cleared during normal operation. It is useful to generate parity errors to test error handling functions.

IARB **Immediate Arbitration** **1**

Setting this bit causes the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multithreaded applications. The ARB[1:0] bits in SCSI Control Zero (SCNTL0) should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration is retried until won. At that point, the LSI53C770 holds BSY and SEL asserted, and waits for a select or reselect sequence to be requested. The Immediate Arbitration bit is reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition clears IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCSI Control Register Two (SCNTL2), bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the SCRIPTS processor registers should be set. Then one of two things happens:

- The Won Arbitration bit (SCSI Status Zero (SSTAT0), bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the LSI53C770 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.
- The abort will complete because the LSI53C770 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SCSI Status Zero (SSTAT0), bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

SST **Start SCSI Transfer** **0**

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SCSI Output Control Latch (SOCL). This bit is self-clearing. This bit should not be set for low level operation.

Register: 0x02 (0x01)

SCSI Control Register Two (SCNTL2)

Read/Write

7	6	5	4	3	2	1	0
SDU	CHM	SLPMD	SLPHBEN	WSS	VUE1	VUE0	WSR
0	0	0	0	0	0	0	0

SDU **SCSI Disconnect Unexpected** **7**

When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error is generated (see the Unexpected Disconnect bit in the SCSI Interrupt Status Zero (SIST0) register, bit 2).

During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be cleared with a register write (Move 0x7f_&_SCNTL2_to_SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue, or Release Recovery message, or before deasserting ACK after receiving a Disconnect command or Command Complete message.

CHM **Chained Mode** **6**

This bit determines whether or not the SCSI core is programmed for chained SCSI mode. This bit is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode is primarily used to transfer consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte boundary, the LSI53C770 stores the last byte in the SCSI Wide Residue Data (SWIDE) register during a receive operation, or in the SCSI Output Data Latch (SODL) register during a send operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer is completed.

SLPMD **SLPAR Mode Bit** **5**

If this bit is cleared, the SCSI Longitudinal Parity (SLPAR) register functions like the LSI53C720. If this bit is set, the SCSI Longitudinal Parity (SLPAR) register reflects the high or low byte of the SLPAR word, depending on the state of SCSI Control Register Two (SCNTL2), bit 4. It also allows a seed value to be written to the SCSI Longitudinal Parity (SLPAR) register.

SLPHBEN **SLPAR High Byte Enable** **4**

If this bit is cleared, the low byte of the SLPAR word is accessible through the SCSI Longitudinal Parity (SLPAR) register. If this bit is set, the high byte of the SLPAR word is present in the SCSI Longitudinal Parity (SLPAR) register.

WSS **Wide SCSI Send** **3**

When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit clears the WSS flag. This clearing function is self-clearing.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of “chain” data in the SCSI Output Data Latch (SODL) register. This data becomes the first low-order byte sent when married with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation clears this bit. Also, performing any nonwide transfer clears this bit.

VUE1 **Vendor Unique Enhancements Bit 1** **2**

This bit is a read only value indicating whether the group code field in the SCSI instruction is standard or vendor unique. If reset, the bit indicates standard group codes; if set, the bit indicates vendor unique group codes. The value in this bit is reloaded at the beginning of all asynchronous target receives. The default for this bit is reset.

VUE0 **Vendor Unique Enhancements Bit 0** **1**

This bit is used to disable the automatic byte count reload during Block Move instructions in the command phase. If this bit is cleared, the device reloads the Block Move byte count if the first byte received is one of the standard group codes. If this bit is set, the device does not reload the Block Move byte count, regardless of the group code.

WSR **Wide SCSI Receive** **0**

When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Setting this bit clears the WSR flag. This clearing function is self-clearing.

The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or nonchained block move command, and temporarily stored the high-order byte in the SCSI Wide Residue Data (SWIDE) register rather than passing the byte out the DMA channel. The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SCSI Wide Residue Data (SWIDE) may be “residue” data, valid data for a subsequent data transfer, or overrun data. The byte is read as normal data by starting a data receive transfer.

Performing a SCSI send operation clears this bit. Also, performing any nonwide transfer clears this bit.

Register: 0x03 (0x00)

SCSI Control Three (SCNTL3)

Read/Write

7	6			4	3	2		0
Ultra	SCF[2:0]				EWS	CCF[2:0]		
0	0	0	0		0	0	0	0

Ultra **Ultra Enable** **7**

Setting this bit enables Ultra SCSI synchronous SCSI transfers in systems that have an 80 MHz clock. The default value of this bit is 0. This bit should remain cleared in systems that have a 40 MHz clock, unless the SCSI clock doubler feature is used to increase the SCLK frequency to at least 80 MHz.

When this bit is set, the signal filtering period for SREQ/ and SACK/ automatically changes to 15 ns, regardless of the value of the Extend REQ/ACK Filtering bit in the SCSI Test Register Two (STEST2) register.

SCF[2:0] **Synchronous Clock Conversion Factor** **[6:4]**
These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. Write these to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. See the table under the description of bits [2:0] of this register for the valid combinations. For additional information on how the synchronous transfer rate is determined, refer to Chapter 2. To migrate from a Fast SCSI-2 system with a 40 MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80 MHz clock.

EWS **Enable Wide SCSI** **3**
When this bit is clear, all information transfer phases are assumed to be eight bits, transmitted on SD[7:0]/, and SDP0/. When this bit is asserted, data transfers are done 16 bits at a time, with the least significant byte on SD[7:0]/, and SDP0/ and the most significant byte on SD[14:8], SDP1/. Command, Status, and Message phases are not affected by this bit.

CCF[2:0] **Clock Conversion Factor** **[2:0]**
These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as follows. All other combinations are reserved and should never be used. The synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above.

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor Frequency	SCSI Clock (MHz)
0	0	0	SCLK/3	50.01-75
0	0	1	SCLK/1	16.67-25
0	1	0	SCLK/1.5	25.01-37.5
0	1	1	SCLK/2	37.51-50
1	0	0	SCLK/3	50.01-75
1	0	1	SCLK/4	75.01-100.00
1	1	0	Reserved	–
1	1	1	Reserved	–

It is important that these bits be set to the proper values to guarantee that the LSI53C770 meets the SCSI timings as defined by the ANSI specification. To migrate from a Fast SCSI-2 system with a 40 MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80 MHz clock. If the SCSI clock doubler is enabled, use the desired frequency after doubling to determine the conversion factor.

Register: 0x04 (0x07)

SCSI Chip ID (SCID)

Read/Write

7	6	5	4	3			0
R	RRE	SRE	R	ID[3:0]			
x	0	0	x	0	0	0	0

R **Reserved** **7**

RRE **Enable Response to Reselection** **6**

When this bit is set, the LSI53C770 is enabled to respond to bus-initiated reselection at the chip ID in the Response ID Zero (RESPID0) and Response ID One (RESPID1) registers. Note that the LSI53C770 does not automatically reconfigure itself to initiator mode as a result of being reselected.

SRE **Enable Response to Selection** **5**

When this bit is set, the LSI53C770 is able to respond to bus-initiated selection at the chip ID encoded in the Response ID Zero (RESPID0) and Response ID One (RESPID1) registers. Note that the chip does not automatically reconfigure itself to target mode as a result of being selected.

R **Reserved** **4**

ID[3:0] **Encoded Chip SCSI ID** **[3:0]**

These bits are used to store the LSI53C770 encoded SCSI ID. This is the ID which the chip asserts when awaiting for the SCSI bus. The priority of the 16 possible IDs, in descending order is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

Register: 0x05 (0x06)

SCSI Transfer (SXFER)

Read/Write

7			5	4	3			0
TP[2:0]				R	MO[3:0]			
0	0	0		x	0	0	0	0

When using Table Indirect I/O commands, bits [7:5] and [3:0] of this register are loaded from the I/O data structure. For additional information on how to determine the synchronous transfer rate is determined, refer to Chapter 2, "Functional Description."

TP[2:0] **SCSI Synchronous Transfer Period** **[7:5]**

These bits determine the SCSI synchronous transfer period (XFERP) used by the LSI53C770 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

Note: For Ultra SCSI transfers, the ideal transfer period is 4, however, 5 is acceptable. Setting the transfer period to a value greater than 5 is not recommended.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the LSI53C770 should use when transferring SCSI data is determined in the following example.

The LSI53C770 is connected to a hard disk which can transfer data at 10 Mbytes/s synchronously. The LSI53C770 SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

Synchronous Send Rate = (SCLK/SCF)/XFERP

Synchronous Receive Rate = (SCLK/SCF) / 4

Where:

SCLK SCLK

XFERP Synchronous transfer period, SCNTL3 bits

SCF Synchronous Clock Conversion Factor SCNTL3 bits

Table 4.2 Examples of Synchronous Transfer Periods and Rates for SCSI-1

CLK (MHz)	SCSI CLK/SCNTL3 Bits[6:4]	XFERP	Synchronous Transfer Period (ns)	Synchronous Send Rate (Mbytes/s)	Synchronous Receive Rate (Mbytes/s)
80	÷ 4	4	200	5	5
80	÷ 4	5	250	4	5
66.67	÷ 3	4	180	5.55	5.55
66.67	÷ 3	5	225	4.44	5.55
50	÷ 2	4	160	6.25	6.25
50	÷ 2	5	200	5	6.25
40	÷ 2	4	200	5	5
37.50	÷ 1.5	4	160	6.25	6.25
33.33	÷ 1.5	4	180	5.55	5.55
25	÷ 1	4	160	6.25	6.25
20	÷ 1	4	200	5	5
16.67	÷ 1	4	240	4.17	4.17

Table 4.3 Examples of Transfer Periods and Rates for Fast SCSI and Ultra SCSI

CLK (MHz)	SCSI CLK/SCNTL3 Bits[6:4]	XFERP	Synchronous Transfer Period (ns)	Synchronous Send Rate (Mbytes/s)	Synchronous Receive Rate (Mbytes/s)
80	÷ 1	4	50	20.0	20.0
80	÷ 2	4	100	10.0	10.0
66.67	÷ 1.5	4	90	11.11	11.11
66.67	÷ 1.5	5	112.5	8.88	8.88
50	÷ 1	4	80	12.5	12.5
50	÷ 1	5	100	10.0	12.5
40	÷ 1	4	100	10.0	10.0
37.50	÷ 1	4	106.67	9.375	9.375
33.33	÷ 1	4	120	8.33	8.33
25	÷ 1	4	160	6.25	6.25
20	÷ 1	4	200	5	5
16.67	÷ 1	4	240	4.17	4.17

R **Reserved** **4**

MO[3:0] **Max SCSI Synchronous Offset)** **[3:0]**
These bits describe the maximum SCSI synchronous offset used by the LSI53C770 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the LSI53C770. These bits determine the LSI53C770's method of transfer for Data-In and Data-Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0-Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	x	x	1	Reserved
1	x	1	x	Reserved
1	1	x	x	Reserved

Register: 0x06 (0x05)

SCSI Destination ID (SDID)

Read/Write

7			4	3			0
R				ID[3:0]			
x	x	x	x	0	0	0	0

R **Reserved** **[7:4]**

ID[3:0] **Encoded Destination SCSI ID** **[3:0]**

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases, respectively. When executing SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction. The value written is the binary-encoded ID. The priority of the 16 possible IDs, in descending order, is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

Register: 0x07 (0x04)
General Purpose (GPREG)
Read/Write

7		5	4				0
R			GPIO[4:0]				
x	x	x	0	1	1	1	1

R **Reserved** **[7:5]**

GPIO[4:0] **General Purpose Inputs/Outputs** **[4:0]**
These bits allow the LSI53C770 to detect the input signals of a connected device. The general purpose inputs can be used to sense the LSI53C770 chip ID or board configuration at power up. It is also possible to program these signals as live inputs and sense them through a register to register Move Instruction. These are live signals; if the pin is changing, the data is also changing. The bit values in the General Purpose Control (GPCNTL) register (0x47) determine whether these bits are inputs or outputs. Bits [3:0] power up as inputs, and Bit 4 powers up as an output. The general purpose output feature may be used to enable attached ROM, RAM, LEDs, or other components on an LSI53C770 board.

Note: The input pins all have 100 µA internal pull-ups.

Register: 0x08 (0x0B)
SCSI First Byte Received (SFBR)
Read/Write

7							0
1B[7:0]							
0	0	0	0	0	0	0	0

1B[7:0] **First Byte Received** **[7:0]**
This register contains the first byte received in any asynchronous information transfer phase. For example, when the LSI53C770 is operating in initiator mode, this register contains the first byte received in Message-In, Status, and Data-In phases.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register, even if the present phase is the same as the last phase. The first byte value received for a particular input phase is not valid until after a Move instruction is executed.

This register is also the accumulator for register read-modify-writes with SCSI First Byte Received (SFBR) as the destination. This allows bit testing after an operation.

This register also holds the state of the lower eight bits of the SCSI data bus during a selection or reselection, unless the COM bit in the DMA Control (DCNTL) register is set.

Register: 0x09 (0x0A)

SCSI Output Control Latch (SOCL)
Read/Write

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
0	0	0	0	0	0	0	0

REQ **Assert SCSI REQ/ Signal** **7**

ACK **Assert SCSI ACK/ Signal** **6**

BSY **Assert SCSI BSY/ Signal** **5**

SEL **Assert SCSI SEL/ Signal** **4**

ATN **Assert SCSI ATN/ Signal** **3**

MSG **Assert SCSI MSG/ Signal** **2**

C/D **Assert SCSI C_D/ Signal** **1**

I/O **Assert SCSI I_O/ Signal** **0**

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SCSI Output Control Latch (SOCL) is only used when transferring data using programmed I/O. Some bits are

set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the LSI53C770 starts executing SCSI SCRIPTS.

Register: 0x0A (0x09)

SCSI Selector ID Register (SSID)

Read Only

7	6		4	3			0
VAL	R			Encoded SCSI Destination ID			
x	x	x	x	x	x	x	x

VAL **SCSI Valid Bit** **7**

If VAL is asserted, then the two SCSI IDs are detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID is present and the contents of the encoded destination ID are meaningless.

R **Reserved** **[6:4]**

Encoded SCSI Destination ID

Encoded SCSI Destination ID **[3:0]**

Reading the SCSI Selector ID Register (SSID) register immediately after the LSI53C770 is selected or reselected returns the binary-encoded SCSI ID of the device that performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register: 0x0B (0x08)
SCSI Bus Control Lines (SBCL)
Read Only

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
x	x	x	x	x	x	x	x

REQ	**REQ/ Status**	**7**
ACK	**ACK/ Status**	**6**
BSY	**BSY/ Status**	**5**
SEL	**SEL/ Status**	**4**
ATN	**ATN/ Status**	**3**
MSG	**MSG/ Status**	**2**
C/D	**C_D/ Status**	**1**
I/O	**I_O/ Status**	**0**

This register returns the SCSI control line status. A bit is set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. This register can be used for diagnostics testing or operation in low level mode.

Register: 0x0C (0x0F)
DMA Status (DSTAT)
Read Only

7	6	5	4	3	2	1	0
DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
1	0	0	0	0	0	0	0

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the LSI53C770 stacks interrupts). The DIP bit

in the Interrupt Status (ISTAT) register will also be cleared. DMA interrupt conditions may be individually masked through the DMA Interrupt Enable (DIEN) register.

When performing consecutive 8-bit reads of the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), and SCSI Interrupt Status One (SIST1) registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. To avoid missing a SCSI interrupt while reading any of these registers when the Interrupt Status (ISTAT) SIP and DIP bits may not be set, read SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) before DMA Status (DSTAT).

DFE **DMA FIFO Empty** **7**
This status bit is set when the DMA FIFO (DFIFO) is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and does not cause an interrupt. This bit is not cleared by reading the register.

HPE **Host Parity Error** **6**
This bit is set when a host bus parity error is detected during a slave write or DMA read operation.

BF **Bus Fault** **5**
This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the LSI53C770 is bus master, and is defined as a memory cycle that ends with the assertion of BERR/ or TEA/.

ABRT **Aborted** **4**
This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the Interrupt Status (ISTAT) register.

SSI **SCRIPTS Step Interrupt** **3**
If the Single Step Mode bit in the DMA Control (DCNTL) register is set, this bit is set and an interrupt is generated after successful execution of each SCRIPTS instruction.

SIR **SCRIPTS Interrupt Instruction Received** **2**
This status bit is set whenever a SCRIPTS Interrupt instruction is received.

WTD **Watchdog Time-out Detected** **1**
This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified time-out period.

IID **Illegal Instruction Detected** **0**
This status bit is set any time an illegal instruction is detected, whether the LSI53C770 is operating in single step mode or automatically executing SCSI SCRIPTS.

This bit is also set if the LSI53C770 is executing a Wait Disconnect instruction and the SCSI REQ line asserts without a disconnect occurring.

Register: 0x0D (0x0E)
SCSI Status Zero (SSTAT0)
Read Only

7	6	5	4	3	2	1	0
ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
0	0	0	0	0	0	0	0

ILF **SIDL Least Significant Byte Full** **7**
This bit is set when the least significant byte in the SCSI Input Data Latch (SIDL) register contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch (SIDL) register before being sent to the DMA FIFO and then to the host bus. The SCSI Input Data Latch (SIDL) register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

ORF **SODR Least Significant Byte Full** **6**
This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR

register is used by the SCSI logic as a second storage register when sending data synchronously. It is not readable or writable by the user. It is possible to use this bit to determine how many bytes reside in the chip when an error occurs.

OLF **SODL Least Significant Byte Full** **5**

This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SCSI Output Data Latch (SODL) register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. It is possible to use this bit to determine how many bytes reside in the chip when an error occurs.

AIP **Arbitration in Progress** **4**

Arbitration in Progress (AIP = 1) indicates that the LSI53C770 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.

LOA **Lost Arbitration** **3**

When set, LOA indicates that the LSI53C770 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

WOA **Won Arbitration** **2**

When set, WOA indicates that the LSI53C770 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCSI Control Zero (SCNTL0) register must be full arbitration and selection to set this bit.

RST/ **SCSI RST/ Signal** **1**

This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the Interrupt Status (ISTAT) register. This bit is not latched and may change as it is read.

SDP/ **SCSI SDP0/ Parity Signal** **0**

This bit represents the active HIGH current status of the SCSI SDP0/ parity signal. This signal is not latched and may change as it is read.

Register: 0x0E (0x0D)

SCSI Status One (SSTAT1)

Read Only

7			4	3	2	1	0
FF[3:0]				SDP0	MSG	C/D	I/O
0	0	0	0	x	x	x	x

FF[3:0] **FIFO Flags** **[7:4]**

These five bits define the number of bytes or words that currently reside in the LSI53C770 SCSI synchronous data FIFO as shown in Table 4.4. These bits are not latched and they will change as data moves through the FIFO.

Table 4.4 SCSI Synchronous Data FIFO Word Count

FF4 (SSTAT2 Bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14

Table 4.4 SCSI Synchronous Data FIFO Word Count (Cont.)

FF4 (SSTAT2 Bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	1	1	1	1	15
1	0	0	0	0	16

SDP0 **Latched SCSI Parity** **3**

This bit reflects the SCSI parity signal (SDP0) corresponding to the data latched in the SCSI Input Data Latch (SIDL) register. It changes when a new byte is latched into the least significant byte of the SCSI Input Data Latch (SIDL) register. This bit is active HIGH, in other words, it is set when the parity signal is active.

MSG **SCSI MSG/ Signal** **2**

C/D **SCSI C_D/ Signal** **1**

I/O **SCSI I_O/ Signal** **0**

These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Register: 0x0F (0x0C)

SCSI Status Two (SSTAT2)

Read Only

7	6	5	4	3	2	1	0
ILF1	ORF1	OLF1	FF4	SD[15:8]	DIFF	LDSC	SDP1
0	0	0	0	x	0	1	x

ILF1 **SIDL Most Significant Byte Full** **7**

This bit is set when the most significant byte in the SCSI Input Data Latch (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch (SIDL) register before being sent to the DMA FIFO and then to the host bus. The SCSI Input Data Latch (SIDL) register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

ORF1 **SODR Most Significant Byte Full** **6**

This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. This bit is used to determine how many bytes reside in the chip when an error occurs.

OLF1 **SODL Most Significant Byte Full** **5**

This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SCSI Output Data Latch (SODL) register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. It is possible to use this bit to determine how many bytes reside in the chip when an error occurs.

FF4 **FIFO Flags** **4**

This is the most significant bit in the SCSI FIFO Flags field, with the rest of the bits in SCSI Status One (SSTAT1). For a complete description of this field, see the definition for SCSI Status One (SSTAT1) bits [7:4].

SD[15:8] **Latched SCSI Parity for SD[15:8]** **3**

This active HIGH bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SCSI Input Data Latch (SIDL) register.

DIFF **DIFFSENSE SENSE** **2**

If this bit is reset, the correct cable type has been connected for the differential operation. If this bit is set, a SE cable has been connected to the device's DIFFSENSE pin.

LDSC **Last Disconnect** **1**

This bit is used in conjunction with the Connected (CON) bit in SCSI Control One (SCNTL1). It allows the user to

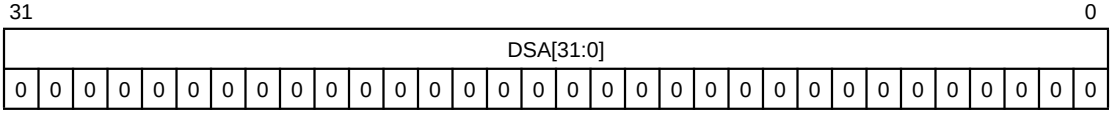
detect the case in which a target device disconnects, and then some SCSI device selects or reselects the LSI53C770. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect is indicated. This bit is set when the Connected bit in SCSI Control One (SCNTL1) is off. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCSI Control One (SCNTL1) is on.

SDP1 **SCSI SDP1 Signal** **0**

This bit represents the active HIGH current state of the SCSI SDP1 parity signal. It is unlatched and may change as it is read.

Registers: 0x10–0x13 (0x10–0x13)

Data Structure Address (DSA)
Read/Write



DSA **Data Structure Address** **[31:0]**

This 32-bit register contains the base address used for all table indirect calculations. During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register: 0x14 (0x17)

Interrupt Status (ISTAT)
Read/Write

7	6	5	4	3	2	1	0
ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
0	0	0	0	0	0	0	0

This is the only register that is accessible by the host CPU while the LSI53C770 is executing SCRIPTS (without interfering in the operation of the LSI53C770). It is used to poll for interrupts if interrupts are disabled. Read this register after servicing an interrupt to check for stacked interrupts.

ABRT **Abort Operation** **7**

Setting this bit aborts the current operation under execution by the LSI53C770. If this bit is set and an interrupt is received, clear this bit before reading the DMA Status (DSTAT) register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit.
2. Wait for an interrupt.
3. Read the Interrupt Status (ISTAT) register.
4. If the SCSI Interrupt Pending bit is set, then read the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) register to determine the cause of the SCSI Interrupt and go back to Step 2.
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 0x00 value to this register.
6. Read the DMA Status (DSTAT) register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Note: The abort function cannot be used during a select or reselect instruction. In these cases, use the time-out feature.

After an abort, follow the data recovery steps in Chapter 2 to make sure no data is left in the chip.

RST **Software Reset** **6**

Setting this bit resets the LSI53C770. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not assert the SCSI RST/ signal. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset also clears this bit). This reset does not clear the Enable Acknowledge (EA) bit, Function Code 1 bit, or the ID Mode bit, DMA Control (DCNTL), bit 0.

SIGP **Signal Process** **5**

SIGP is a R/W bit that can be written at any time, and polled and reset using Chip Test Two (CTEST2). The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS instruction.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/reselection condition.

SEM **Semaphore** **4**

The SCRIPTS processor may set this bit using a SCRIPTS register write instruction. An external processor may also set this bit while the LSI53C770 is executing a SCRIPTS operation. This bit enables the LSI53C770 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the LSI53C770 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

CON **Connected** **3**

This bit is automatically set any time the LSI53C770 is connected to the SCSI bus as an initiator or as a target. It is set after successfully completing arbitration or when the LSI53C770 responds to a bus-initiated selection or reselection. It is also be set after the LSI53C770 wins arbitration when operating in low level mode. When this bit is clear, the LSI53C770 is not connected to the SCSI bus.

INTF **Interrupt-on-the-Fly** **2**

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs does not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. This bit must be written to one in order to clear it after it has been set. If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip

status registers. An Interrupt-on-the-Fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

SIP **SCSI Interrupt Pending** **1**

This status bit is set when an interrupt condition is detected in the SCSI portion of the LSI53C770. The following conditions cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence completes
- A selection or reselection time-out occurs
- The LSI53C770 is selected
- The LSI53C770 is reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- The handshake-to-handshake timer is expired
- The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, read the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers. Both registers must be read to clear the interrupt.

This bit is synchronous to BCLK, but may change during read cycles.

DIP **DMA Interrupt Pending** **0**

This status bit is set when an interrupt condition is detected in the DMA portion of the LSI53C770. The following conditions cause a DMA interrupt to occur:

- A host parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single step mode
- A SCRIPTS interrupt instruction is executed

- The Watchdog Timer decrements to zero
- An illegal instruction is detected

To clear DIP and determine exactly which condition(s) caused the interrupt, read the DMA Status (DSTAT) register.

This bit is synchronous to BCLK, but may change during read cycles.

Register: 0x18 (0x1B)

Chip Test Zero (CTEST0)

Read/Write

7	6	5	4	3	2	1	0
CDIS	SC[1:0]		GRP	DFP	EHP	TT1	C386E
0	0	0	0	x	0	0	0

CDIS **Cache Burst Disable** **7**

When this bit is set, the LSI53C770 does not request a cache line burst. When this bit is clear, the chip attempts cache line bursts when all necessary conditions are met.

Note: If the hardware does not support cache line bursts, set this bit to maximize performance.

SC[1:0] **Snoop Control** **[6:5]**

The values of these bits assert on the corresponding device pins during bus mastership if bit 0 of Chip Test Three (CTEST3) is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal host cycle request signal. These bits are not available for snoop mode if the Size Throttle Enable bit (DMA Control (DCNTL), bit 7) is set.

GRP **Generate Receive Parity** **4**

When this bit is set and the LSI53C770 is in parity pass through mode (Bit 2 in the SCSI Control Zero (SCNTL0) register is clear), parity received on the SCSI bus does not pass through the DMA FIFO. Parity generates as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt generates but a system parity

problem is not created. After reset or when the bit is cleared, and when parity pass through mode is enabled (bit 2 in SCSI Control Zero (SCNTL0) is clear), parity received on the SCSI bus passes through the LSI53C770 unmodified.

DFP **DMA FIFO Parity** **3**

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO using programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the Chip Test Six (CTEST6) register. Manually loading the FIFO moves this bit into the FIFO as the parity bit, along with the byte that came was written to the Chip Test Six (CTEST6) register.

EHP **Even Host Parity** **2**

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the LSI53C770 to generate even parity when driving data on the host data bus. The LSI53C770 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the LSI53C770 checks parity and sends the data to the SCSI bus. Clearing this bit causes the LSI53C770 to maintain odd parity throughout the chip.

TT1 **Transfer Type Bit** **1**

The inverted value of this bit is asserted on the TT1 pin during bus mastership in Bus Modes 2, 3, and 4 only. This bit is not used in Bus Mode 1. In Bus Mode 4, the TT1 pin is supported only if Cache 386 mode is not enabled. The TT0 bit is in the DMA Mode (DMODE) register.

C386E **Cache 386 Enable** **0**

Asserting this bit enables caching in the 80386DX bus mode. Caching implies that the chip supplies an address together with an Address Strobe (ADS/), and on the consecutive clocks the LSI53C770 waits for four READYI/ pulses and either supplies four Dwords of data or receives four Dwords of data. The LSI53C770 does not support caching in 80386SX mode or slave mode. The chip generates the Cache Burst Request (CBREQ) signal

and samples the Transfer Burst Inhibit (TBI) signal during the first data transfer (first READYI/). CBREQ/ indicates an attempt to execute a line transfer of four Dwords. TBI/ asserted indicates that the system memory does not support the LSI53C770 burst request. The chip powers up with this feature disabled. The bit is reset during either a software or hardware reset.

Register: 0x19 (0x1A)

Chip Test One (CTEST1)

Read Only

7			4	3			0
FMT[3:0]				FFL[3:0]			
1	1	1	1	0	0	0	0

FMT[3:0] **Byte Empty in DMA FIFO** **[7:4]**

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 is set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

FFL[3:0] **Byte Full in DMA FIFO** **[3:0]**

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 is set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register: 0x1A (0x19)
Chip Test Two (CTEST2)
Read Only

7	6	5	4	3	2	1	0
DDIR	SIGP	R		DFP	TEOP	DREQ	DACK
0	0	x	x	0	0	0	1

DDIR **Data Transfer Direction** **7**
This status bit indicates which direction data is being transferred. When this bit is set, the data is transferred from the SCSI bus to the host bus. When this bit is clear, the data is transferred from the host bus to the SCSI bus.

SIGP **Signal Process** **6**
This bit is a copy of the SIGP bit in the Interrupt Status (ISTAT) register (bit 5). The SIGP bit is used to signal a running SCRIPTS operation. When this register is read, the SIGP bit in the Interrupt Status (ISTAT) register is cleared.

R **Reserved** **[5:4]**

DFP **DMA FIFO Parity** **3**
This bit represents the parity bit of the DMA FIFO when the Chip Test Six (CTEST6) register reads data out of the FIFO. Reading the Chip Test Six (CTEST6) register unloads one data byte from the bottom of the DMA FIFO. When the Chip Test Six (CTEST6) register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

TEOP **SCSI True End of Process** **2**
This bit indicates the status of the LSI53C770 internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the LSI53C770. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

DREQ **Data Request Status** **1**
This bit indicates the status of the LSI53C770 internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

DACK **Data Acknowledge Status** **0**

This active LOW bit indicates the status of the LSI53C770 internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register: 0x1B (0x18)

Chip Test Three (CTEST3)

Read/Write

7			4	3	2	1	0
V[3:0]				FLF	CLF	FM	SM
x	x	x	x	0	0	0	0

V[3:0] **Chip Revision Level** **[7:4]**

These bits identify the chip revision level for software purposes.

FLF **Flush DMA FIFO** **3**

When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DMA Next Data Address (DNAD) register. The internal DMAWR signal, controlled by the Chip Test Five (CTEST5) register, determines the direction of the transfer. This bit is not self-clearing; clear it once the data is successfully transferred by the LSI53C770.

CLF **Clear DMA FIFO** **2**

When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the LSI53C770 has successfully cleared the appropriate FIFO pointers.

FM **Fetch Pin Mode** **1**

When set, this active LOW bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ is only active during the opcode portion of an instruction fetch. This allows the storage of SCRIPTS in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ is asserted for all bus cycles during instruction fetches.

SM **Snoop Pins Mode** **0**

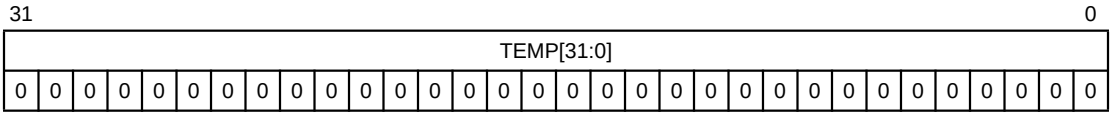
When set, the snoop pins change functions and become pure outputs that are always driven, except when in ZMODE. The values driven are listed in the following table. When clear, the snoop pins are driven during host bus ownership with the values of the Chip Test Zero (CTEST0) SC[1:0] bits.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal asserts prior to TS/_BR/ and is negated during the TS_BR/ of the last bus cycle. **Note**: This signal cannot be used when the STE bit in the DMA Control (DCNTL) register is set.

Registers: 0x1C–0x1F (0x1C–0x1F)

Temporary Stack (TEMP)

Read/Write



TEMP **Temporary Stack** **[31:0]**

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DMA SCRIPTS Pointer (DSP) register. This address points to the next instruction to execute. Do not write to this register while the LSI53C770 is executing SCRIPTS. During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register: 0x20 (0x23)
DMA FIFO (DFIFO)
Read/Write

7	6						0
R	BO[6:0]						
x	0	0	0	0	0	0	0

R **Reserved** **7**

BO[6:0] **Byte Offset Counter** **[6:0]**
These seven bits indicate the amount of data transferred between the SCSI core and the DMA core. It is used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores. Once the chip has stopped transferring data, these bits are stable.

The following steps determine how many bytes are left in the DMA FIFO:

1. Subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register.
2. AND the result with 0x7F for a byte count between zero and 96.

Register: 0x21 (0x22)
Chip Test Four (CTEST4)
Read/Write

7	6	5	4	3	2		0
MUX	ZMOD	ZSD	SRTM	EHPC	FBL[2:0]		
0	0	0	0	0	0	0	0

MUX **Host Bus Multiplex Mode** **7**
When set, the MUX bit puts the LSI53C770 into host bus multiplex mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is 3-stated), and then 3-states the address bus and drives the data bus (if a write). This allows the

address and data buses to be tied together. It should be written before acquiring bus mastership. Multiplex mode is only available in Bus Mode 2.

ZMOD **High Impedance Mode** **6**

Setting this bit causes the LSI53C770 to place all output and bidirectional pins into a high impedance state. In order to read data out of the LSI53C770, this bit must be cleared.

This bit is intended for board level testing only. Setting this bit during system operation results in a system failure.

ZSD **SCSI DMA High Impedance Mode** **5**

Setting this bit causes the LSI53C770 to place the SCSI data bus (SD [15:0]) and the parity lines (SDP [1:0]) in a high impedance state. In order to transfer data on the SCSI bus, this bit must be cleared. This bit differs from the SCSI High Impedance Mode bit in the SCSI Test Register Two (STEST2) register, in that it only affects the SCSI data lines.

SRTM **Shadow Register Test Mode** **4**

Setting this bit allows the user access to the shadowed Temporary Stack (TEMP) and Data Structure Address (DSA) registers. The registers are shadowed to prevent them from being overwritten during a Memory-to-Memory Move operation. The Data Structure Address (DSA) and Temporary Stack (TEMP) registers contain the base address used for table indirect calculations, and the instruction address pointer for a call or return instruction, respectively.

EHPC **Enable Host Parity Check** **3**

Setting this bit enables parity checking during slave write and DMA read execution if the Enable Parity Generation bit is cleared (SCSI Control Zero (SCNTL0), bit 2). The system powers up with this bit disabled so that the LSI53C770 functions properly with systems that do not support parity.

FBL[2:0] **FIFO Byte Control** **[2:0]**

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	x	x	Disabled	N/A
1	0	0	0	D[7:0]
1	0	1	1	D[15:8]
1	1	0	2	D[23:16]
1	1	1	3	D[31:24]

These bits define which byte lane of the DMA FIFO is read or written when the Chip Test Six (CTEST6) register is read or written. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

Register: 0x22 (0x21)

Chip Test Five (CTEST5)

Read/Write

7	6	5	4	3	2	1	0
ADCK	BBCK	R	MASR	DDIR	RAM[1:0]		RAMEN
0	0	x	0	0	0	0	0

ADCK **Clock Address Incrementor** **7**

Setting this bit increments the address pointer contained in the DMA Next Data Address (DNAD) register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

BBCK **Clock Byte Counter** **6**

Setting this bit decrements the byte count contained in the DMA Byte Counter (DBC) register. The DMA Byte Counter (DBC) register supports 24 bits. It is

decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DMA Byte Counter (DBC) register.

R **Reserved** **5**

MASR **Master Control for Set or Reset Pulses** **4**
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is cleared, bit 3 deasserts the corresponding signals. Do not change this bit and bit 3 in the same write cycle.

DDIR **DMA direction** **3**
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data is transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

RAM[1:0] **SCRIPTS RAM Bits [1:0]** **[2:1]**
These bits are used to enable the 4K internal SCRIPTS RAM. Their values combine to allow three different implementations of the SCRIPTS RAM. For more information on the internal SCRIPTS RAM, see Chapter 2, "Functional Description."

Table 4.5 SCRIPTS RAM Access

Bit 2	Bit 1	Method
0	0	SCRIPTS RAM disabled
0	1	SCRIPTS RAM accessed through indexed addressing in chip register space
1	0	SCRIPTS RAM accessed through increased chip select address space
1	1	SCRIPTS RAM access through additional chip select pin

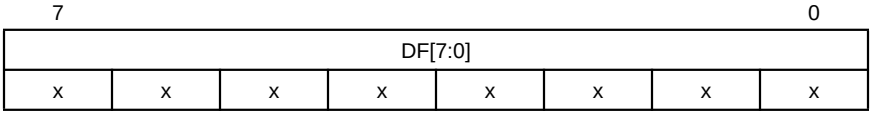
RAMEN **RAM Base Address Enable** **0**
When this bit is set, the Scratch Register A (SCRATCHA) register is shadowed to hold the base address of the

internal SCRIPTS RAM. This allows the internal chip logic to recognize the location of the SCRIPTS RAM in the system memory map. The actual contents of the Scratch Register A (SCRATCHA) register are preserved. This bit also causes SCRATCHB to become the indexed address pointer when the indexed mode has been enabled. The actual contents of SCRATCHB are preserved.

Register: 0x23 (0x20)

Chip Test Six (CTEST6)

Read/Write



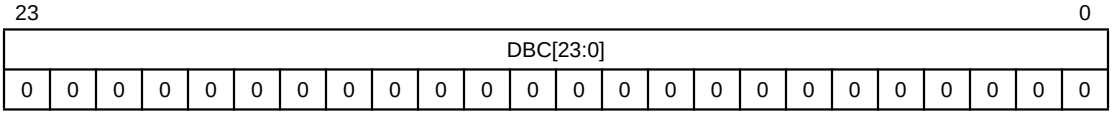
DF[7:0] **DMA FIFO** **[7:0]**

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the Chip Test Two (CTEST2) register. To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS.

Registers: 0x24–0x26 (0x25–0x27)

DMA Byte Counter (DBC)

Read/Write



DBC **DMA Byte Counter** **[23:0]**

This 24-bit register determines the number of bytes transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the LSI53C770. The DBC counter is decremented each time that the AS/ (TS/ in Bus Mode 2, ADS/ in Bus Modes 3 and 4) signal is pulsed by the LSI53C770. It is decremented by an amount equal to the number of bytes that were transferred.

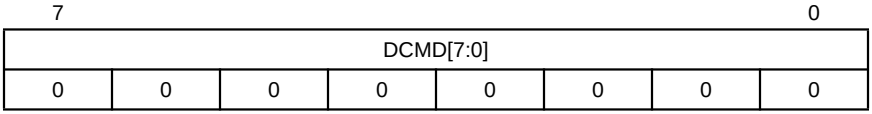
The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DMA Byte Counter (DBC) register is 0xFFFFFF. If the instruction is Block Move and a value of 0x000000 is loaded into the DMA Byte Counter (DBC) register, an illegal instruction interrupt occurs if the LSI53C770 is not in target mode Command phase.

The DMA Byte Counter (DBC) register is also used during table indirect I/O SCRIPTS to hold the offset value.

Register: 0x27 (0x24)

DMA Command (DCMD)

Read/Write



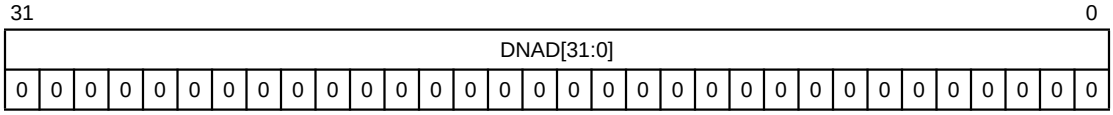
DCMD **DMA Command** **[7:0]**

This 8-bit register determines the instruction for the LSI53C770 to execute. This register has a different format for each instruction. For a complete description see Chapter 5, "Instruction Set of the I/O Processor."

Registers: 0x28–0x2B (0x28–0x2B)

DMA Next Data Address (DNAD)

Read/Write



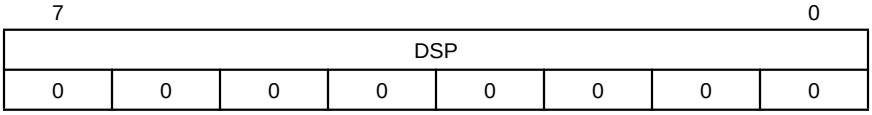
DNAD **DMA Next Data Address** **[31:0]**

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DMA SCRIPTS Pointer Save (DSPS) register. Its value may not be valid except in certain abort conditions.

Registers: 0x2C–0x2F (0x2C–0x2F)

DMA SCRIPTS Pointer (DSP)

Read/Write



DSP **DMA SCRIPTS Pointer** **[7:0]**

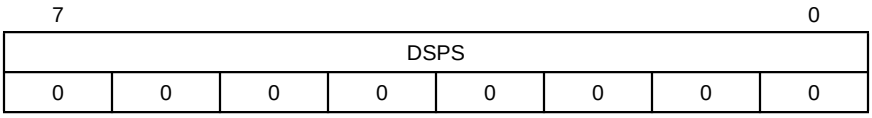
To execute SCSI SCRIPTS, the address of the first SCRIPTS instruction must be written to this register. In normal SCRIPTS operation, once the starting address of

the SCRIPT is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DMA SCRIPTS Pointer (DSP) register does not need to be written with the next address, but the Start DMA bit (bit 2, DMA Control (DCNTL) register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPTS instruction. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS routine.

Registers: 0x30–0x33 (0x30–0x33)

DMA SCRIPTS Pointer Save (DSPS)
Read/Write

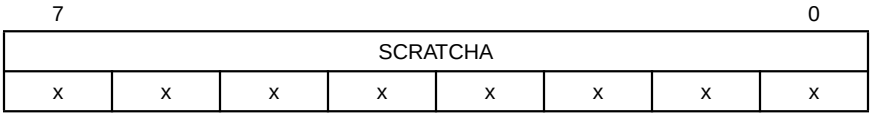


DSPS **DMA SCRIPTS Pointer Save** **[7:0]**

This register contains the second Dword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS Interrupt instruction is fetched, this register holds the interrupt vector.

Registers: 0x34–0x37 (0x34–0x37)

Scratch Register A (SCRATCHA)
Read/Write



SCRATCHA **SCRATCHA** **[7:0]**

This is a general purpose, user-definable scratch pad register. Normal SCRIPTS operations do not destroy the contents of this register. Only Register Read/Write and Memory Moves into the Scratch Register A (SCRATCHA) register alter its contents.

Note: The LSI53C770 cannot fetch SCRIPTS instructions from this location.

SCRIPTS programs may read or write individual bytes in this register by using the names SCRATCHA0 and SCRATCHA1.

When the internal SCRIPTS RAM is enabled using any of the three methods described in Chapter 2, and when bit 0 is set in the Chip Test Five (CTEST5) register, this register is shadowed to provide a base address for the SCRIPTS RAM. The shadowed version of this register allows the internal logic of the LSI53C770 to recognize the location of the SCRIPTS RAM in the system memory map. The contents of the Scratch Register A (SCRATCHA) register are preserved when shadowed.

Register: 0x38 (0x3B)

DMA Mode (DMODE)

Read/Write

7	6	5	4	3	2	1	0
BL[1:0]		FC[1:0]		PD	FAM	U0/TT0	MAN
0	0	0	0	0	0	0	0

BL[1:0] **Burst Length** **[7:6]**

These bits control the maximum number of bus cycles performed per bus ownership. The LSI53C770 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (Hold in Bus Modes 3 and 4) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. To perform cache line bursts, these bits must be set to 4, 8, or 16 transfers and cache bursting must be enabled (by clearing the CDIS bit, bit 7 in the Chip Test Zero (CTEST0) register).

The LSI53C770 inserts a “fairness delay” of exactly 5 CLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts. The fairness timer has been modified in the LSI53C770 to improve DMA transfer rates while still allowing other DMA masters to gain access to

the bus. In the LSI53C720, the fairness delay was 5–8 CLKs. In the LSI53C770, the fairness delay is fixed at 5 CLKs.

BL1	BL0	Burst Length
0	0	2 - Transfer Burst
0	1	4 - Transfer Burst
1	0	8 - Transfer Burst
1	1	16 - Transfer Burst

FC[1:0] **Function Code (Bus Modes 1, 3 and 4), or TM[2:1] Transfer Modifier (Bus Mode 2) [5:4]**

These bits, along with bit 6 in the DMA Control (DCNTL) register (Bus Mode), define the function of the FC[2:1]_TM[2:1] signals as illustrated in Table 4.6.

Table 4.6 FC[2:1], TM[2:1] Pin Function

DCNTL Bit 6	DMODE Bits [5:4]	FC[2:1]_TM[2:1] Pin Function
0 0 0 0	00 01 10 11	User defined. The value of bits [5:4] correspond directly to the signal pins (FC[2:1]_TM[2:1]). The values of these bits are asserted onto the device pins during bus mastership.
1 1 1 1	00 01 10 11	FC2_TM2 becomes a Preview of Address input signal used to tell the LSILSI53C770 that the system is ready for the next address value. FC1-TM1 is an output that is always asserted.

PD **Program/Data 3**

This bit affects the function of the FC0_TM0 pin. It works in conjunction with the Bus Mode bit (bit 6 of the DMA Control (DCNTL) register), as shown in Table 4.7. When the Bus Mode bit is not set, the LSI53C770 can store SCRIPTS routines and data in separate memory banks. When the Bus Mode bit is set, the LSI53C770 performs the same function as the DC/ signal that is commonly found in Intel processors.

FAM **Fixed Address Mode** **2**

When the Fixed Address Mode bit is set, the address pointer in the DMA Next Data Address (DNAD) register is disabled and does not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. The fixed address mode feature is used to transfer data to or from a fixed port address. This port width must be 32 bits and Dword aligned. Setting this bit does not affect SCRIPTS fetching instructions; only data transfer instructions are affected.

In fixed address mode, if a SCSI interrupt occurs while the LSI53C770 is receiving data, flush the data manually. Once the interrupt occurs (within the chip), the DMA FIFO Empty bit (bit 7 in the DMA Status (DSTAT) register) may not have been set when reading the DMA Status (DSTAT) register. At this point, the user may clear the DMA FIFO by writing to the Clear DMA FIFO bit (bit 2) in the Chip Test Three (CTEST3) register and setting the CSF (Clear SCSI FIFO) bit, bit 1 in the SCSI Test Register Three (STEST3) register. The Block Move instruction may now be restarted. Instead of clearing the FIFO, it may be flushed. This is done as follows: 1) reset the FAM bit; 2) load the DMA Next Data Address (DNAD) register with a valid memory address; 3) write to the Flush DMA FIFO bit (bit 3) in the Chip Test Three (CTEST3) register 4) set the FAM bit again. The Block Move instruction may now be restarted, assuming the byte count and address have been updated.

Table 4.7 FC0_TM0 Pin Function

DCNTL Bit 6	DMODE Bit 3	FC0_TM0 Pin Function
0	0	Driven HIGH when data is moved to or from memory.
0	1	Driven LOW when fetching instructions from memory. This is only done during instruction fetch cycles.
1	0	Driven HIGH when the LSI53C770 is bus master, indicating that data space is being accessed. When the LSI53C770 is not bus master, FC0_TM0 is 3-stated.
1	1	Driven LOW, indicating that control space is being accessed.

UO/TT0 **User Programmable Transfer Type** **1**

In all bus modes, UPSO-TT0/ is a general purpose output pin. The value in the register bit is asserted onto the UPSO-TT0/ pin while the LSI53C770 is a bus master. The TT1 bit is in Chip Test Zero (CTEST0).

MAN **Manual Start Mode** **0**

Setting this bit disables the LSI53C770 from automatically fetching and executing SCSI SCRIPTS after the DMA SCRIPTS Pointer (DSP) register is written. When the Start DMA bit in the DMA Control (DCNTL) register is cleared, the chip is running in normal mode. Once the Start DMA bit in the DMA Control (DCNTL) register is set, the LSI53C770 automatically fetches and executes each instruction. Clearing this bit causes the LSI53C770 to automatically fetch and execute SCSI SCRIPTS after the DMA SCRIPTS Pointer (DSP) register is written.

Register: 0x39 (0x3A)
DMA Interrupt Enable (DIEN)
Read/Write

7	6	5	4	3	2	1	0
R	HPED	BF	ABRT	SSI	SIR	WTD	IID
x	0	0	0	0	0	0	0

R **Reserved** **7**

HPED **Host Parity Error Detected During DMA Read or Slave Write** **6**

BF **Bus Fault** **5**

ABRT **Aborted** **4**

SSI **SCRIPTS Step Interrupt** **3**

SIR **SCRIPTS Interrupt Instruction Received** **2**

WTD **Watchdog Time-out Detected** **1**

IID **Illegal Instruction Detected** **0**

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the DMA Status (DSTAT) register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the DMA Status (DSTAT) register. Masking an interrupt does not prevent setting the DIP bit (bit 0 in the Interrupt Status (ISTAT) register). All DMA interrupts are considered fatal, therefore SCRIPTS stops running when a DMA interrupt occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

The IRQ/ output is latched. Once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

For more information on enabling interrupts, please refer to Chapter 2.

Register: 0x3A (0x39)

DMA Watchdog Timer (DWT)

Read/Write

7							0
DWT[7:0]							
0	0	0	0	0	0	0	0

DWT **DMA Watchdog Timer** **[7:0]**

The DMA watchdog timer register provides a time-out mechanism during data transfers between the LSI53C770 and memory. This register determines the amount of time that the LSI53C770 waits for the assertion of the STERM/-TA/-READYIN/ signal after starting a bus cycle. Write the time-out value to this register during initialization. Every time that the LSI53C770 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the time-out feature by writing 0x00 to this register.

The unit time base for this register is 32* BCLK input period. For example, at 50 MHz the time base for this register is 32 * 20 ns = 640 ns. If a time-out of 50 µs is desired, then this register should be loaded with a value of 0x4E.

The minimum time-out value that should be loaded into this register is 0x02. The value 0x01 does not provide a reliable time-out period.

Register: 0x3B (0x38)
DMA Control (DCNTL)
Read/Write

7	6	5	4	3	2	1	0
STE	BSM	EA	SSM	BW16	STD	FA	COM
0	0	0	0	0	0	0	0

STE **Size Throttle Enable** **7**
Asserting this bit causes the LSI53C770 to relinquish bus ownership every time the transfer size changes. When the size bits change from 01 (byte), 10 (word), or 00/11 (Dword), the LSI53C770 relinquishes the bus and attempts to complete the transfer in succeeding cycles. The chip powers up with this bit disabled. The bit is reset during a software or hardware reset. When cache line bursting is enabled, the LSI53C770 performs one transfer at a time until it reaches a cache line boundary. If this bit is set the snoop mode function of the SC0 pin, internal bus request, is not available.

BSM **Bus Mode** **6**
Setting this bit changes the function of the Function Code (FC[2:0]) or Transfer Modifier (TM[2:0]) pins. FC0_TM0 becomes a data control signal, FC1_TM1 becomes an output that is always asserted, and FC2_TM2 becomes an input to allow Preview of Address (PA/). For more information on the operation of this bit, refer to the descriptions of bits [5:3] in the DMA Mode (DMODE) register.

EA **Enable ACK** **5**
Setting this bit causes the STERM/ (TA/ in Bus Mode 2, ReadyIn/ in Bus Modes 3 and 4) pin to become bidirectional, so the LSI53C770 generates STERM/ during slave accesses. When this bit is clear, the LSI53C770 monitors STERM/ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the LSI53C770 if this feature is desired. This bit is not cleared with a software reset. Refer to the Bidirectional STERM/-TA/ section in Chapter 2, for more information on how this bit operates.

SSM **Single Step Mode** **4**

Setting this bit causes the LSI53C770 to stop after executing each SCRIPTS instruction, and generate a SCRIPTS step interrupt. When this bit is cleared the LSI53C770 does not stop after each instruction. It continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, keep this bit clear. To restart the LSI53C770 after it generates a SCRIPTS Step interrupt, read the Interrupt Status (ISTAT) and DMA Status (DSTAT) registers to clear the interrupt. Then set the START DMA bit in this register.

BW16 **Host Bus Width Equal to 16** **3**

When this bit is set, the LSI53C770 host interface becomes 16 bits wide. This bit can only be set in little endian mode. Data lines [31:16] must be tied to data lines [15:0], respectively. Cache bursting is not available in this mode.

STD **Start DMA Operation** **2**

The LSI53C770 fetches a SCSI SCRIPTS instruction from the address contained in the DMA SCRIPTS Pointer (DSP) register when this bit is set. This bit is required if the LSI53C770 is in one of the following modes:

- Manual start mode – Bit 0 in the DMA Mode (DMODE) register is set
- Single step mode – Bit 4 in the DMA Control (DCNTL) register is set

When the LSI53C770 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the LSI53C770 is in single step mode, set the Start DMA bit to restart execution of SCRIPTS after a single step interrupt.

FA **Fast Arbitration** **1**

When this bit is set, the LSI53C770 immediately becomes bus master after receiving a Bus Grant (HLDAI in Bus Modes 3 and 4), saving one clock cycle of arbitration time. When this bit is clear, the LSI53C770 follows the normal arbitration sequence.

COM **LSI53C700 Family Compatibility** **0**

When this bit is clear, the LSI53C770 behaves in a manner compatible with the LSI53C700 family. Selection/reselection IDs is stored in both the SCSI Selector ID Register (SSID) and SCSI First Byte Received (SFBR) registers.

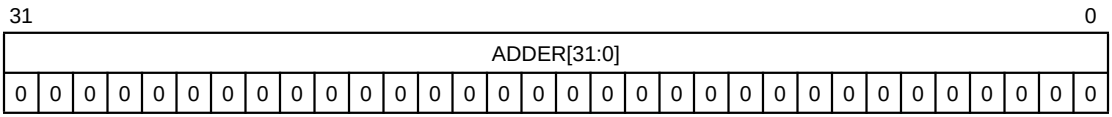
When this bit is set, the ID is stored only in the SCSI Selector ID Register (SSID) register, protecting the SFBR from being overwritten should a selection/reselection occur during a DMA register to register operation. The default condition of this bit (clear) causes the LSI53C770 to function the same as the LSI53C700.

Note: This bit is not cleared with a software reset.

Register: 0x3C–0x3F (0x3C–0x3F)

Adder Sum Output (ADDER)

Read Only



ADDER **Adder Sum Output** **[31:0]**

This register contains the output of the internal adder, and is used primarily for test purposes.

Register: 0x40 (0x43)

SCSI Interrupt Enable Zero (SIEN0)

Read/Write

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SCSI Interrupt Status Zero (SIST0) register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the SCSI Interrupt Status Zero (SIST0) register. Masking an interrupt does not prevent the ISTAT SIP bit from being set, except in the case of nonfatal interrupts (SEL, RSL, CMP, and M/A (target mode only)). Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked nonfatal interrupt does not prevent unmasked or fatal interrupts from getting through. Interrupt stacking does not begin until either the SIP (bit 1) or DIP (bit 0) bit in the Interrupt Status (ISTAT) register is set.

The LSI53C770 IRQ/ output is latched. Once asserted, it remains asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted does not cause IRQ/ to be deasserted. In the case of nonfatal interrupts, masking an interrupt after it occurs causes the SIP bit in the Interrupt Status (ISTAT) register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). Do not toggle the bits in this register on or off during normal operation. They should be set or cleared during the initialization routine.

For more information on interrupts, refer to Chapter 2, "Functional Description."

M/A **SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode** **7**

In initiator mode, this bit is set when the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SCSI Output Control Latch (SOCL) register. This expected phase is automatically written by SCSI SCRIPTS.

In target mode, this bit is set when the initiator has asserted ATN. See the Disable halt on parity error or ATN condition bit in the SCSI Control One (SCNTL1) register for more information on when this status is actually raised.

CMP **Function Complete** **6**

Indicates full arbitration and selection sequence is completed.

SEL **Selected** **5**

Indicates the LSI53C770 is selected as a SCSI target device. Set the Enable response to selection bit in the SCSI Chip ID (SCID) register for this to occur.

RSL **Reselected** **4**

The LSI53C770 has been reselected as a SCSI initiator device. The Enable response to reselection bit in the SCSI Chip ID (SCID) register must be set for this to occur.

SGE **SCSI Gross Error** **3**

The following conditions are considered SCSI Gross Errors:

- Data underflow – reading the SCSI FIFO when no data is present.
- Data overflow – writing to the SCSI FIFO while it is full.
- Offset underflow – receiving an ACK pulse in target mode before the corresponding REQ is sent.
- Offset overflow – receiving an REQ pulse in initiator mode and exceeding the maximum offset (defined by the MO[3:0] bits in the SCSI Transfer (SXFER) register).

- A phase change in initiator mode, with an outstanding REQ/ACK offset.
- Residual data in SCSI FIFO – starting a transfer other than synchronous data receive with data left in the SCSI synchronous receive FIFO.

UDC **Unexpected Disconnect** **2**

This condition only occurs in initiator mode. It happens when the target to which the LSI53C770 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCSI Control Register Two (SCNTL2) register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

RST **SCSI Reset Condition** **1**

Indicates assertion of the RST signal by the LSI53C770 or any other SCSI device. This condition is edge-triggered, so multiple interrupts cannot occur because of a single RST pulse.

PAR **SCSI Parity Error** **0**

Indicates detection by the LSI53C770 of a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCSI Control One (SCNTL1) register for more information on when this condition is actually raised.

Register: 0x41 (0x42)

SCSI Interrupt Enable One (SIEN1)

Read/Write

7				3	2	1	0
R					STO	GEN	HTH
x	x	x	x	x	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SCSI Interrupt Status One (SIST1) register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the SCSI Interrupt Status One (SIST1) register. Masking an interrupt does not prevent the

SIP bit (bit 1) in the Interrupt Status (ISTAT) register from being set. Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked nonfatal interrupt does not prevent unmasked or fatal interrupts from getting through. Interrupt stacking does not begin until either the DIP (bit 0) or SIP (bit 1) bit in the Interrupt Status (ISTAT) register is set.

The LSI53C770 IRQ/ output is latched. Once asserted, it remains asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted does not cause IRQ/ to be deasserted. In the case of nonfatal interrupts, masking an interrupt after it occurs causes the SIP bit (bit 1) in the Interrupt Status (ISTAT) register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). Do not toggle the bits in this register on or off during normal operation. They should be set or cleared during the initialization routine.

R	**Reserved**	**[7:3]**
STO	**Selection or Reselection Time-out** This bit is set when the SCSI device which the LSI53C770 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the SCSI Timer Register 0 (STIME0) register bits [3:0] for more information on the time-out timer.	**2**
GEN	**General Purpose Timer Expired** This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer Register One (STIME1) register, bits [3:0], for more information on the general purpose timer.	**1**
HTH	**Handshake-to-Handshake Timer Expired** This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request-to-Request (target) or Acknowledge-to-Acknowledge (initiator) period. See the description of the SCSI Timer Register 0 (STIME0) register, bits [7:4], for more information on the handshake-to-handshake timer.	**0**

Register: 0x42 (0x41)
SCSI Interrupt Status Zero (SIST0)
Read Only

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

Reading the SCSI Interrupt Status Zero (SIST0) register returns the status of the various interrupt conditions, whether they are enabled in the SCSI Interrupt Enable Zero (SIEN0) register or not. Each bit set indicates occurrence of the corresponding condition. Reading the SCSI Interrupt Status Zero (SIST0) clears the selected conditions. The SIP bit in the Interrupt Status (ISTAT) register will be cleared after both SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) are read.

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the LSI53C770 stacks interrupts). SCSI interrupt conditions are individually masked through the SCSI Interrupt Enable Zero (SIEN0) register.

When performing consecutive 8-bit reads of the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), and SCSI Interrupt Status One (SIST1) registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, read the SIST0 and SIST1 registers before the DSTAT register to avoid missing a SCSI interrupt. For more information on interrupts, refer to Chapter 2, "Functional Description."

M/A — **Initiator Mode: Phase Mismatch; Target Mode: ATN/ Active** — **7**

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode. It is set in low level mode any time there is a phase change.

CMP **Function Complete** **6**

This bit is set when full arbitration and selection sequence is completed.

SEL **Selected** **5**

This bit is set when the LSI53C770 is selected by another SCSI device. The Enable Response to Selection bit must be set in the SCSI Chip ID (SCID) register for the LSI53C770 to respond to selection attempts.

RSL **Reselected** **4**

This bit is set when the LSI53C770 is reselected by another SCSI device. The Enable Response to Reselection bit must be set in the SCSI Chip ID (SCID) register for the LSI53C770 to respond to reselection attempts.

SGE **SCSI Gross Error** **3**

This bit is set when the LSI53C770 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

- Data Underflow – reading the SCSI FIFO when no data is present.
- Data Overflow – writing too many bytes to the SCSI FIFO, or the synchronous offset causes overwriting the SCSI FIFO.
- Offset Underflow – the LSI53C770 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.
- Offset Overflow – the other SCSI device sends a REQ/ or ACK/ pulse with data which exceeds the maximum synchronous offset defined by the SCSI Transfer (SXFER) register.
- Residual data in the Synchronous data FIFO – a transfer other than synchronous data receive is started with data left in the synchronous data FIFO.
- A phase change occurred with an outstanding synchronous offset when the LSI53C770 is operating as an initiator.

UDC **Unexpected Disconnect** **2**

This bit is set when the LSI53C770 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the LSI53C770 operates in the initiator mode. When the LSI53C770 operates in low level mode, any disconnect causes an interrupt, even a valid SCSI disconnect.

This bit is also set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected interrupt).

RST **SCSI RST/ Received** **1**

This bit is set when the LSI53C770 detects an active RST/ signal, whether the reset was generated external to the chip or caused by the Assert RST/ bit in the SCSI Control One (SCNTL1) register. This SCSI reset detection logic is edge-sensitive, so that multiple interrupts are not generated for a single assertion of the SCSI RST/ signal.

PAR **Parity Error** **0**

This bit is set when the LSI53C770 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCSI Control Zero (SCNTL0) register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SCSI Output Data Latch (SODL) register. A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCSI Control Zero (SCNTL0) register = 1, bit 2 in the SCSI Control Zero (SCNTL0) register = 0).

Register: 0x43 (0x40)
SCSI Interrupt Status One (SIST1)
Read Only

7				3	2	1	0
R					STO	GEN	HTH
x	x	x	x	x	0	0	0

Reading the SCSI Interrupt Status One (SIST1) register returns the status of the various interrupt conditions, whether they are enabled in the SCSI Interrupt Enable One (SIEN1) register or not. Each bit that is set indicates an occurrence of the corresponding condition.

Reading this register resets the selected conditions, and resets the SCSI Interrupt Status One (SIST1) register. The SIP bit in the Interrupt Status (ISTAT) register is cleared after both SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) is read.

R **Reserved** **[7:3]**

STO **Selection or Reselection Time-out** **2**
This bit is set when the SCSI device which the LSI53C770 was attempting to select or reselect did not respond within the programmed time-out period (See the description of the SCSI Timer Register 0 (STIME0) register, bits [3:0], for more information on the time-out timer). After the LSI53C770 wins arbitration, it waits for selection or reselection to complete. While waiting, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register. The SCRIPTS routine then executes the next instruction before the selection has completed. The chip continues executing SCRIPTS until it encounters an interrupt, or a SCRIPTS instruction that requires it to respond. If time-out occurs and a block move instruction was loaded, FIFO needs to be flushed.

GEN **General Purpose Timer Expired** **1**
This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer Register One (STIME1) register, bits [3:0], for more information on the general purpose timer.

HTH **Handshake-to-Handshake Timer Expired** **0**
This bit is set when the handshake-to-handshake timer expires. The time measured is the SCSI Request-to-Request (target) or Acknowledge-to-Acknowledge (initiator) period. See the description of the SCSI Timer Register 0 (STIME0) register, bits [7:4], for more information on the handshake-to-handshake timer.

Register: 0x44 (0x47)
SCSI Longitudinal Parity (SLPAR)
Read/Write

7							0
SLPAR							
x	x	x	x	x	x	x	x

SLPAR **SCSI Longitudinal Parity** **[7:0]**
The SCSI Longitudinal Parity (SLPAR) register consists of two multiplexed bytes; other register bit settings determine what is displayed at this memory location at any given time. When bit 5 in the SCSI Control Register Two (SCNTL2) (SLPMD) register is cleared, the chip XORs the high and low bytes of the SCSI Longitudinal Parity (SLPAR) register together to give a single-byte value which is displayed in the SCSI Longitudinal Parity (SLPAR) register. If the SLPMD bit is set, then the SCSI Longitudinal Parity (SLPAR) register shows either the high byte or the low byte of the SLPAR word. The SLPAR High Byte Enable bit, SCSI Control Register Two (SCNTL2), bit 4, determines which byte of the SCSI Longitudinal Parity (SLPAR) register is visible on the SCSI Longitudinal Parity (SLPAR) register at any given time. If this bit is cleared, the SCSI Longitudinal Parity (SLPAR) register contains the low byte of the SLPAR word; if it is set, the SCSI Longitudinal Parity (SLPAR) register contains the high byte of the SLPAR word.

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example,

suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active HIGH):

Data/Check Bytes	Running SLPAR	Comments
–	00000000	SLPAR initialized to zero
11001100 (Data)	11001100)	XOR data byte with SLPAR, place result in SLPAR
01010101 (Data)	10011001	XOR data byte with SLPAR, place result in SLPAR
00001111 (Data)	10010110	XOR data byte with SLPAR, place result in SLPAR
10010110 (Check)	00000000	XOR check byte with SLPAR, place result in SLPAR. The result should be zeros; a one in any bit position indicates a transmission error.

The SCSI Longitudinal Parity (SLPAR) register is also used to generate the check bytes for SCSI send operations. If the SCSI Longitudinal Parity (SLPAR) register contains all zeros prior to sending a block move, it contains the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Note: Writing any value to this register clears it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances.

Register: 0x45 (0x46)
SCSI Wide Residue Data (SWIDE)
Read Only

7							0
SWIDE							
x	x	x	x	x	x	x	x

SWIDE **SCSI Wide Residue** **[7:0]**
After a wide SCSI data receive operation, this register contains a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte.

Register: 0x46 (0x45)
Memory Access Control (MACNTL)
Read/Write

7			4	3	2	1	0
TYP[3:0]				DataWR	DataRD	PSCRIPT	SCRIPT
x	x	x	x	0	0	0	0

MACNTL is used to determine if an external access is to local or far memory.

TYP[3:0] **Chip Type** **[7:4]**
These bits identify the chip type for software purposes.

Bits 7654	Chip Type
0000	LSI53C720
0001	LSI53C720SE
0010	LSI53C770

DataWR **Data Write** **3**
This bit is used to define if a data write s considered local memory access.

DataRD **Data Read** **2**
This bit is used to define if a data read is considered local memory access.

PSCRIPT **Pointer SCRIPTS** **1**
This bit is used to define if a pointer to a SCRIPTS indirect or table indirect fetch is considered local memory access.

SCRIPT **SCRIPTS** **0**
This bit is used to define if a SCRIPTS fetch is considered local memory access.

Register: 0x47 (0x44)

General Purpose Control (GPCNTL)
Read/Write

7		5	4	3	2	1	0
R			GPIO_en4	GPIO_en3	GPIO_en2	GPIO_en1	GPIO_en0
x	x	x	0	1	1	1	1

GPCNTL is used to determine if the pins controlled by the General Purpose Control (GPCNTL) register (GPREG, address 0x07 (0x04)) are inputs or outputs.

R **Reserved** **[7:5]**

GPIO_en4 **General Purpose Output Enable 4** **4**
GPCNTL, corresponding to bit 4 in the General Purpose (GPREG) register and pin 43, powers up as a general purpose output.

GPIO_en[3:0] **General Purpose Output Enable [3:0]** **[3:0]**
Bits [3:0] in GPCNTL, corresponding to bits [3:0] in the General Purpose (GPREG) register and pins 39–42, power up as general purpose inputs. If any of the bits are cleared, this indicates an output and if any of the bits are set this indicates an input. When the bits are enabled as inputs, an internal pull-up is also enabled.

Register: 0x48 (0x4B)

SCSI Timer Register 0 (STIME0)

Read/Write

7			4	3			0
HTH[3:0]				SEL[3:0]			
0	0	0	0	0	0	0	0

HTH **Handshake-to-Handshake Timer Period** **[7:4]**

These bits select handshake-to-handshake time-out period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SCSI Interrupt Status One (SIST1) register is set, and an interrupt is generated, if bit 0 in the SCSI Interrupt Enable One (SIEN1) register is set. The following table contains time-out periods for the Handshake-to-Handshake Timer and the General Purpose Timer (SCSI Timer Register One (STIME1) bits [3:0]).

HTH[7:4], GEN[3:0]	Minimum Time-out without scale factor bit set (50 MHz CLK)	Minimum Time-out with scale factor bit set (50 MHz CLK)
0000	Disabled	Disabled
0001	100 µs	1.6 ms
0010	200 µs	3.2 ms
0011	400 µs	6.4 ms
0100	800 µs	12.8 ms
0101	1.6 ms	25.6 ms
0110	3.2 ms	51.2 ms
0111	6.4 ms	102.4 ms
1000	12.8 ms	204.8 ms
1001	25.6 ms	409.6 ms
1010	51.2 ms	819.2 ms
1011	102.4 ms	1.6 s
1100	204.8 ms	3.2 s
1101	409.6 ms	6.4 s
1110	819.2 ms	12.8 s
1111	1.6 s	25.6 s

SEL **Selection Time-out Period** **[3:0]**
These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 sselection abort time) is exceeded, the STO bit in the SCSI Interrupt Status One (SIST1) register is set. An interrupt is optionally generated, if bit 2 in the SCSI Interrupt Enable One (SIEN1) register is set.

Register: 0x49 (0x4A)

SCSI Timer Register One (STIME1)
Read/Write

7	6	5	4	3			0
HTHBA		GENSF	HTHSF	GEN[3:0]			
0	0	0	0	0	0	0	0

HTHBA **Handshake-to-Handshake Timer Bus Activity Enable Bit** **[7:6]**
Setting this bit causes this timer to begin testing for SCSI request/acknowledge activity as soon as SCSI busy is asserted regardless of the agents participating in the transfer.

GENSF **General Purpose Timer Scale Factor Bit** **5**
Setting this bit causes this timer to shift by a factor of 16.

HTHSF **Handshake-to-Handshake Timer Scale Factor Bit** **4**
Setting this bit causes this timer to shift by a factor of 16.

GEN[3:0] **General Purpose Timer Period** **[3:0]**
These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SCSI Interrupt Status One (SIST1) register is set and an interrupt is optionally generated, if bit 1 in the SCSI Interrupt Enable One (SIEN1) register is set. Refer to the table under SCSI Timer Register 0 (STIME0), bits [3:0], for the available time-out periods.

Register: 0x4A (0x49)

Response ID Zero (RESPID0)

Read/Write

7							0
RESPID0							
x	x	x	x	x	x	x	x

RESPID0 **Response ID Zero** **[7:0]**

RESPID0 and Response ID One (RESPID1) contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of Response ID One (RESPID1) representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCSI Chip ID (SCID) register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the Response ID One (RESPID1) and Response ID Zero (RESPID0) registers. However, the chip can arbitrate with only one ID value in the SCSI Chip ID (SCID) register.

Register: 0x4B (0x48)

Response ID One (RESPID1)

Read/Write

15							8
RESPID1							
x	x	x	x	x	x	x	x

RESPID1 **Response ID One** **[15:8]**

RESPID0 and RESPID1 contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCSI Chip ID (SCID) register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the

Response ID One (RESPID1) and Response ID Zero (RESPID0) registers. However, the chip can arbitrate with only one ID value in the SCSI Chip ID (SCID) register.

Register: 0x4C (0x4F)

SCSI Test Register Zero (STEST0)
Read Only

7			4	3	2	1	0
SSAID				SLT	ART	SOZ	SOM
x	x	x	x	0	x	1	1

SSAID **SCSI Selected as ID** **[7:4]**
These bits are read only and contain 4 bits that encode the possible 0–15 IDs the LSI53C770 can be selected as. During the selection phase, when a valid ID is put on the bus, and the LSI53C770 responds to that ID as the ID it was selected as, this ID is written into the SCSI Selector ID Register (SSID) register.

SLT **Selection Response Logic Test** **3**
This bit is set when the LSI53C770 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

ART **Arbitration Priority Encoder Test** **2**
This bit is always set when the LSI53C770 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but may be used during low level mode operation to determine if the LSI53C770 has won arbitration.

SOZ **SCSI Synchronous Offset Zero** **1**
This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the LSI53C770, as an initiator, is waiting for the target to request data transfers. If the LSI53C770 is a target, then the initiator has sent the offset number of acknowledges.

SOM **SCSI Synchronous Offset Maximum** **0**

This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits [3:0] in the SCSI Transfer (SXFER) register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set the LSI53C770, as a target, is waiting for the initiator to acknowledge the data transfers. If the LSI53C770 is an initiator, then the target has sent the offset number of requests.

Register: 0x4D (0x4E)

SCSI Test Register One (STEST1)

Read Only

7			4	3	2	1	0
R				DBLEN	DBLSEL	SFP[1:0]	
x	x	x	x	0	0	x	x

R **Reserved** **[7:4]**

DBLEN **SCLK Doubler Enable** **3**

Set this bit to bring the SCSI clock doubler out of the powered down state. The default value of this bit is clear (SCSI clock doubler powered down). Set bit 2 after setting this bit, to double the SCLK frequency.

DBLSEL **SCLK Doubler Select** **2**

Set this bit after powering up the SCSI clock doubler to double the SCLK frequency. This bit has no effect unless bit 3 is set.

SFP[1:0] **SCSI FIFO Parity** **[1:0]**

These bits represent the parity that is read from the SCSI FIFO byte lanes during test access through the SCSI Output Data Latch (SODL) register. To read the SCSI FIFO in test mode, read these bits after reading the SCSI Output Data Latch (SODL) register. SFP1 represents parity for the most significant byte and SFP0 represents parity for the least significant byte. See the description of the SCSI FIFO Test Mode bit in the SCSI Test Register Three (STEST3) register for more information on testing the SCSI FIFO.

Doubling the SCSI CLK Frequency – The LSI53C770 SCSI clock doubler doubles a 40–50 MHz SCSI clock, increasing the frequency to 80–100 MHz. Follow these steps to use the clock doubler:

1. Set the SCLK Doubler Enable bit (SCSI Test Register One (STEST1), bit 3).
2. Wait 20 µs.
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (SCSI Test Register Three (STEST3), bit 5).
4. Set the clock conversion factor using the SCF and CCF fields in the SCSI Control Three (SCNTL3) register.
5. Set the SCLK Doubler Select bit (SCSI Test Register One (STEST1), bit 2).
6. Clear the Halt SCSI Clock bit.

Register: 0x4E (0x4D)
SCSI Test Register Two (STEST2)
Read/Write

7	6	5	4	3	2	1	0
SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
0	0	0	0	0	0	0	0

SCE **SCSI Control Enable** **7**

Setting this bit allows assertion of all SCSI control and data lines through the SCSI Output Control Latch (SOCL) and SCSI Output Data Latch (SODL) registers regardless of whether the LSI53C770 is configured as a target or initiator.

Do not set this bit during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

ROF **Reset SCSI Offset** **6**

Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. Set this bit if a SCSI gross error condition occurs to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

DIF **SCSI Differential Mode** **5**

Setting this bit allows the LSI53C770 to interface to external differential transceivers. Its only real effect is to 3-state the BSY/, SEL/, and RST/ pads so that they can be used as pure inputs. Clearing this bit enables SE mode operation. Set this bit the initialization routine if the differential pair interface is used.

SLB **SCSI Loopback Mode** **4**

Setting this bit allows the LSI53C770 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

SZM **SCSI High Impedance Mode** **3**

Setting this bit places all the open drain 48 mA SCSI drivers into a high impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

AWS **Always Wide SCSI** **2**

When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. Normally, deassert this bit since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI specifications.

EXT **Extend REQ/ACK Filtering** **1**

The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which causes glitches on deasserting edges to be disregarded. Asserting this bit increases the filtering period from 30 ns to 60 ns on the deasserting edge of the REQ/ and ACK/ signals.

Note: Never set this bit during fast SCSI (> 5 M transfers per second) operations, because a valid assertion could be treated as a glitch.

LOW **SCSI Low level Mode** **0**

Setting this bit places the LSI53C770 in low level mode. In this mode, no DMA operations occur, and no SCRIPTS instructions execute. Arbitration and selection may be performed by setting the start sequence bit as described in the SCSI Control Zero (SCNTL0) register. SCSI bus

transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers (SCSI Output Data Latch (SODL), SCSI Bus Control Lines (SBCL), and input registers). This bit must be clear for the chip to properly respond to selection or reselection.

Register: 0x4F (0x4C)

SCSI Test Register Three (STEST3)

Read/Write

7	6	5	4	3	2	1	0
TE	STR	HSC	DSI	S16	TTM	CSF	STW
x	x	0	0	0	0	0	0

TE **TolerANT Enable** **7**

Setting this bit enables the Active Negation of TolerANT technology. Active Negation causes the SCSI Request, Acknowledge, Data, and parity signals to be actively deasserted, instead of relying on external pull-ups, when the LSI53C770 is driving these signals. Active deassertion of these signals occurs only when the LSI53C770 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and deassertion times. Active Negation is disabled after reset, or when this bit is cleared.

STR **SCSI FIFO Test Read** **6**

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO is easily read. Reading the least significant byte of the SCSI Output Data Latch (SODL) register causes the FIFO to unload. The functions are summarized in the table below.

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	[15:0]	Unload
SODL0	Read	[7:0]	Unload
SODL1	Read	[15:8]	None

HSC **Halt SCSI Clock** **5**

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit is used for test purposes or to lower I_{DD} during a power-down mode.

DSI **Disable Single Initiator Response** **4**

If this bit is set, the LSI53C770 ignores all bus-initiated selection attempts which employ the single initiator option from SCSI-1. In order to select the LSI53C770 while this bit is set, the LSI53C770's SCSI ID and the initiator's SCSI ID must both be asserted. Assert this bit in SCSI-2 systems so that a single bit error on the SCSI bus is not interpreted as a single initiator response. This bit works in conjunction with the VAL bit in the SCSI Selector ID Register (SSID) register.

S16 **16-Bit System** **3**

If this bit is set, all devices in the SCSI system implementation are assumed to be 16-bit. This causes the LSI53C770 to always check the parity bit for SCSI IDs [15:8] during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the LSI53C770 while this bit is set, the LSI53C770 will ignore the selection attempt, because the parity bit for IDs [15:8] will be undriven. See the description of the Enable Parity Checking bit in the SCSI Control Zero (SCNTL0) register for more information.

TTM **Timer Test Mode** **2**

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective

bits in the SCSI Interrupt Enable One (SIEN1) register are asserted, the LSI53C770 generates interrupts at time-out.

CSF **Clear SCSI FIFO** **1**

Setting this bit causes the “full flags” for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-clearing. The SIDL, SODL, and SODR Least and Most Significant Byte Full bits in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers are cleared.

STW **SCSI FIFO Test Write** **0**

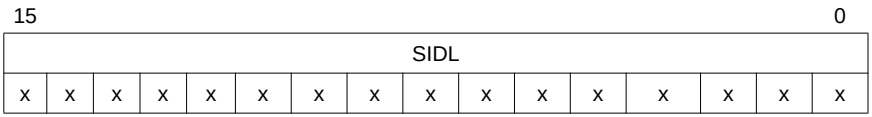
Setting this bit places the SCSI core into a test mode in which the FIFO can be easily read and written. While this bit is set, writes to the least significant byte of the SCSI Output Data Latch (SODL) register causes the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the SCSI Output Data Latch (SODL) register causes the FIFO to load. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Write	[15:0]	Load
SODL0	Write	[7:0]	Load
SODL1	Write	[15:8]	None

Registers: 0x50–0x51 (0x52–0x53)

SCSI Input Data Latch (SIDL)

Read Only



SIDL **SCSI Input Data Latch** **[15:0]**

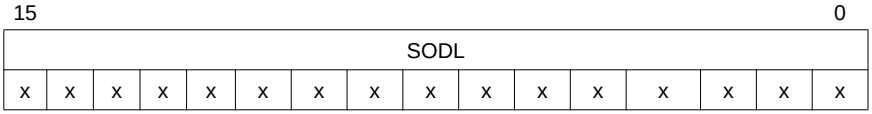
This register is used primarily for diagnostic testing, programmed I/O operation, or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SCSI Output Data Latch (SODL) register and then read back into the

LSI53C770 by reading this register to allow loopback testing. When receiving SCSI data, the data flows into this register and out to the host FIFO. This register differs from the SCSI Bus Data Lines (SBDL) register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and causes a parity error interrupt if the data is not valid.

Registers: 0x54–0x55 (0x56–0x57)

SCSI Output Data Latch (SODL)

Read/Write



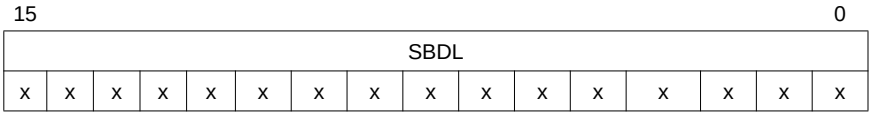
SODL **SCSI Output Data Latch** **[15:0]**

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCSI Control One (SCNTL1) register. This register is used to send data using programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Registers: 0x58–0x59 (0x5A–0x5B)

SCSI Bus Data Lines (SBDL)

Read Only



SBDL **SCSI Bus Data Lines** **[15:0]**

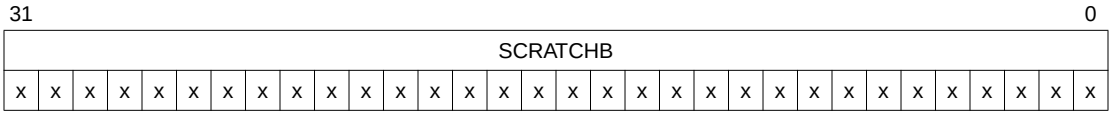
This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the

time the register is read. This register is used when receiving data using programmed I/O. This register can also be used for diagnostic testing or in low level mode.

Registers: 0x5C–0x5F

Scratch Register B (SCRATCHB)

Read/Write



SCRATCHB **Scratch Register B** **[31:0]**

This is a general purpose, user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the Scratch Register B (SCRATCHB) register will alter its contents.

Note: The LSI53C770 cannot fetch SCRIPTS instructions from this location.

If the internal SCRIPTS RAM is enabled using the indexed addressing method, a shadowed version of this register is used to address 128 blocks of 32-byte segments of the SCRIPTS RAM. Each 32-byte block of data is loaded into the Scratch Registers C–J (SCRATCHC–J) registers.

Registers: 0x60–0x7F

Scratch Registers C–J (SCRATCHC–J)

Read/Modify/Write

These are general purpose, user-definable scratch pad registers. They are accessible through read/modify/write instructions and are defined as Scratch Registers C–J (SCRATCHC–J).

Note: The LSI53C770 cannot fetch SCRIPTS instructions from this location.

When the indexed addressing method is used to enable and access the internal SCRIPTS RAM, the SCRIPTS RAM replaces these registers and can optionally be used as a block of scratchpad RAM. For more information on this and other methods of implementing the SCRIPTS RAM, see Chapter 2.

Chapter 5
Instruction Set of the I/O Processor

This chapter provides a high-level overview of the SCSI instruction types supported by LSI Logic SCSI SCRIPTS and the LSI53C770. This chapter contains the following sections:

5.1 SCSI SCRIPTS

After power up and initialization of the LSI53C770, the chip may operate with a low level register interface or in SCSI SCRIPTS mode. With the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip operates much like an LSI53C80 when in low level mode. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface provides backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip’s pins.

To operate in the SCSI SCRIPTS mode, the LSI53C770 requires only a SCRIPTS start address. All commands are fetched from local or external memory. The LSI53C770 fetches and executes its own instructions by

becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the LSI53C770 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer (DSP) register to restart the automatic fetching and execution of instructions.

The SCSI SCRIPTS mode of execution allows the LSI53C770 to make decisions based on the status of the SCSI bus, which offloads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI oriented features included in the instruction set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of SCSI SCRIPTS instructions are implemented in the LSI53C770:

- Block Move
- I/O or Read/Write
- Transfer Control
- Memory Move

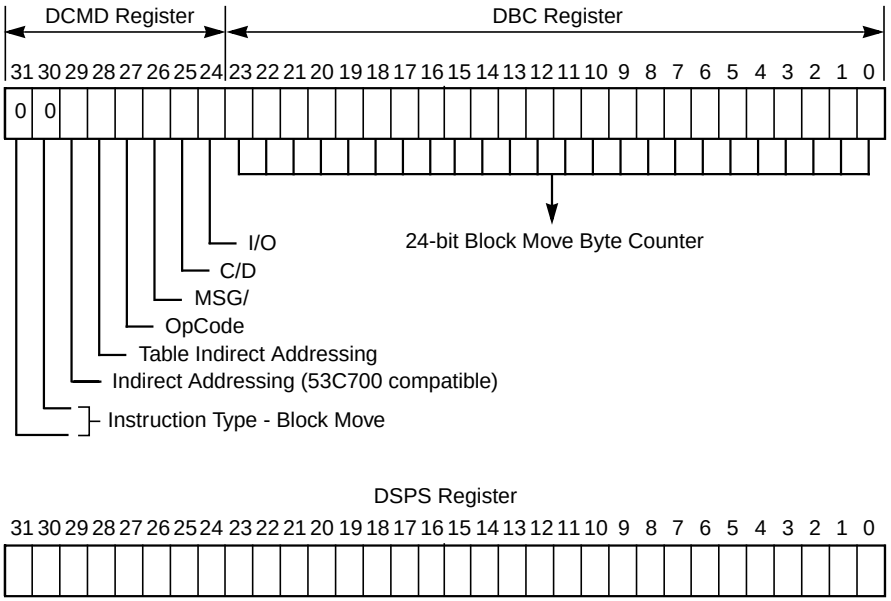
Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DMA Command (DCMD) and DMA Byte Counter (DBC) registers, the second into the DMA SCRIPTS Pointer Save (DSPS) register. The third word, used only by Memory Move instructions, is loaded into the Temporary Stack (TEMP) register.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any Dword boundary and can cross system segment boundaries. There are two restrictions on the placement of data in system memory: the eight bytes of data in the command must be contiguous; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

5.2 Block Move Instruction

Figure 5.1 describes the Block Move Instruction register.

Figure 5.1 Block Move Instruction Register



5.2.1 First Dword

Block Move Instruction **[31:30]**
A value of 00 in the two high order bits of the DMA Command (DCMD) register indicates the Block Move instruction type.

Indirect Addressing **29**
When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the DMA Next Data Address (DNAD) register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer

address. The value at the 32-bit start address is loaded into the chip's DMA Next Data Address (DNAD) register using a third long word fetch (4-byte transfer across the host computer bus).

Direct Addressing

The byte count and absolute address are:

Command	Byte Count
Address of Data	

Indirect Addressing

Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DMA Byte Counter (DBC) register and the data address is fetched from the DMA SCRIPTS Pointer Save (DSPS) register.

Command	Byte Count
Address of Pointer to Data	

Once the data buffer address is loaded, it is executed as if the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the LSI Logic SCSI SCRIPTS compiler, the address is placed in the SCRIPTS program at compile time. Then at the actual data transfer time, the chip fetches a Dword from the address specified in the program and writes this value to the DMA SCRIPTS Pointer Save (DSPS) register. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Table Indirect Addressing **28**
When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the Data Structure Address (DSA) register. Both the transfer count and the source/ destination address are fetched from this address.

Table Indirect
Use the signed integer offset in bits [23:0] of the second Dwords of the instruction to fetch first the byte count and then the data address. The signed value is combined with

the data structure base address to generate the physical address used to fetch values from the data structure. Sign extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
xx	Table Offset

Prior to the start of an I/O, the Data Structure Address (DSA) register must be loaded with the base address of the I/O data structure. The address may be any Dword on a Dword boundary.

At the start of an I/O, the Data Structure Address (DSA) is added to the 24-bit signed table offset value from the opcode to generate the address of the table entry; both positive and negative offsets are allowed. A subsequent fetch from this address brings the byte counts and buffer addresses into the chip.

OpCode **27**

This 1-bit field defines the instruction to be executed, either a block move (MOVE) or a chained block move (CHMOV). The OpCode Field bit has different meaning depending on whether the LSI53C770 is operating in Initiator or Target mode. If the OpCode bit is asserted (target mode) or deasserted (initiator mode) during a chained block move instruction, the corresponding bit in the SCSI Control Register Two (SCNTL2) register (SCNTL bit 6) is asserted. The OpCode bit and the SCSI Control Register Two (SCNTL2) bit are cleared once a block move instruction is executed.

Target Mode

In Target mode, the Opcode bit defines the following operations:

OPC	Instruction Defined
0	MOVE
1	Reserved

These instructions perform the following steps:

1. The LSI53C770 verifies that it is connected to the SCSI bus as a Target before executing this instruction.
2. The LSI53C770 asserts the SCSI phase signals (MSG/, C_D/, and I_O/) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the Command phase, the LSI53C770 receives the first command byte and decodes its SCSI Group Code.
   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the LSI53C770 overwrites the DMA Byte Counter (DBC) register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b) If any other Group Code is received, the DMA Byte Counter (DBC) register is not modified and the LSI53C770 requests the number of bytes specified in the DMA Byte Counter (DBC) register. If the DMA Byte Counter (DBC) register contains 0x000000 an illegal instruction interrupt is generated.
4. The LSI53C770 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address specified in the DMA Next Data Address (DNAD) register. If the OpCode bit is set and a data transfer ends on an odd byte boundary, the LSI53C770 stores the last byte in the SCSI Wide Residue Data (SWIDE) register during a receive operation or in the SCSI Output Data Latch (SODL) register during a send operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 5.2.
5. If the SCSI ATN/ signal is asserted by the Initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCSI Control One (SCNTL1) register controls whether an interrupt is generated.

   Initiator Mode

   In Target mode, the Opcode bit defines the following operations:

OPC	Instruction Defined
0	CHMOV
1	MOVE

These instructions perform the following steps:

1. The LSI53C770 verifies that it is connected to the SCSI bus as an Initiator before executing this instruction.
2. The LSI53C770 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the LSI53C770 has not yet transferred data by responding with an ACK/.
3. The LSI53C770 compares the SCSI phase bits in the DMA Command (DCMD) register with the latched SCSI phase lines stored in the SCSI Status One (SSTAT1) register. These phase lines are latched when REQ/ is asserted.
4. If the SCSI phase bits match the value stored in the SCSI Status One (SSTAT1) register, the LSI53C770 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address pointed to by the DMA Next Data Address (DNAD) register. If the opcode bit is cleared and a data transfer ends on an odd byte boundary, the LSI53C770 will be stored the last byte in the SCSI Wide Residue Data (SWIDE) register during a receive operation, or in the SCSI Output Data Latch (SODL) register during a send operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can complete. See Figure 5.2.
5. If the SCSI phase bits do not match the value stored in the SCSI Status One (SSTAT1) register, the LSI53C770 generates a phase mismatch interrupt and the command is not executed.
6. During a Message-Out phase, after the LSI53C770 has performed a select with Attention, the LSI53C770 deasserts ATN/ during the final REQ/ACK handshake.

7. When the LSI53C770 is performing a block move for Message In phase, it does not deassert the ACK/ signal for the last REQ/ACK handshake. The ACK signal must be cleared using the Clear ACK I/O instruction.

SCSI Phase **[26:24]**

This 3-bit field defines the desired SCSI information transfer phase. When the LSI53C770 operates in Initiator mode, these bits are compared with the latched SCSI phase bits in the SCSI Status One (SSTAT1) register. When the LSI53C770 operates in Target mode, the LSI53C770 asserts the phase defined in this field. Table 5.1 describes the possible combinations and the corresponding SCSI phase.

Table 5.1 SCSI Information Transfer Phase

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message out
1	1	1	Message in

Transfer Counter **[23:0]**

A 24-bit field specifying the number of data bytes to be moved between the LSI53C770 and system memory. The field is stored in the DMA Byte Counter (DBC) register. When the LSI53C770 transfers data to/from memory, the DMA Byte Counter (DBC) register is decremented by the number of bytes transferred. In addition, the DMA Next Data Address (DNAD) register is incremented by the number of bytes transferred. This process is repeated until the DMA Byte Counter (DBC) register is decremented to zero. At that time, the LSI53C770 fetches the next instruction.

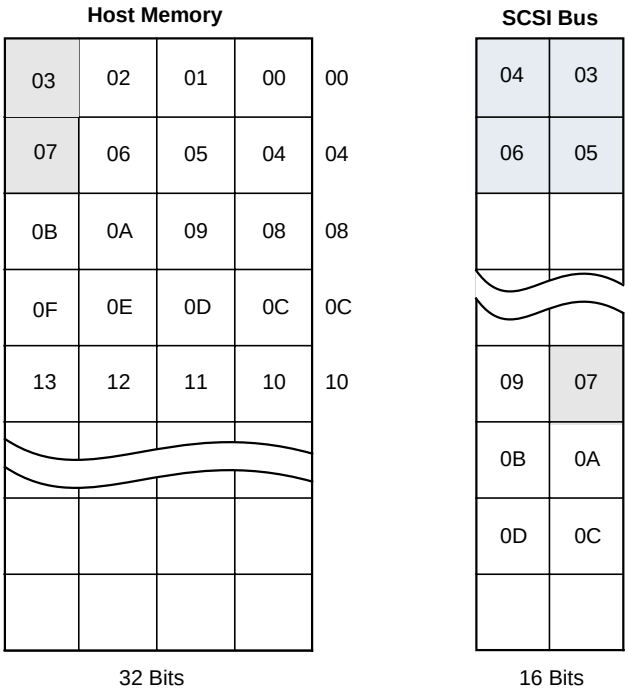
5.2.2 Second Dword

Start Address **[31:0]**

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DMA Next Data Address (DNAD) register. When the LSI53C770 transfers data to or from memory, the DMA Next Data Address (DNAD) register is incremented by the number of bytes transferred.

Figure 5.2 describes the Block Move and Chained Block Move Instructions.

Figure 5.2 Block Move and Chained Block Move Instructions



5.3 I/O Instructions

5.3.1 First Dword

I/O Instruction **[31:30]**

OpCode **[29:27]**

The following OpCode Field bits have different meanings, depending on whether the LSI53C770 is operating in initiator or target mode. The following opcodes determine if the instruction is a Read/Write or an I/O instruction. Opcode bit configurations (101, 110, and 111) are considered Read/Write instructions, and are described in Section 5.4, "Read/Write Instructions." This section describes Target mode operations.

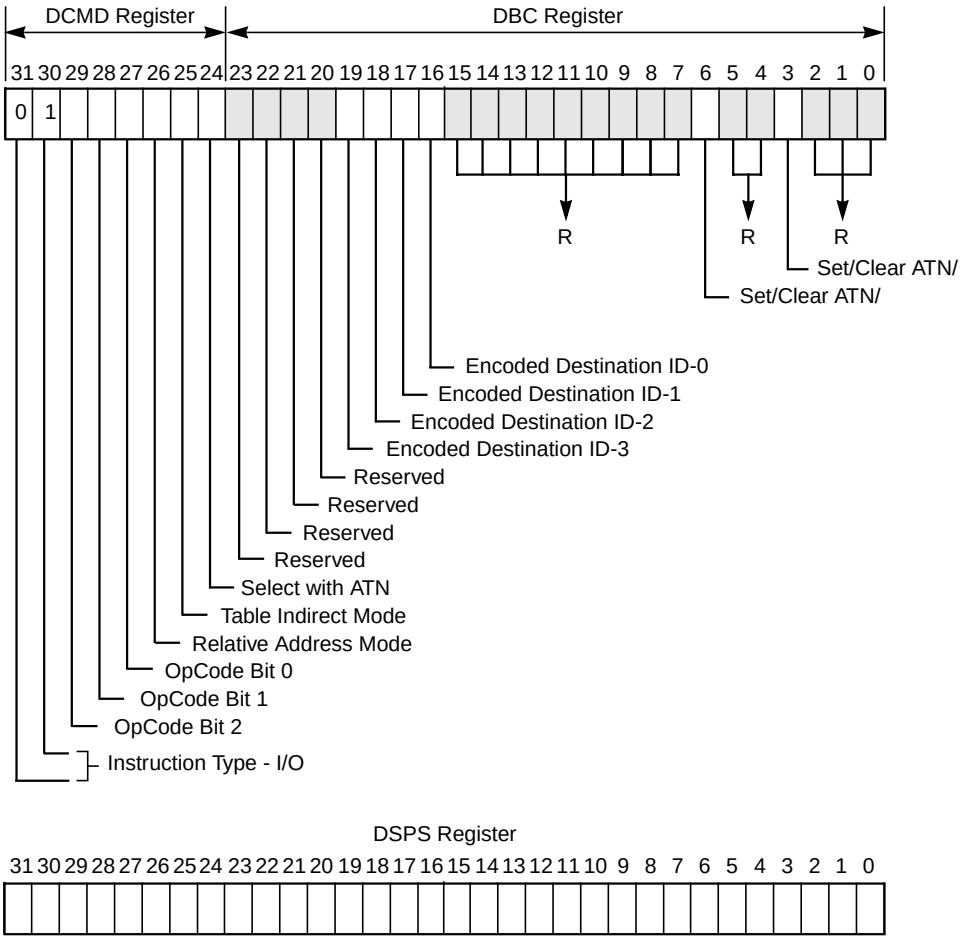
Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction (Target only)

The LSI53C770 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If it loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.

Figure 5.3 I/O Instruction Register



If the LSI53C770 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the LSI53C770 wins arbitration, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.

If the LSI53C770 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. Manually set the LSI53C770 to Initiator mode if it is reselected, or to Target mode if it is selected.

Disconnect Instruction (Target only)
The LSI53C770 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction
If the LSI53C770 is selected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.

If reselected, the LSI53C770 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. Manually set the LSI53C770 to Initiator mode when reselected.

If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the LSI53C770 aborts the Wait Select instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register.

Set Instruction
When the ACK/ or ATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. Do not set ACK/ or ATN/ except for testing purposes. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set. When the carry bit is set the corresponding bit in the ALU is set.

Note: None of the signals are set on the SCSI bus in target mode.

Clear Instruction
When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: None of the signals are reset on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

The LSI53C770 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If the LSI53C770 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.

If the LSI53C770 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register. This fetch can occur before the target responds to selection.

If the LSI53C770 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. Manually set the LSI53C770 to Initiator mode if it is reselected, or to Target mode if it is selected.

If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

The LSI53C770 waits for the Target to perform a disconnect from the SCSI bus. A disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (800 ns).

Wait Reselect Instruction

If the LSI53C770 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. Manually set the LSI53C770 Target mode when selected.

If the LSI53C770 is reselected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.

If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the LSI53C770 aborts the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register.

Set Instruction
When the ACK/ or ATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set.

Clear Instruction
When the ACK/ or ATN/ bits are cleared, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is cleared.

Relative Addressing Mode 26
When this bit is set, the 24-bit signed value in the DMA Next Data Address (DNAD) register is used as a relative displacement from the current DMA SCRIPTS Pointer (DSP) address.

Use this bit only in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Table Indirect Mode 25
When this bit is set, the 24-bit signed value in the DMA Byte Counter (DBC) register is used as an offset relative to the value in the Data Structure Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, load the DSA with the base address of the I/O data structure. Any address on a Dword boundary is allowed. At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data. Both positive and negative

offsets are allowed. A subsequent fetch from that address brings the data values into the chip. SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any Dword boundary and can cross system segment boundaries. There are two restrictions on the placement of data in system memory.

- The I/O data structure must lie within the 8 Mbyte above or below the base address.
- An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SCSI Transfer (SXFER) register. The configuration bits are ordered as in the SCSI Control Three (SCNTL3) register.

Config	ID	Offset/period	00

Use this bit in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Use bits 25 and 26 individually or in combination to produce the following combinations:

Bit 25	Bit 26	Addressing Mode
0	0	Direct
0	1	Table Indirect
1	0	Relative
1	1	Table Relative

Direct

Uses the device ID and physical address in the instruction.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect

Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative

Uses the device ID in the instruction, but treats the alternate address as a relative jump.

Command	ID	Not Used	Not Used
xx	Alternate Jump Offset		

Table Relative

Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. The value in bits [23:0] of the first four bytes of the SCRIPTS instruction is added to the data structure base address to form the fetch address.

Command	Table Offset
xx	Alternate Jump Offset

Select with ATN/ **24**

This bit specifies whether ATN/ is asserted during the selection phase when the LSI53C770 is executing a Select instruction. When operating in Initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Reserved **[23:20]**

Encoded SCSI Destination ID **[19:16]**

This 4-bit field specifies the destination SCSI ID for an I/O instruction.

Set/Clear Carry **10**

This bit is used in conjunction with a Set or Clear instruction to set or clear the Carry bit.

Set/Clear Target Mode **9**

This bit is used in conjunction with a Set or Clear instruction to set or clear Target mode. Setting this bit

with a Set command configures the LSI53C770 as a target device (this sets bit 0 of the SCSI Control Zero (SCNTL0) register). Clearing this bit with a Clear instruction configures the chip as an Initiator device.

Set/Clear ACK/ **6**

Set/Clear ATN/ **3**
These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal. Bit 3 controls the SCSI ATN/ signal.

Setting either of these bits sets or resets the corresponding bit in the SCSI Output Control Latch (SOCL) register, depending on the command used. The Set instruction is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear instruction is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are Initiator signals, they are not asserted on the SCSI bus unless the LSI53C770 is operating as an Initiator or the SCSI Loopback Enable bit is set in the SCSI Test Register Two (STEST2) register.

The Set/Clear SCSI ACK/ATN instruction is used after message phase Block Move operations to give the Initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the Initiator wishes to reject a message, it issues an Assert SCSI ATN instruction before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

5.3.2 Second Dword

Jump Address **[31:0]**
This 32-bit field specifies the address of the instruction to fetch when the LSI53C770 encounters a jump condition. The LSI53C770 fetches instructions from the address pointed to by this field whenever the LSI53C770 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a Select instruction in initiator mode, if the LSI53C770 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

5.4 Read/Write Instructions

The Read/Write instruction supports addition, subtraction, and comparison of two separate values within the chip. It performs the desired operation on the specified register and the SCSI First Byte Received (SFBR) register, then stores the result back to the specified register or SFBR.

The opcode bits determine if the instruction is a Read/Write or an I/O instruction. Opcode bit configurations (000, 001, 010, 011, and 100) are considered I/O instructions, and are described in Section 5.3, "I/O Instructions."

5.4.1 First Dword

Read/Write Instruction **[31:30]**

Opcode **[29:27]**
The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Opcodes 000 through 100 are considered I/O instructions.

Operator **[26:24]**

These bits are used in conjunction with the opcode bits to determine which instruction is currently selected. Refer to Table 5.2 for field definitions.

Bit 24, which in earlier versions of the LSI53C770 was Carry Enable, is now included with the Operator bits.

Figure 5.4 Read/Write Instruction Register

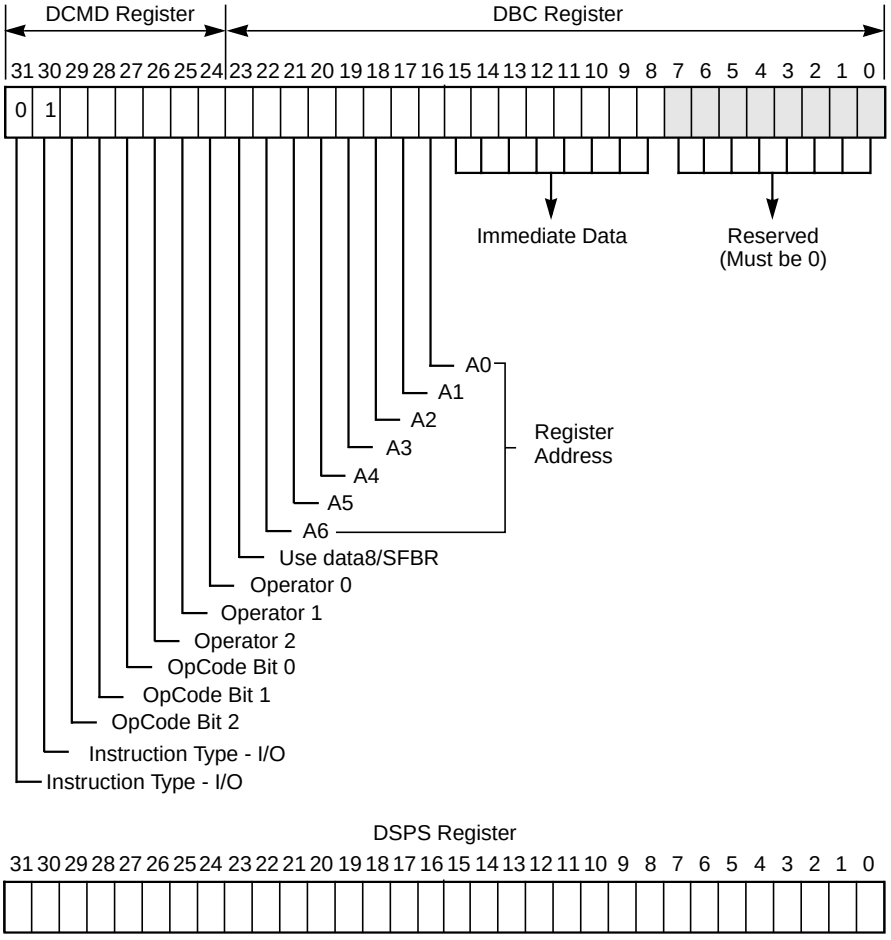


Table 5.2 Read/Write Instructions

Operator Bits [26:24]	Opcode 111 Read-Modify-Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
000	Move data into register. Syntax: “Move data8 to RegA”	Move data into SCSI First Byte Received (SFBR) register. Syntax: “Move data8 to SFBR”	Move data into register. Syntax: “Move data8 to RegA”
001	Shift register one bit to the left and place the result in the same register. Syntax: “Move RegA SHL RegA”	Shift register one bit to the left and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA SHL SFBR”	Shift the SCSI First Byte Received (SFBR) register one bit to the left and place the result in the register. Syntax: “Move SFBR SHL RegA”
010	OR data with register and place the result in the same register. Syntax: “Move RegA | data8 to RegA”	OR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA | data8 to SFBR”	OR data with SFBR and place the result in the register. Syntax: “Move SFBR | data8 to RegA”
011	XOR data with register and place the result in the same register. Syntax: “Move RegA XOR data8 to RegA”	XOR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA XOR data8 to SFBR”	XOR data with SFBR and place the result in the register. Syntax: “Move SFBR XOR data8 to RegA”
100	AND data with register and place the result in the same register. Syntax: “Move RegA & data8 to RegA”	AND data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA & data8 to SFBR”	AND data with SFBR and place the result in the register. Syntax: “Move SFBR & data8 to RegA”
101[1]	Shift register one bit to the right and place the result in the same register. Syntax: “Move RegA SHR RegA”	Shift register one bit to the right and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA SHR SFBR”	Shift the SCSI First Byte Received (SFBR) register one bit to the right and place the result in the register. Syntax: “Move SFBR SHR RegA”

Table 5.2 Read/Write Instructions (Cont.)

Operator Bits [26:24]	Opcode 111 Read-Modify-Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
110	Add data to register without carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA”	Add data to register without carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA + data8 to SFBR”	Add data to SFBR without carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA”
111	Add data to register with carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA with carry”	Add data to register with carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA + data8 to SFBR with carry”	Add data to SFBR with carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA with carry”

1. Data is shifted through the Carry bit and the Carry bit is shifted into the data byte.

Miscellaneous notes:

Substitute the desired register name or address for “RegA” in the syntax examples.
data8 indicates eight bits of data.
Use SFBR instead of data8 to add two register values.

Use data8/SFBR **23**

When this bit is set, SCSI First Byte Received (SFBR) is used instead of the data8 value during a Read-Modify-Write instruction (see Table 5.2). This allows the user to operate on two register values.

Register Address A[6:0] **[22:16]**

Register values are changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A[6:0] select an 8-bit source/destination register within the LSI53C770. Register addresses are always little endian addresses.

Immediate Data **[15:8]**

Reserved **[7:0]**

5.4.1.1 Read-Modify-Write Cycles

During these cycles the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation is used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Subtraction is not available when SFBR is used instead of data8 in the instruction syntax. To subtract one value from another when using SFBR, first XOR the value to subtract (subtrahend) with 0xFF, and add 1 to the resulting value. This creates the 2's complement of the subtrahend. The two values are added to obtain the difference of the original two values.

5.4.1.2 Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SCSI First Byte Received (SFBR). The possible functions of this instruction are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SCSI First Byte Received (SFBR) from/to any other register.
- Alter the value of a register with AND, OR, or ADD operators.
- After moving values to the SFBR, the compare and jump, call, or similar commands may are used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR is used to perform a register-to-register move.

5.5 Transfer Control Instructions

5.5.1 First Dword

Transfer Control Instruction **[31:30]**

OpCode **[29:27]**
This 3-bit field specifies the type of Transfer Control instruction execute. All Transfer Control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the

Data Compare field. Each instruction can operate in Initiator or Target mode. Transfer Control Instructions are shown in Table 5.3.

Table 5.3 Transfer Control Instructions

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	x	x	Reserved

Jump Instruction

The LSI53C770 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields.

If the comparisons are true, then it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register. The DMA SCRIPTS Pointer (DSP) register now contains the address of the next instruction.

If the comparisons are false, the LSI53C770 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register, leaving the instruction pointer unchanged.

Call Instruction

The LSI53C770 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

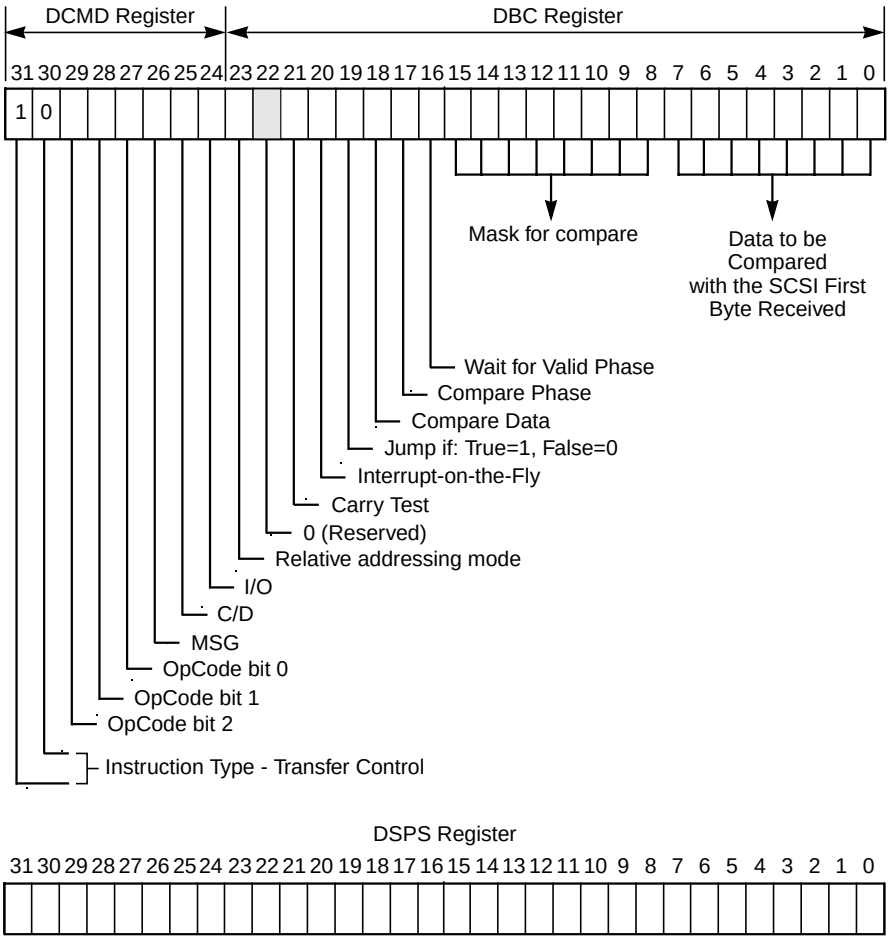
If the comparisons are true, then it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register and that address value becomes the address of the next instruction.

When the LSI53C770 executes a Call instruction, the instruction pointer contained in the DMA SCRIPTS Pointer (DSP) register is stored in the Temporary Stack (TEMP) register.

When a Return instruction is executed, the value stored in the Temporary Stack (TEMP) register is returned to the DMA SCRIPTS Pointer (DSP) register.

If the comparisons are false, the LSI53C770 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Figure 5.5 Transfer Control Instruction Register



Return Instruction

The LSI53C770 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, then it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register. That address value becomes the address of the next instruction.

When the LSI53C770 executes a Call instruction, the current instruction pointer contained in the DMA SCRIPTS Pointer (DSP) register is stored in the Temporary Stack (TEMP) register.

When a Return instruction is executed, the value stored in the Temporary Stack (TEMP) register is returned to the DMA SCRIPTS Pointer (DSP) register.

The LSI53C770 does not check to see whether the Call instruction has already been executed. It does not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

If the comparisons are false, the LSI53C770 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Interrupt Instruction
The LSI53C770 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, then the LSI53C770 generates an interrupt by asserting the IRQ/ signal.

The 32-bit address field stored in the DMA SCRIPTS Pointer Save (DSPS) register can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the interrupt service routine to quickly identify the point at which the interrupt occurred.

The LSI53C770 halts and the DMA SCRIPTS Pointer (DSP) register must be written to start any further operation.

Interrupt-on-the-Fly Instruction
The LSI53C770 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the LSI53C770 asserts the Interrupt-on-the-Fly bit (Interrupt Status (ISTAT), bit 2).

SCSI Phase **[26:24]**

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. Table 5.4 describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the LSI53C770 is operating in Initiator mode. Clear the bits when the LSI53C770 is operating in the Target mode.

Table 5.4 SCSI Phase Comparisons

MSG	C/D	I/O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message-Out
1	1	1	Message-In

Relative Addressing Mode **23**

When this bit is set, the 24-bit signed value in the DMA SCRIPTS Pointer Save (DSPS) register is used as a relative offset from the current DMA SCRIPTS Pointer (DSP) address (which is pointing to the next instruction, not the one currently executing). The relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address

Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address
Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
xx	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPTS currently under execution by the LSI53C770. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (2's complement), the jump can be forward or backward.

A relative transfer can be to any address within a 16-Mbyte segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it does not require any run time alteration of physical addresses, and can be stored in and executed from a PROM.

Reserved **22**

Carry Test **21**
When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Interrupt-on-the-Fly **20**
When this bit is set, the interrupt instruction does not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt-on-the-Fly bit (Interrupt Status (ISTAT), bit 2) is asserted.

Jump If True/False **19**

This bit determines whether the LSI53C770 branches when a comparison is true or when a comparison is false. This bit applies to both phase compares and data compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Compare Data **18**

When this bit is set, then the first byte received from the SCSI data bus (contained in SCSI First Byte Received (SFBR) register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare occurs. The Jump if True/False bit determines the condition (true or false) to branch on.

Compare Phase **17**

When the LSI53C770 is in Initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ) are compared to the Phase Field in the Transfer Control instruction. If they match, the comparison is true. The Wait for Valid Phase bit controls when the compare occurs.

When the LSI53C770 is operating in Target mode and this bit is set it tests for an active SCSI ATN/ signal.

Wait For Valid Phase **16**

If the Wait for Valid Phase bit is set, the LSI53C770 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is cleared, then the LSI53C770 compares the SCSI phase and data immediately.

Data Compare Mask **[15:8]**
The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, if any mask bits are set, the corresponding bit in the SCSI First Byte Received (SFBR) data byte is ignored. For instance, a mask of 0b01111111 and data compare value of 0b1XXXXXXX allows the SCRIPTS processor to determine whether or not the high order bit is set while ignoring the remaining bits.

Data Compare Value **[7:0]**
This 8-bit field is the data compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

5.5.2 Second Dword

Jump Address **[31:0]**
This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the LSI53C770 fetches the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DMA SCRIPTS Pointer (DSP) register and becomes the current instruction pointer.

5.6 Memory Move Instructions

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

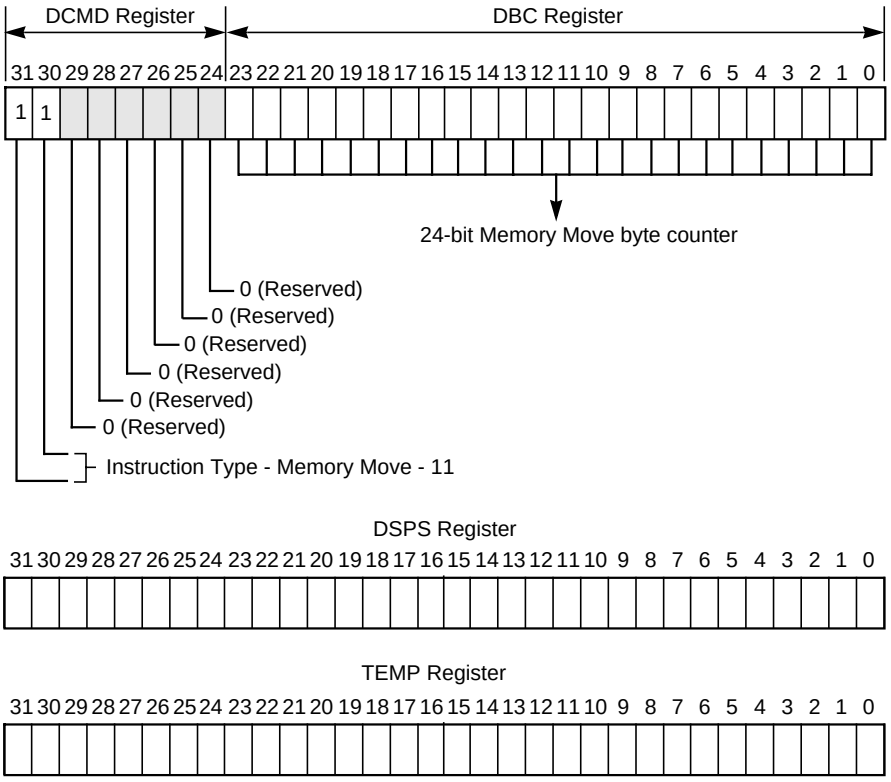
Allowing the LSI53C770 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 Mbytes may be transferred with one instruction. There are two restrictions:

- Both the source and destination addresses must start with the same address alignment A[1:0]. If source and destination are not aligned, then an illegal instruction interrupt occurs. If cache line burst is enabled and the byte count is greater than 32 bytes, address lines A[3:0] must be the same.
- Indirect addresses are not allowed. A special block move instruction passes the source and destination addresses and the byte count to the LSI53C770. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPTS is fetched from system memory.

Upon completion of the move, an interrupt instruction or jump to a SCSI function should be executed.

The DMA SCRIPTS Pointer Save (DSPS) and Data Structure Address (DSA) registers are additional holding registers used during the Memory Move.

Figure 5.6 Memory Move Instruction Register



5.6.1 First Dword

Memory Move Instruction **[31:30]**

Reserved **[29:24]**
These bits are reserved and must be zero. If any of these bits are set, an illegal instruction interrupt occurs.

Transfer Count **[23:0]**
The number of bytes to transferred is stored in the lower 24 bits of the first instruction word.

5.6.2 Second Dword

Source Address **[31:0]**
This is the absolute 32-bit starting address of the data in memory.

Chapter 6
Electrical Characteristics

This chapter specifies the LSI53C770 electrical and mechanical characteristics. It is divided into the following sections:

6.1 DC Characteristics

This section of the manual describes the LSI53C770 DC Characteristics. Table 6.1 through Table 6.11 give current and voltage specifications.

Table 6.1 Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	–55	150	˚C
V_{DD}	Supply voltage	–0.5	7.0	V
V_{IN}	Input voltage	V_{SS} –0.5	V_{DD} +0.5	V
I_{LP}	Latch-up current	200	–	mA[1]
ESD[2]	Electrostatic discharge	–	2 K	V

1. –2 V = Vpin > +8 V.
2. SCSI pins only. Measured according to MIL-STD-883C, Method 3015.7.

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.

Table 6.2 Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	4.75	5.25	V
V_{DD}	Supply voltage	4.75	5.25	V
I_{DD}	Supply current (static)	–	1	mA
I_{DD}	Supply current (dynamic)	–	75	mA
T_A	Operating temperature (free air)	0	70	˚C
Θ_{JA}	Thermal resistance (junction to ambient air)	50	65	˚C/W
P_{DD}	Power dissipation	0	0.40	W

Table 6.3 SCSI Signals—SD[15:0][1], SDP0/[1], REQ/[1], MSG/, I_O/, C_D/, ATN/, ACK/[1], BSY/, SEL/, RST/, SDP1[1]

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{HYS}	Hysteresis	300	–	mV	–
I_{IN}	Input leakage current	–10	10	µA	–
–	Input leakage (SCSI RST)	–400	10	µA	–
I_{OZ}	3-state leakage current	–10	10	µA	–

1. TolerANT not enabled.

Table 6.4 Input Signals—BG/-HLDAI/, BOFF/, RESET/, CS/, BS[2:0]/, BCLK, SCLK, AUTO/, DIFFSENS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IN}	Input leakage current	–10.0	10.0	µA	–

Table 6.5 Input Signal—TSTIN/

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IH}	Input high leakage current	–10.0	10	µA	$V_{IH} = V_{DD}$
I_{IL}	Input low pull-up current	–200	–50	µA	V_{IL} = 0 V

Table 6.6 Output Signals—SDIR[15:0], SDIRP0, BSYDIR, SELDIR, RSTDIR, TGS, IGS, SDIRP1

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 4 mA
I_{OH}	Output high current	–2.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	4.0	–	mA	V_{OL} = 0.4 V

Table 6.7 Output Signals—FETCH/, IRQ/, TSTOUT

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 8mA
I_{OH}	Output high current	–4.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	8.0	–	mA	V_{OL} = 0.4 V

Table 6.8 Output Signal—SLACK/-READYO/, MASTER/, MAC/

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V

Table 6.9 3-State Output Signals—A[31:7], FC[2:0]-TM[2:0], SC[1:0], UPSO-TT0/, CBREQ/-TT1/, BR/-HOLD/

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	V_{OH} = V_{DD} –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V
I_{OZ}	3-state leakage current	–10	10	µA	–

Table 6.10 Bidirectional Signals—A[6:0], D[31:0], DP[3:0], DS/-DLE/, AS/-TS/-ADS/, R_W/, BE0, BE1/, SIZ[1:0], BHE/-BE2, SIZ1-BE3, BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/-READYI/, GPIO[4:0]

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	V_{OH} = V_{DD} –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V
I_{IN}	Input leakage current	–10	10	µA	–
I_{OZ}	3-state leakage current	–10	10	µA	–

Table 6.11 Capacitance

Symbol	Parameter	Min	Max	Units	Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

6.2 LSI Logic TolerANT Technology

The LSI53C770 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Table 6.12 provides electrical characteristics for SE SCSI signals. Figure 6.1 through Figure 6.5 provide reference information for testing SCSI signals.

Table 6.12 TolerANT Active Negation Technology Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.5	3.1	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.2	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	–	7.0	V	–
V_{IL}	Input low voltage	–0.5	–	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.74	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.1	1.2	1.3	V	–
V_{TL}	Threshold, LOW to HIGH	1.5	1.6	1.7	V	–
V_{TH}-V_{TL}	Hysteresis	300	350	400	mV	–
I_{OH}[2]	Output high current	2.5	15	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	150	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	–	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	–	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	0.05	10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	–0.05	–10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	–	20	–	MΩ	SCSI pins[3]
C_P	Capacitance per pin	–	8	10	pF	PQFP
t_R[2]	Rise time, 10% to 90%	9.7	15.0	18.5	ns	Figure 6.1
t_F	Fall time, 90% to 10%	5.2	8.1	14.7	ns	Figure 6.1
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.23	0.49	V/ns	Figure 6.1
dV_L/dt	Slew rate, HIGH to LOW	0.19	0.37	0.67	V/ns	Figure 6.1
	Electrostatic discharge	2	–	–	KV	MIL-STD-883C; 3015.7
	Latch-up	100	–	–	mA	–
	Filter delay	20	25	30	ns	Figure 6.2
	Extended filter delay	40	50	60	ns	Figure 6.2

1. Active Negation outputs only: Data, Parity, SREQ, SACK.
2. Single pin only. Irreversible damage may occur if sustained for one second.
3. SCSI RESET pin has 10 kΩ pull-up resistor.

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

Figure 6.1 Rise and Fall Time Test Conditions

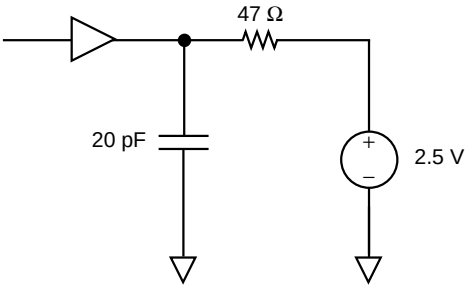
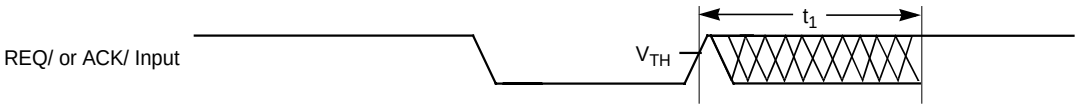


Figure 6.2 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 6.3 Hysteresis of SCSI Receiver

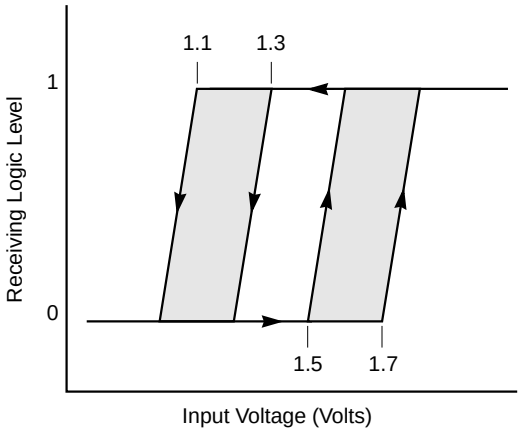


Figure 6.4 Input Current as a Function of Input Voltage

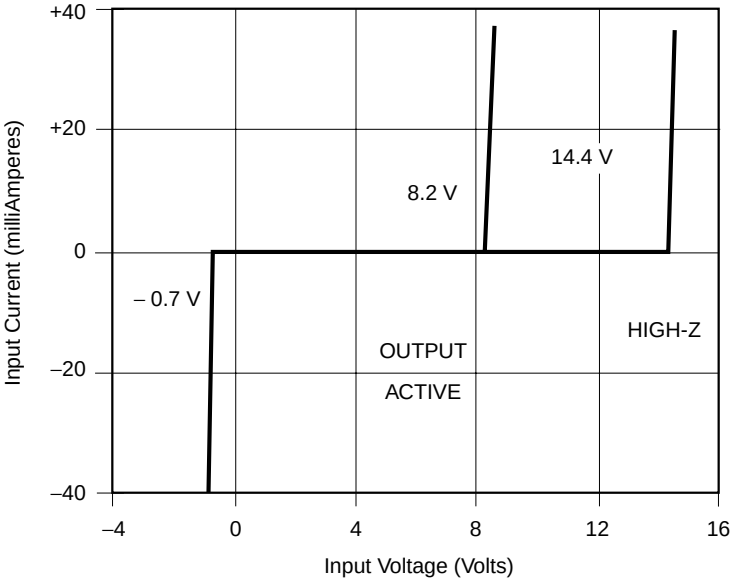
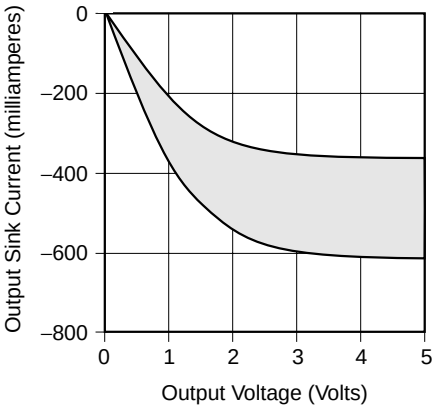
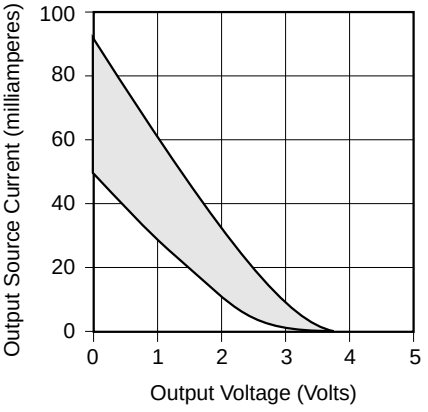


Figure 6.5 Output Current as a Function of Output Voltage





6.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Table 6.2, Operating Conditions). Chip timing is based on simulation at worst case voltage, temperature, and processing. Figure 6.6 and Table 6.13 provide Clock Timing data.

Figure 6.6 Clock Waveform

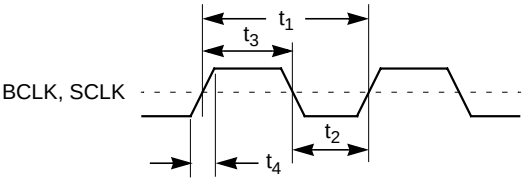


Table 6.13 Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time (BCLK			
	Bus Mode 1	40	DC	ns
	Bus Mode 2, 3, 4	30	DC	ns
	SCSI clock cycle time (SCLK)[1]	15	60	ns
t_2	BCLK LOW time	40% of BCLK cycle time	DC	ns
	Bus Mode1		DC	ns
	Bus Modes 2, 3, 4			
	SCLK LOW time[1]	40% of BCLK cycle time	33	ns
t_3	BCLK HIGH time[2]	40% of BCLK cycle time	–	ns
	Bus Mode1	7	–	ns
	Bus Modes 2, 3, 4			
	SCSI HIGH time	Bus Modes 2, 3, 4	33	ns
t_4	BCLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. This parameter must be met to ensure SCSI timing are within specification.

Figure 6.7 and Table 6.14 provide Reset Input Timing data.

Figure 6.7 Reset Input Waveforms

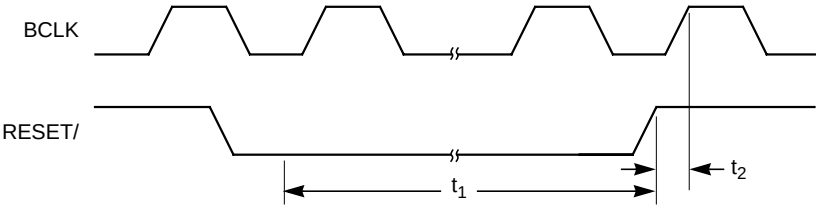


Table 6.14 Reset Input Timing

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	–	BCLK
t_2	Reset deasserted setup to BCLK HIGH	10	–	ns

Figure 6.8 and Table 6.15 provide Interrupt Output Timing data.

Figure 6.8 Interrupt Output Waveforms

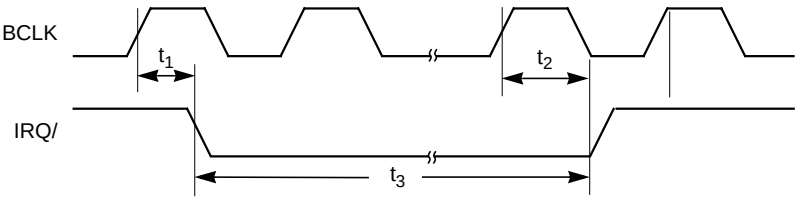


Table 6.15 Interrupt Output Timing

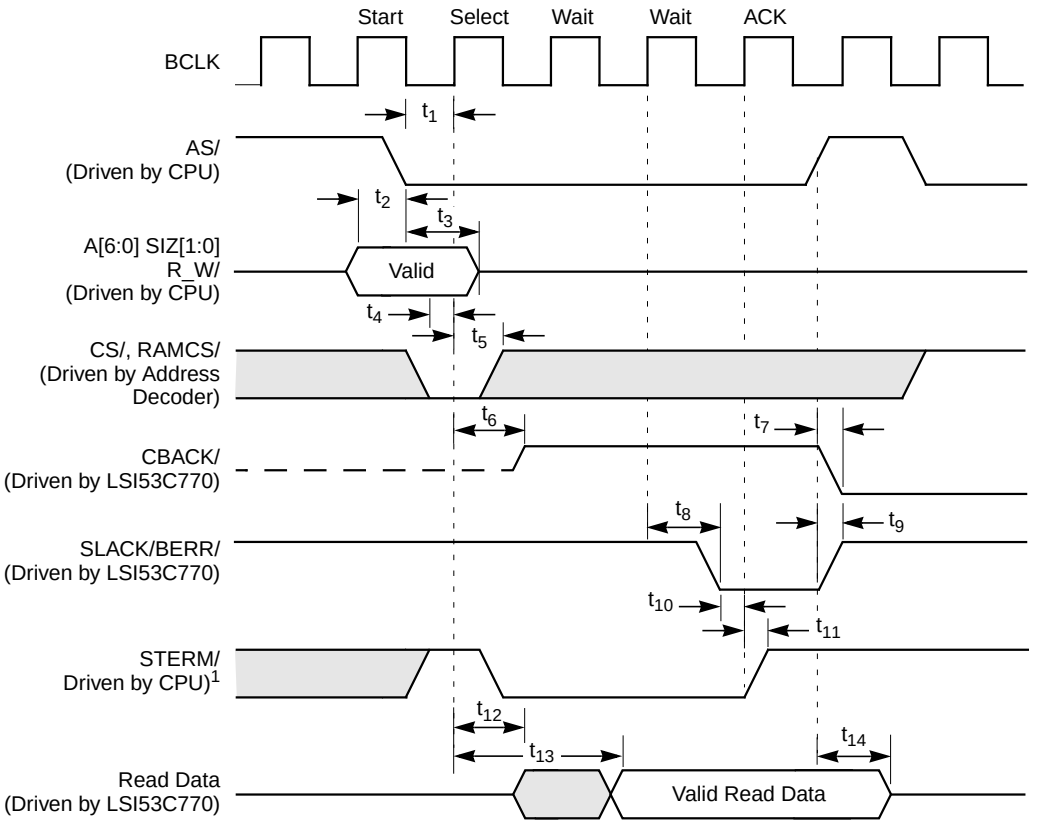
Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to IRQ/ high	–	20	ns
t_2	BCLK HIGH to IRQ/ low	–	58	ns
t_3	IRQ/ assertion time	3	–	BCLK

6.4 Bus Mode 1 Slave Cycle

6.4.1 Bus Mode 1 Slave Read Sequence

1. The Read/Write, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the LSI53C770.
5. Two clock cycles of wait-state are inserted (these wait-states are required) and the data lines are asserted by the LSI53C770.
6. Slave Acknowledge is asserted by the LSI53C770 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the LSI53C770 and the data lines are 3-stated by the LSI53C770.

Figure 6.9 Bus Mode 1 Slave Read Waveforms



[1] This signal may be driven by the LSI53C770 if the Enable ACK bit is set (DMA Control (DCNTL), bit 5). See the explanation in Chapter 2 for use of this signal as an output.

Note: The LSI53C770 must see address strobes (AS/) paired up with synchronous cycle terminations (STERM/), even though the slave cycle may not be intended for the LSI53C770.

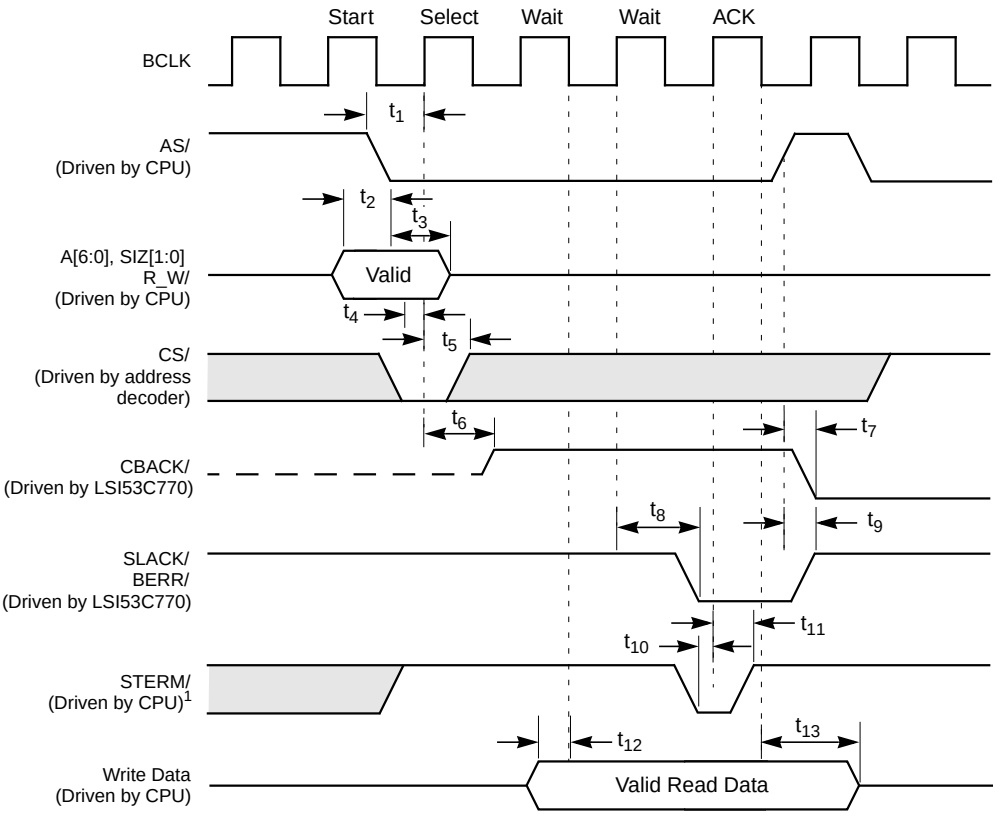
Table 6.16 Bus Mode 1 Slave Read Timing

Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[6:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[6:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	30	ns
t_7	AS/ HIGH to CBACK/ LOW	3	17	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	22	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	22	ns
t_{10}	STERM/ setup to BCLK HIGH	3	–	ns
t_{11}	STERM/ hold from BCLK HIGH	7	–	ns
t_{12}	BCLK HIGH to data bus driven	8	28	ns
t_{13}	BCLK HIGH to read data valid	–	75	ns
t_{14}	AS/ HIGH to data bus HIGH-Z	7	32	ns

6.4.2 Bus Mode 1 Slave Write Sequence

1. The Read/Write, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the LSI53C770
5. The data lines are asserted by the CPU.
6. Slave Acknowledge is asserted by the LSI53C770 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the LSI53C770.

Figure 6.10 Bus Mode 1 Slave Write Waveforms



[1] This signal may be driven by LSI53C770 if the Enable ACK bit is set (DMA Control (DCNTL), bit 5). See the explanation in Chapter 2 for use of this signal as an output.

Note: Data is latched on the rising edge of the ACK cycle when SLACK/ is asserted. Wait-states cannot be inserted by using STERM/.

Table 6.17 Bus Mode 1 Slave Write Timing

Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[6:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[6:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	30	ns
t_7	AS/ HIGH to SLACK/ BERR/ HIGH	3	17	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	22	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	22	ns
t_{10}	STERM/ (input) setup to BCLK HIGH	3	–	ns
t_{11}	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_{12}	Write data setup to BCLK LOW	4	–	ns
t_{13}	Write data hold from BCLK LOW	6	–	ns

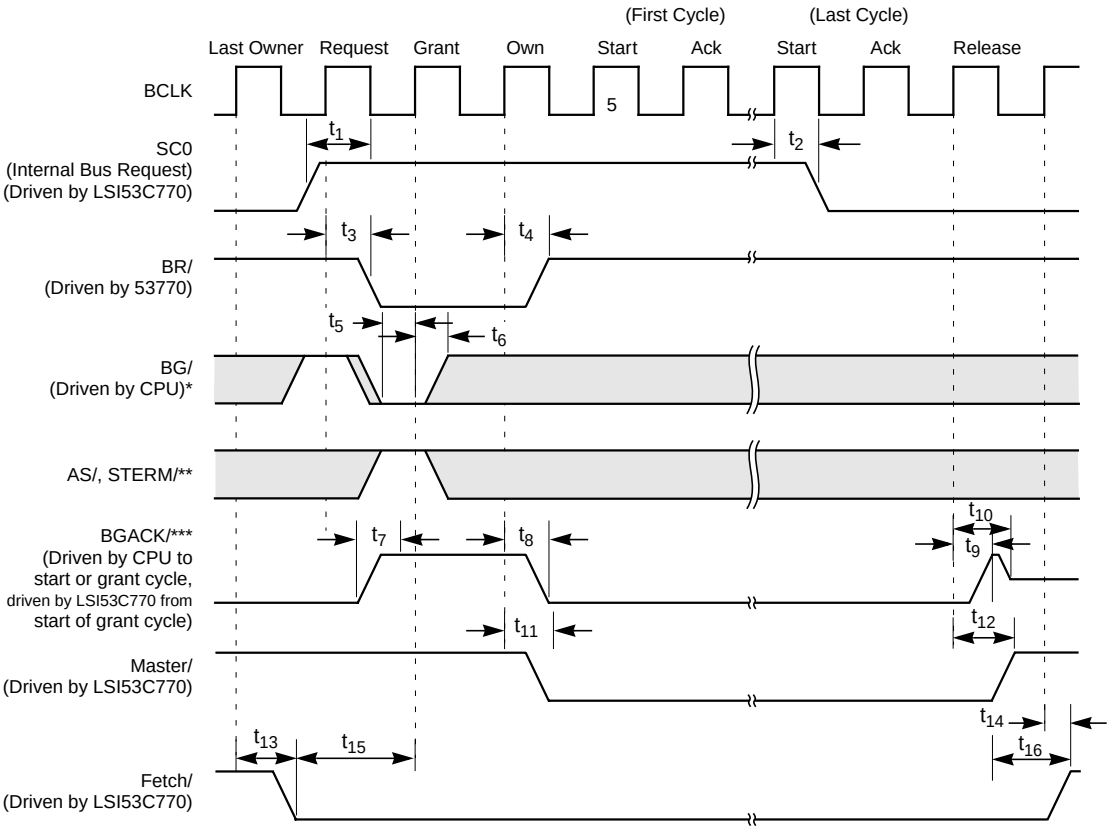
Note: The LSI53C770 must see address strobes (AS/) paired up with synchronous cycle terminations (STERM/), even though the slave cycle may not be intended for the LSI53C770.

6.5 Bus Mode 1 Host Bus Arbitration

6.5.1 Bus Arbitration Sequence

1. The LSI53C770 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The LSI53C770 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the LSI53C770 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Figure 6.11 Bus Mode 1 Host Bus Arbitration



* The LSI53C770 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access – it deasserts the BR/. Master/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may service.

** AS/ and STERM/ must be deasserted at this point for the LSI53C770 to take control of the bus.

*** If the Fast Arbitration bit is set (DMA Control (DCNTL), bit 1), the LSI53C770 will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

Table 6.18 Bus Mode 1 Host Bus Arbitration Timing

Symbol	Parameter	Min	Max	Unit
t_1	SC0 HIGH to BR/ LOW[1]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on last cycle	5	28	ns
t_3	BCLK HIGH to BR/ LOW	4	20	ns
t_4	BCLK HIGH to BR/ HIGH	5	25	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BGACK/ setup to BCLK HIGH (any rising edge after BR/)	5	–	ns
t_8	BCLK HIGH to BGACK/ LOW	4	24	ns
t_9	BCLK HIGH to BGACK/ HIGH	3	19	ns
t_{10}	BCLK HIGH to BGACK/ HIGH-Z	7	32	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	22	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	26	ns
t_{13}	BCLK HIGH to FETCH/ LOW	5	36	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	36	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BGACK/ HIGH to FETCH/ HIGH[2]	1	2	BCLK

1. When the Snoop Mode bit (Chip Test Three (CTEST3), bit 0) is set to 1.
2. During a retry operation, FETCH/ remains LOW until a successful completion of the opcode fetch or a fatal bus error.

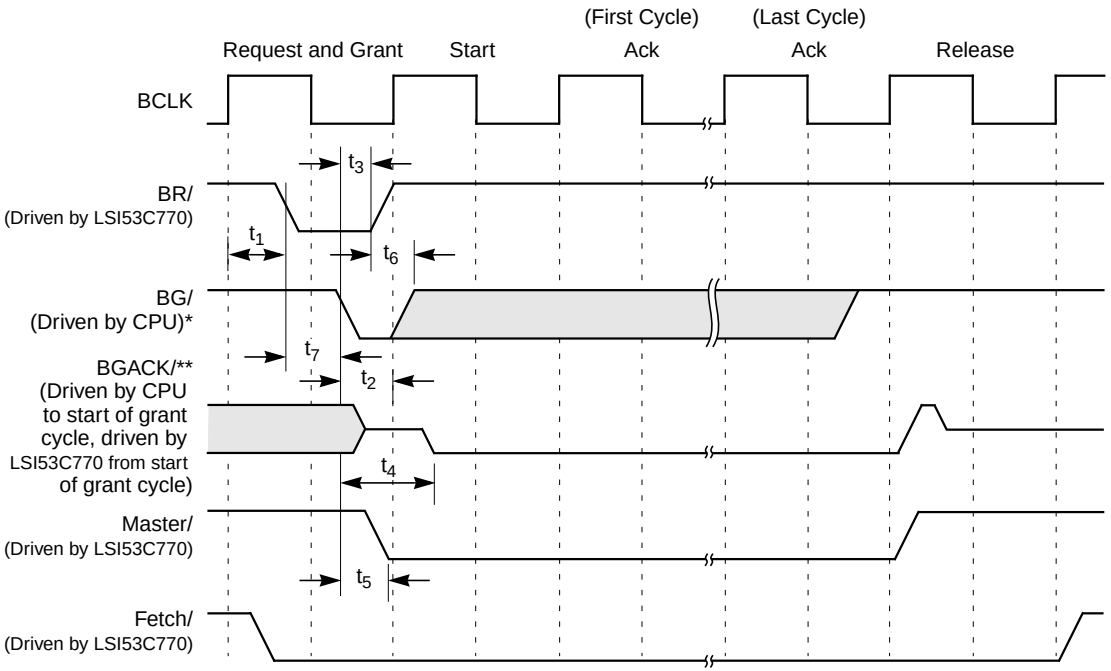
6.6 Bus Mode 1 Fast Arbitration

6.6.1 Fast Arbitration Sequence

1. The LSI53C770 internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the LSI53C770 is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The LSI53C770 waits for Bus Grant. The LSI53C770 becomes bus master asynchronously on the leading edge of BG/. The LSI53C770 asynchronously asserts Bus Grant Acknowledge and Master, then deasserts Bus Request.
4. The LSI53C770 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the LSI53C770 takes bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/.

Figure 6.12 Bus Mode 1 Fast Arbitration



* The LSI53C770 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access – it deasserts the BR/. Master/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may service.

** If the Fast Arbitration bit is set (DMA Control (DCNTL), bit 1), the LSI53C770 will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

Table 6.19 Bus Mode 1 Fast Arbitration Timing

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	20	ns
t_2	BG/ setup to BCLK HIGH	12	–	ns
t_3	BG/ asserted to BR/ deasserted	–	22	ns
t_4	BG/ asserted to BGACK/ asserted	–	20	ns
t_5	BG/ asserted to MASTER/ asserted	–	16	ns
t_6	BG/ hold after BR/ deasserted[1]	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns

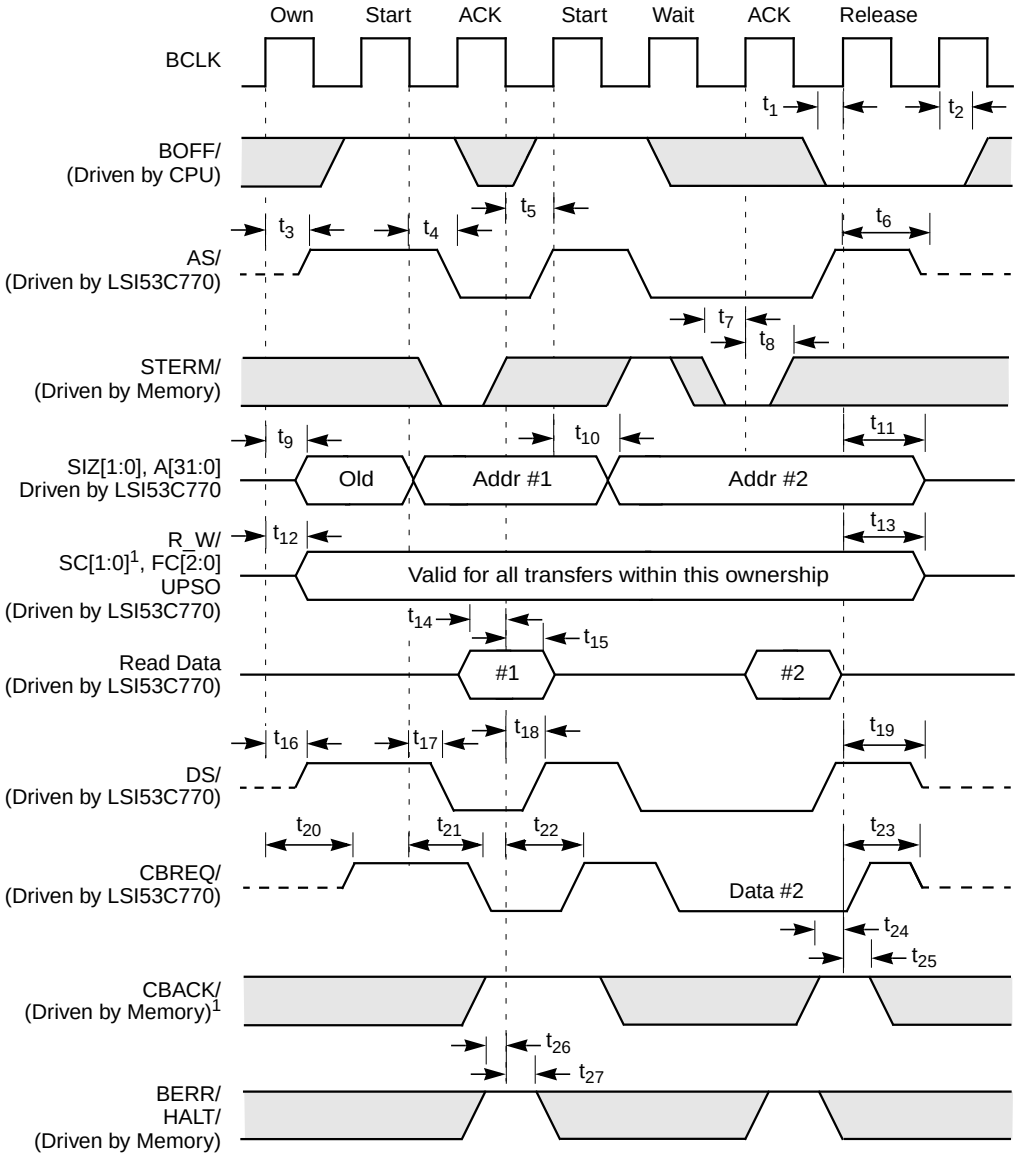
1. BG/ may not be asserted prior to BR/.

6.7 Bus Mode 1 Master Cycle

6.7.1 Bus Mode 1 Master Read Sequence

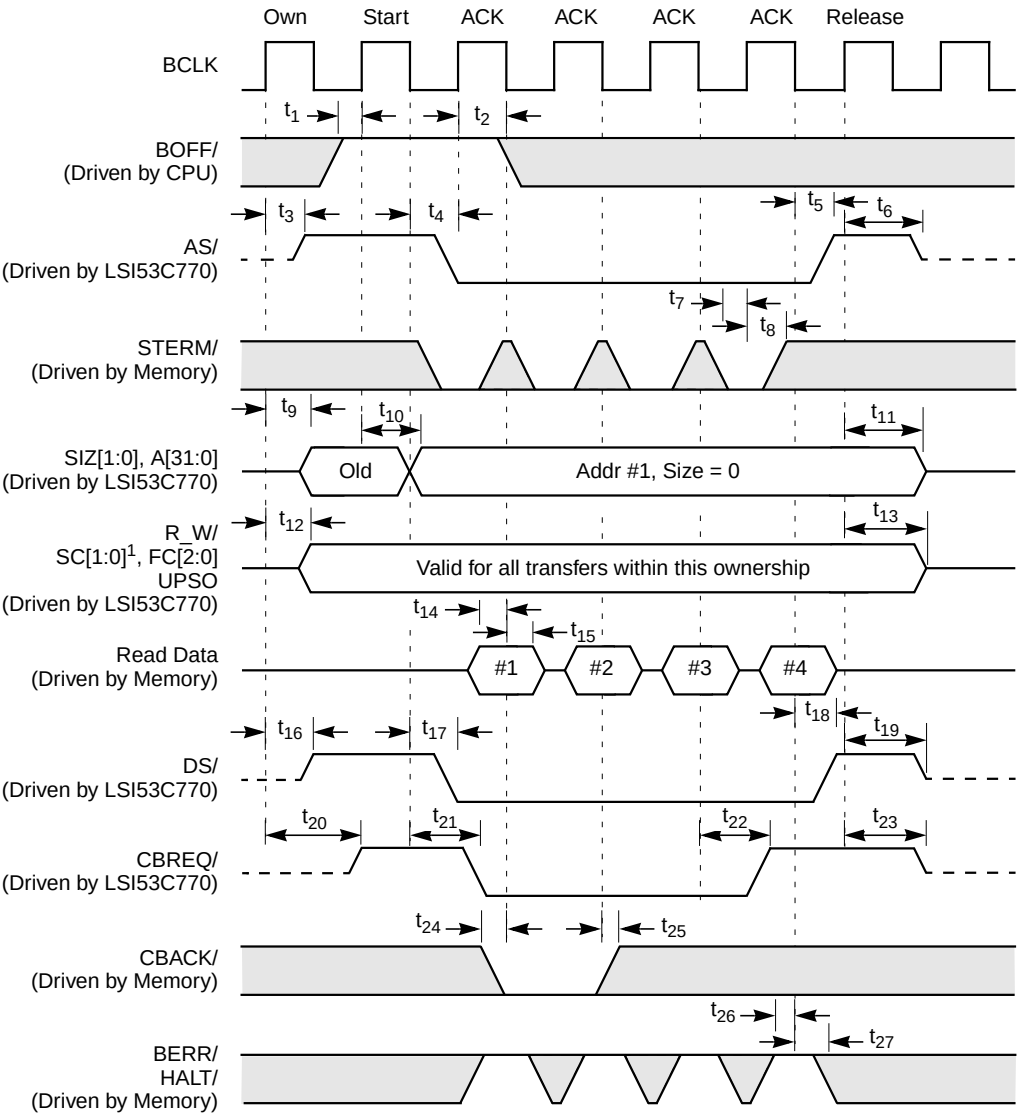
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the Read/Write, Snoop Control, Function Control, and general purpose lines.
3. The LSI53C770 asserts the Address and Size lines.
4. The LSI53C770 asserts Address Strobe, Cache Burst Request (if bursting is enabled), and Data Strobe.
5. The LSI53C770 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting. Otherwise, proceed with noncache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the LSI53C770 requires more cycles, then return to Step 3.
6. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master and Bus Grant Acknowledge.
7. The LSI53C770 floats the Control and Address lines.

Figure 6.13 Bus Mode 1 Bus Master Read (Cache Line Burst Requested but not Acknowledged)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Figure 6.14 Bus Mode 1 Bus Master Read (Cache Line Burst)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

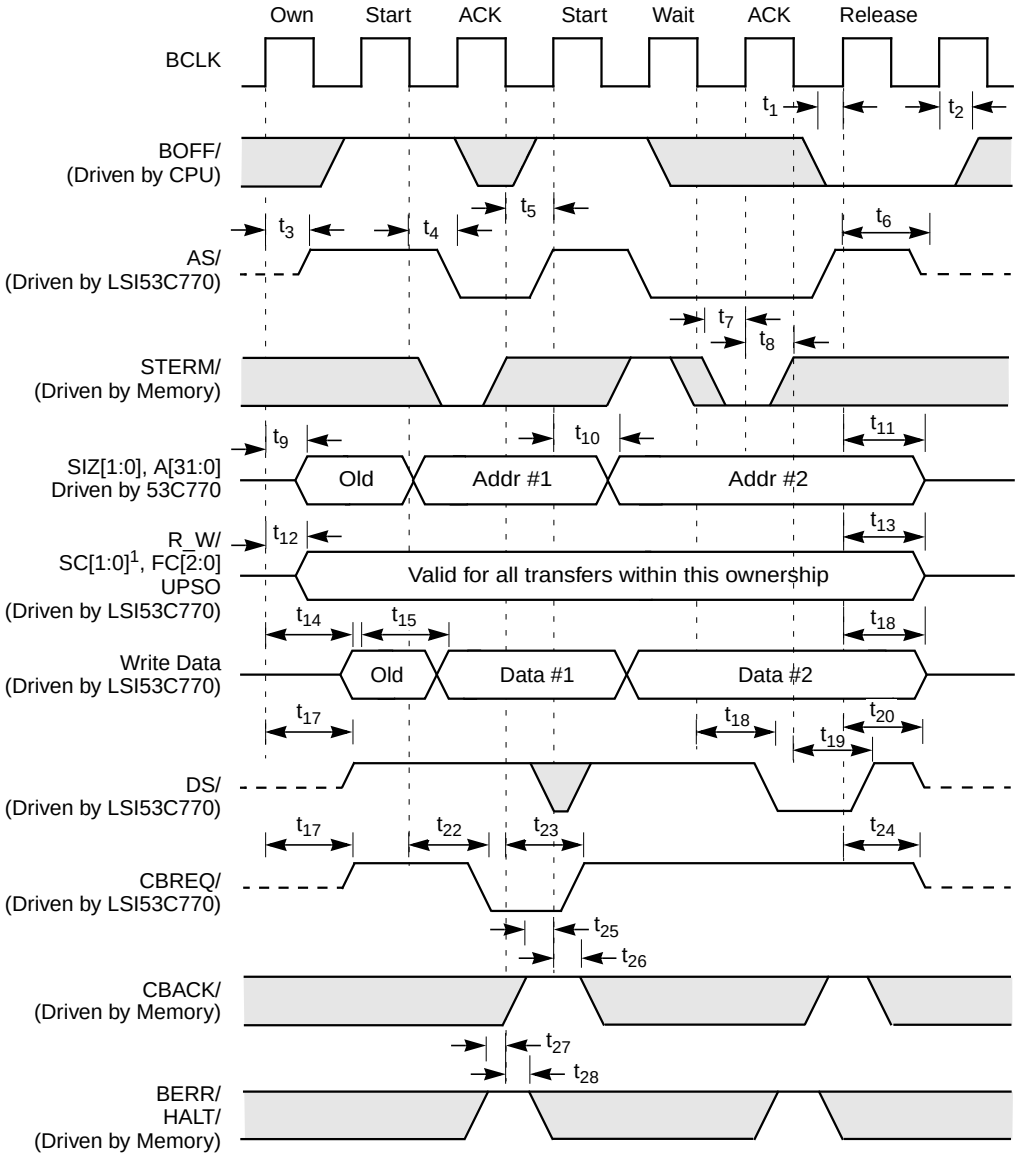
Table 6.20 Bus Mode 1 Master Read Timing

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	32	ns
t_4	BCLK LOW to AS/ LOW	3	15	ns
t_5	BCLK LOW to AS/ HIGH	3	15	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	34	ns
t_7	STERM/ setup to BCLK HIGH	3	–	ns
t_8	STERM/ hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to SIZ[1:0], A[31:0] driven	5	28	ns
t_{10}	BCLK HIGH to SIZ[1:0], A[31:0] valid	4	20	ns
t_{11}	BCLK HIGH to SIZ[1:0], A[31:0] HIGH-Z	7	34	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	28	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	30	ns
t_{14}	Read data setup to BCLK LOW	4	–	ns
t_{15}	Read data hold from BCLK LOW	6	–	ns
t_{16}	BCLK HIGH to DS/ driven	5	28	ns
t_{17}	BCLK LOW to DS/ LOW	3	17	ns
t_{18}	BCLK LOW to DS/ HIGH	3	17	ns
t_{19}	BCLK HIGH to DS/ HIGH-Z	7	32	ns
t_{20}	BCLK HIGH to CBREQ/ driven	5	28	ns
t_{21}	BCLK LOW to CBREQ/ LOW	3	18	ns
t_{22}	BCLK LOW to CBREQ/ HIGH	3	18	ns
t_{23}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns
t_{24}	CBACK/ setup to BCLK LOW	8	–	ns
t_{25}	CBACK/ hold from BCLK LOW	4	–	ns
t_{26}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{27}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

6.7.2 Bus Mode 1 Bus Master Write Sequence

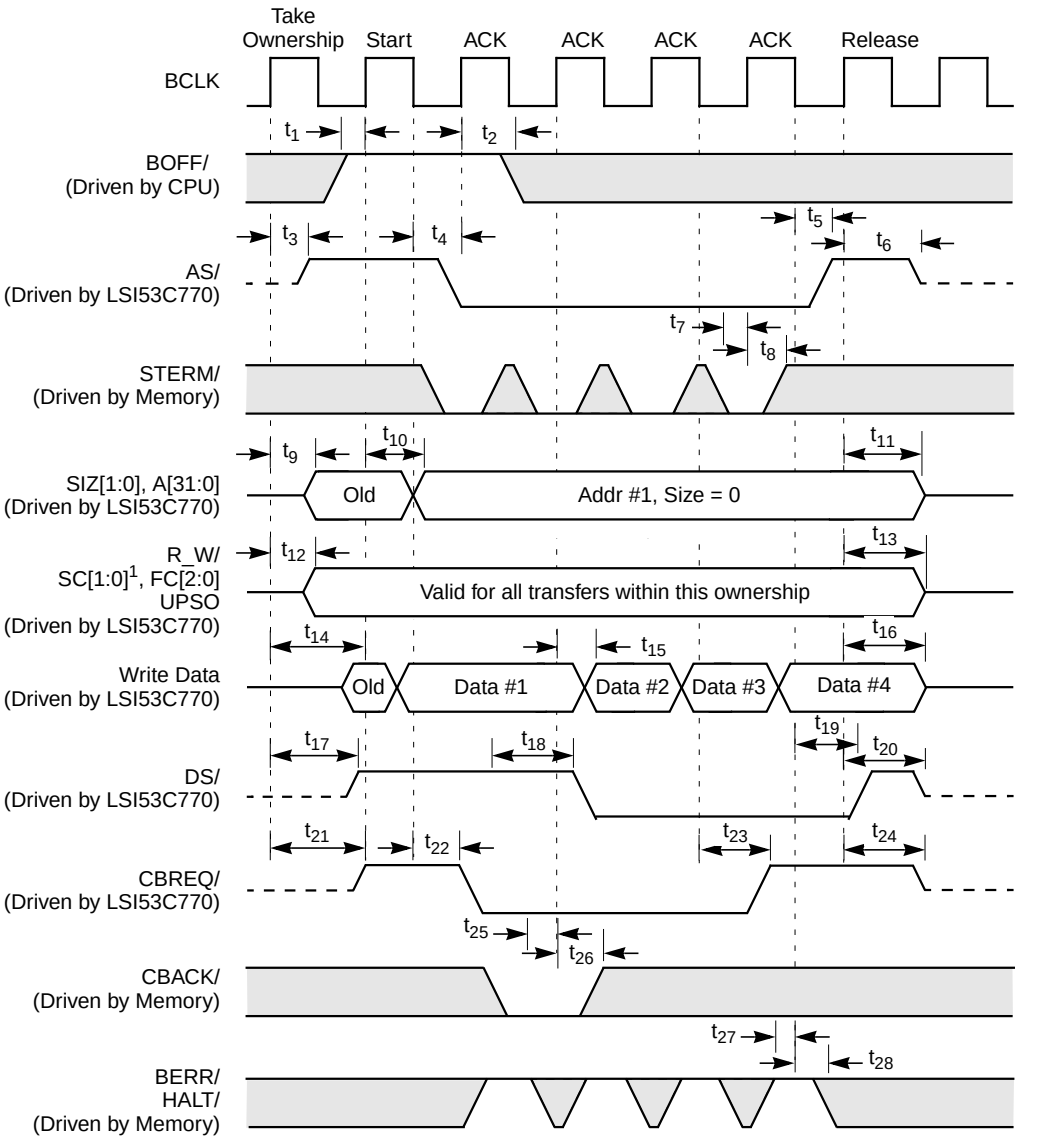
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the Read/Write, Snoop Control, Function Control, and General Purpose lines
3. The LSI53C770 asserts the Address, Size, and Data lines
4. The LSI53C770 asserts Address Strobe and Cache Burst Request.
5. The LSI53C770 asserts Data Strobe.
6. The LSI53C770 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting. Otherwise, proceed with noncache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the LSI53C770 requires more cycles, then return to Step 3.
7. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master and Bus Grant Acknowledge
8. The LSI53C770 floats the Control, Address, and Data lines.

Figure 6.15 Bus Mode 1 Bus Master Write (Cache Line Burst Requested but not Acknowledged)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Figure 6.16 Bus Mode 1 Bus Master Write (Cache Line Burst)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Table 6.21 Bus Mode 1 Master Write Timing

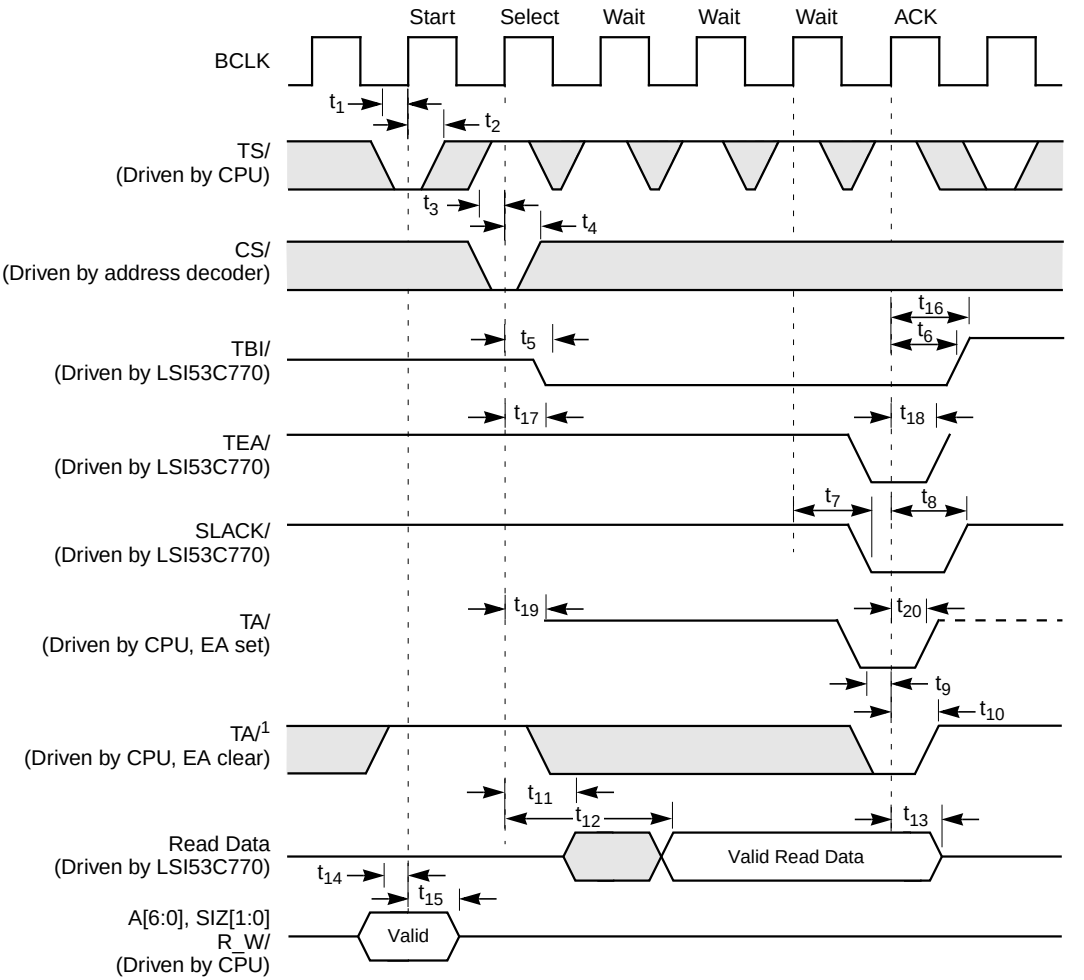
Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	32	ns
t_4	BCLK LOW to AS/ LOW	3	15	ns
t_5	BCLK LOW to AS/ HIGH	3	15	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	34	ns
t_7	STERM/ setup to BCLK HIGH	3	–	ns
t_8	STERM/ hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to SIZ[1:0], A[31:0] driven	5	28	ns
t_{10}	BCLK HIGH to SIZ[1:0], A[31:0] valid	4	20	ns
t_{11}	BCLK HIGH to SIZ[1:0], A[31:0] HIGH-Z	7	34	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	28	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	30	ns
t_{14}	BCLK HIGH to write data driven	6	34	ns
t_{15}	BCLK HIGH to write data valid	6	24	ns
t_{16}	BCLK HIGH to write data HIGH-Z	6	32	ns
t_{17}	BCLK HIGH to DS/ driven	5	32	ns
t_{18}	BCLK LOW to DS/ LOW	3	17	ns
t_{19}	BCLK LOW to DS/ HIGH	3	17	ns
t_{20}	BCLK HIGH to DS/ HIGH-Z	7	34	ns
t_{21}	BCLK HIGH to CBREQ/ driven	5	30	ns
t_{22}	BCLK LOW to CBREQ/ LOW	3	18	ns
t_{23}	BCLK LOW to CBREQ/ HIGH	3	18	ns
t_{24}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns
t_{25}	CBACK/ setup to BCLK HIGH	8	–	ns
t_{26}	CBACK/ hold from BCLK HIGH	4	–	ns
t_{27}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{28}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

6.8 Bus Mode 2 Slave Cycle

6.8.1 Bus Mode 2 Slave Read Sequence

1. The Read/Write, Address, Transfer Start, and the Size lines are asserted by the CPU.
2. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. Three clock cycles of wait-state are inserted (these wait-states are required) and the data lines are asserted.
6. Slave Acknowledge is asserted by the LSI53C770, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Slave Acknowledge or Transfer Error Acknowledge is deasserted.
9. The LSI53C770 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10. The data lines are 3-stated by the LSI53C770.

Figure 6.17 Bus Mode 2 Slave Read Waveforms



[1] This signal may be driven by LSI53C770 if the Enable ACK bit is set (DMA Control (DCNTL), bit 5). See the explanation in Chapter 2 for use of this signal as an output.

Note: The LSI53C770 must see transfer starts (TS/) paired up with transfer acknowledges, (TA/) even though the slave cycle may not be intended for the LSI53C770.

Table 6.22 Bus Mode 2 Slave Read Timing

Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	20	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	BCLK HIGH to data bus driven	8	28	ns
t_{12}	BCLK HIGH to read data valid	–	75	ns
t_{13}	BCLK HIGH to data bus HIGH-Z	7	34	ns
t_{14}	A[6:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{15}	A[6:0], SIZ[1:0], R_W/ hold from BCLK HIGH	12	–	ns
t_{16}	BCLK HIGH to TBI/ HIGH-Z	8	32	ns
t_{17}	BCLK HIGH to TEA/ driven	8	27	ns
t_{18}	BLCK HIGH to TEA/ HIGH-Z	9	34	ns
t_{19}	BCLK HIGH to TA/ driven	8	27	ns
t_{20}	BCLK HIGH to TA/ HIGH-Z	9	33	ns

6.8.2 Bus Mode 2 Slave Write Sequence

1. The Read/Write, Address, Transfer Start, and the Size Lines are asserted by the CPU.
2. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait-state are inserted (these wait-states are required).
7. Slave Acknowledge is asserted by the LSI53C770, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. The LSI53C770 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if there are no errors.
10. Slave Acknowledge or Transfer Error Acknowledge is deasserted.

Figure 6.18 Bus Mode 2 Slave Write Waveforms

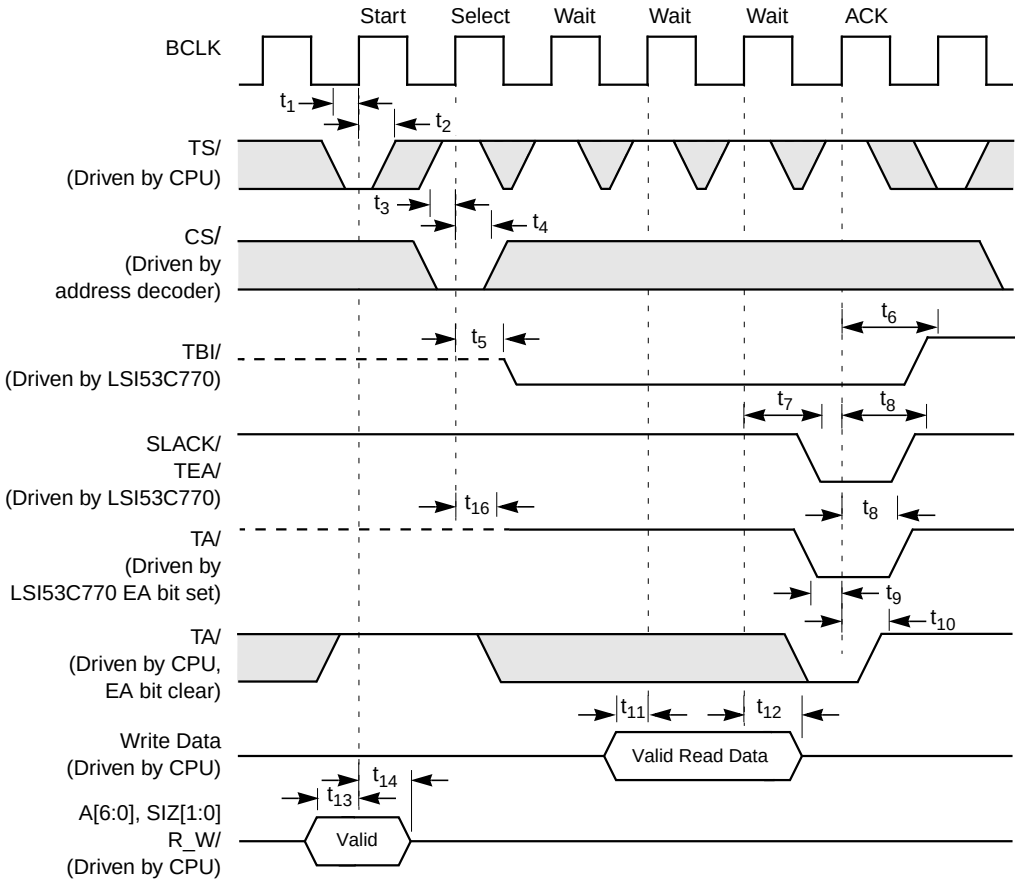


Table 6.23 Bus Mode 2 Slave Write Timing

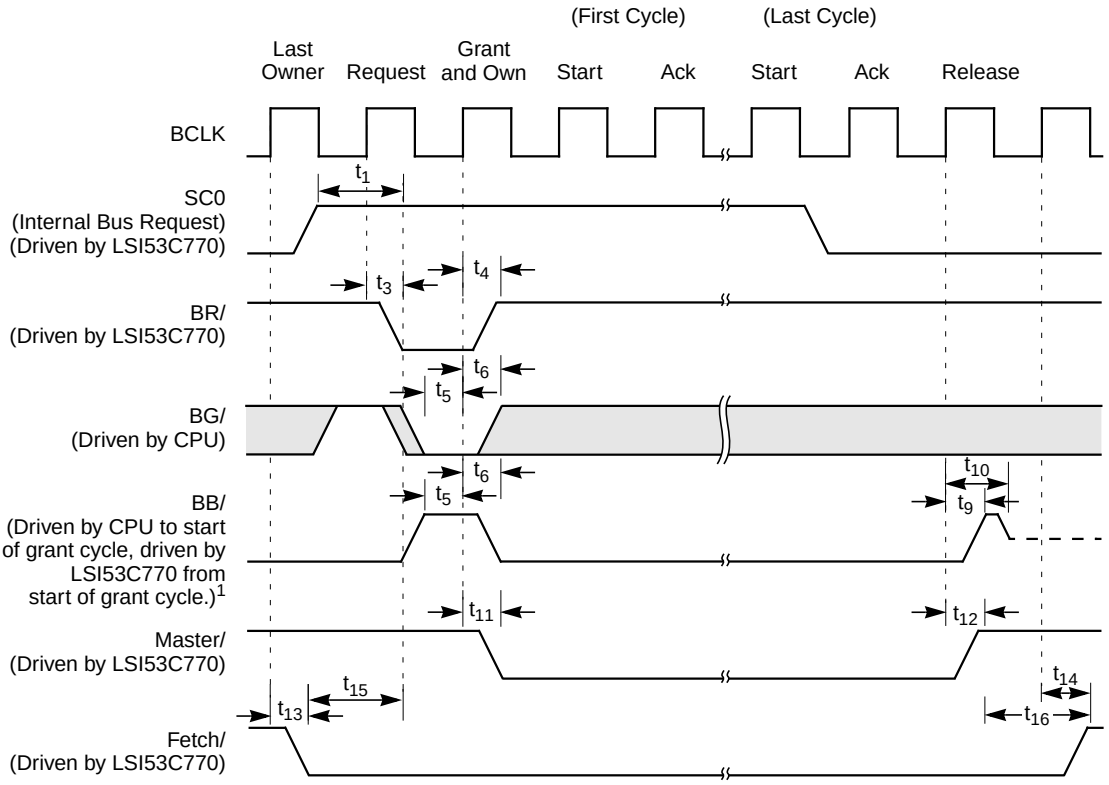
Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	20	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	Valid write data setup to BCLK HIGH	6	–	ns
t_{12}	Valid write data hold from BCLK HIGH	14	–	ns
t_{13}	A[6:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{14}	A[6:0], SIZ(1:0], R_W/ hold from BCLK HIGH	12	–	ns
t_{15}	BCLK HIGH to TA/ driven	8	27	ns
t_{16}	BCLK HIGH to TA/ HIGH-Z	9	33	ns

6.9 Bus Mode 2 Host Bus Arbitration

6.9.1 Bus Mode 2 Bus Arbitration Sequence

1. The LSI53C770 internally determines bus mastership is required. FETCH/ is asserted during cycles in which the LSI53C770 is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The LSI53C770 waits for BG/ and checks that BB/ is deasserted. Then the LSI53C770 asserts BB/ and MASTER/, and deasserts BR/.

Figure 6.19 Bus Mode 2 Host Bus Arbitration



[1] If the Fast Arbitration bit is set (DMA Control (DCNTL), bit 1), the LSI53C770 will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

Note: The LSI53C770 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access – it deasserts the BR/. Master/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may service.

Table 6.24 Bus Mode 2 Host Bus Arbitration Timing

Symbol	Parameter	Min	Max	Units
t_1	SC0 HIGH to BR/ LOW[1]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on last cycle[1]	5	28	ns
t_3	BCLK HIGH to BR/ LOW	4	20	ns
t_4	BCLK HIGH to BR/ HIGH	5	25	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BB/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_8	BCLK HIGH to BB/ LOW	4	24	ns
t_9	BCLK HIGH to BB/ HIGH	3	19	ns
t_{10}	BCLK HIGH to BB/ HIGH-Z	7	32	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	22	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	26	–
t_{13}	BCLK HIGH to FETCH/ LOW	5	36	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	36	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BB/ HIGH to FETCH/ HIGH[2]	1	2	BCLK

1. When the Snoop Mode bit Chip Test Three (CTEST3) is set to 1.
2. During a retry operation, FETCH/ remains low until successful completion of an opcode fetch or a fatal bus error.

6.10 Bus Mode 2 Fast Arbitration

6.10.1 Bus Mode 2 Fast Arbitration Sequence

1. The LSI53C770 determines bus mastership is required. FETCH/ is asserted during cycles in which the LSI53C770 is retrieving new SCRIPTS instructions.
2. Bus request is asserted.
3. The LSI53C770 waits for Bus Grant. The LSI53C770 becomes bus master asynchronously on the leading edge of BG/. Then the LSI53C770 asynchronously asserts Bus Busy and Master, and deasserts Bus Request.
4. The LSI53C770 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the LSI53C770 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.

Figure 6.20 Bus Mode 2 Fast Arbitration

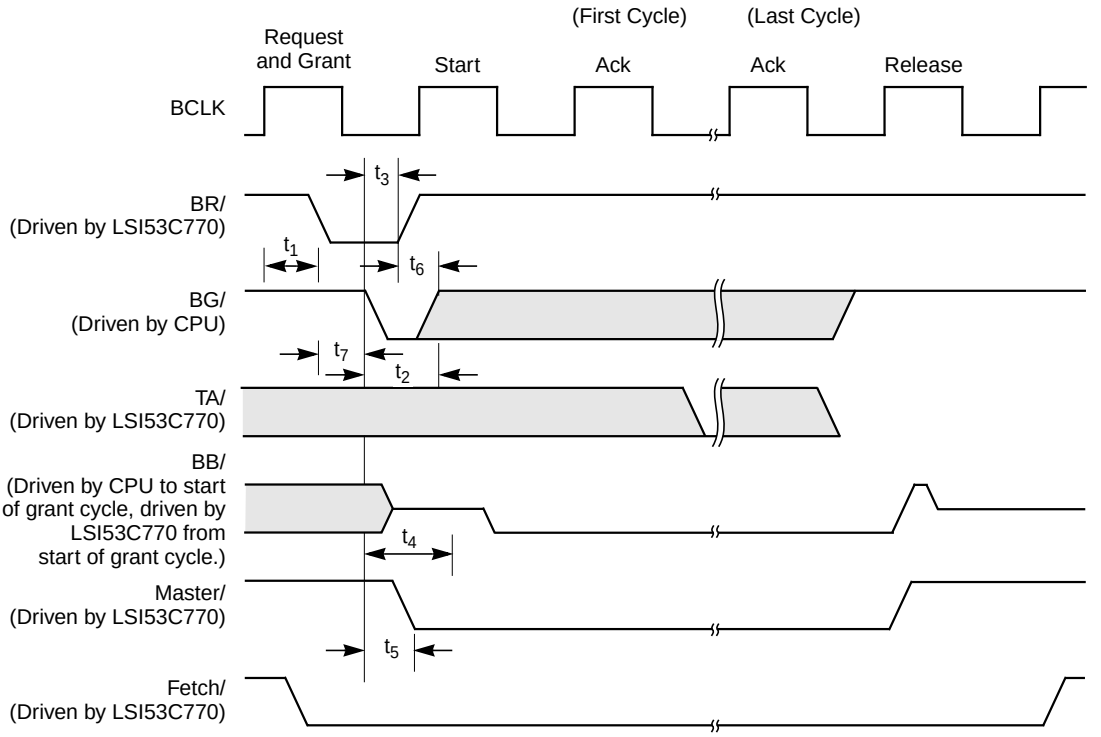


Table 6.25 Bus Mode 2 Fast Arbitration Timing

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	20	ns
t_2	BG/ setup to BCLK HIGH	12	–	ns
t_3	BG/ asserted to BR/ deasserted	–	22	ns
t_4	BG/ asserted to BB/ asserted	–	20	ns
t_5	BG/ asserted to MASTER/ asserted	–	16	ns
t_6	BG/ hold after BR/ deasserted	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns

6.11 Bus Mode 2 Master Cycle

6.11.1 Bus Mode 2 Master Read Sequence

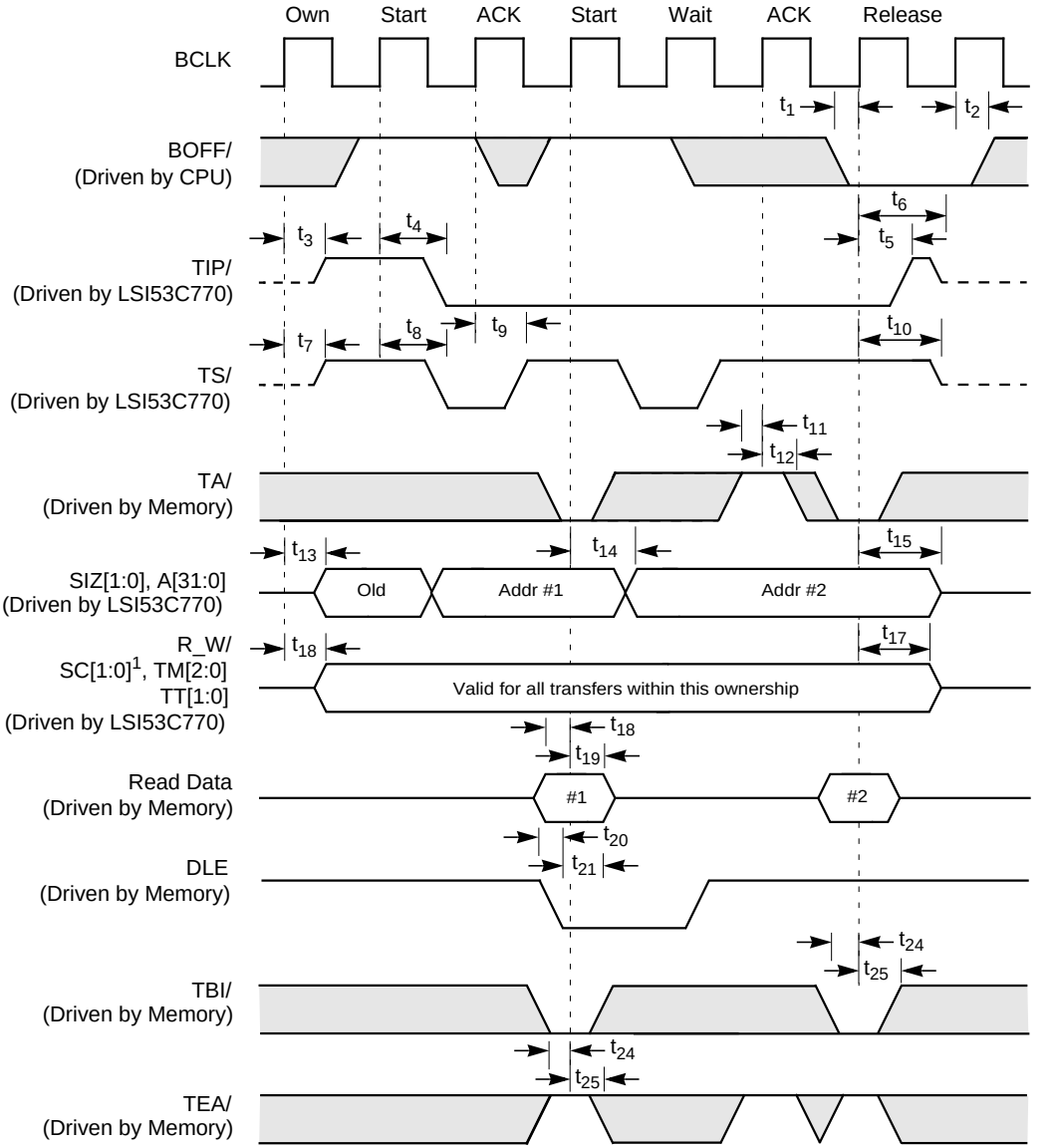
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type lines.

3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts Transfer Start, Address, and Size lines.

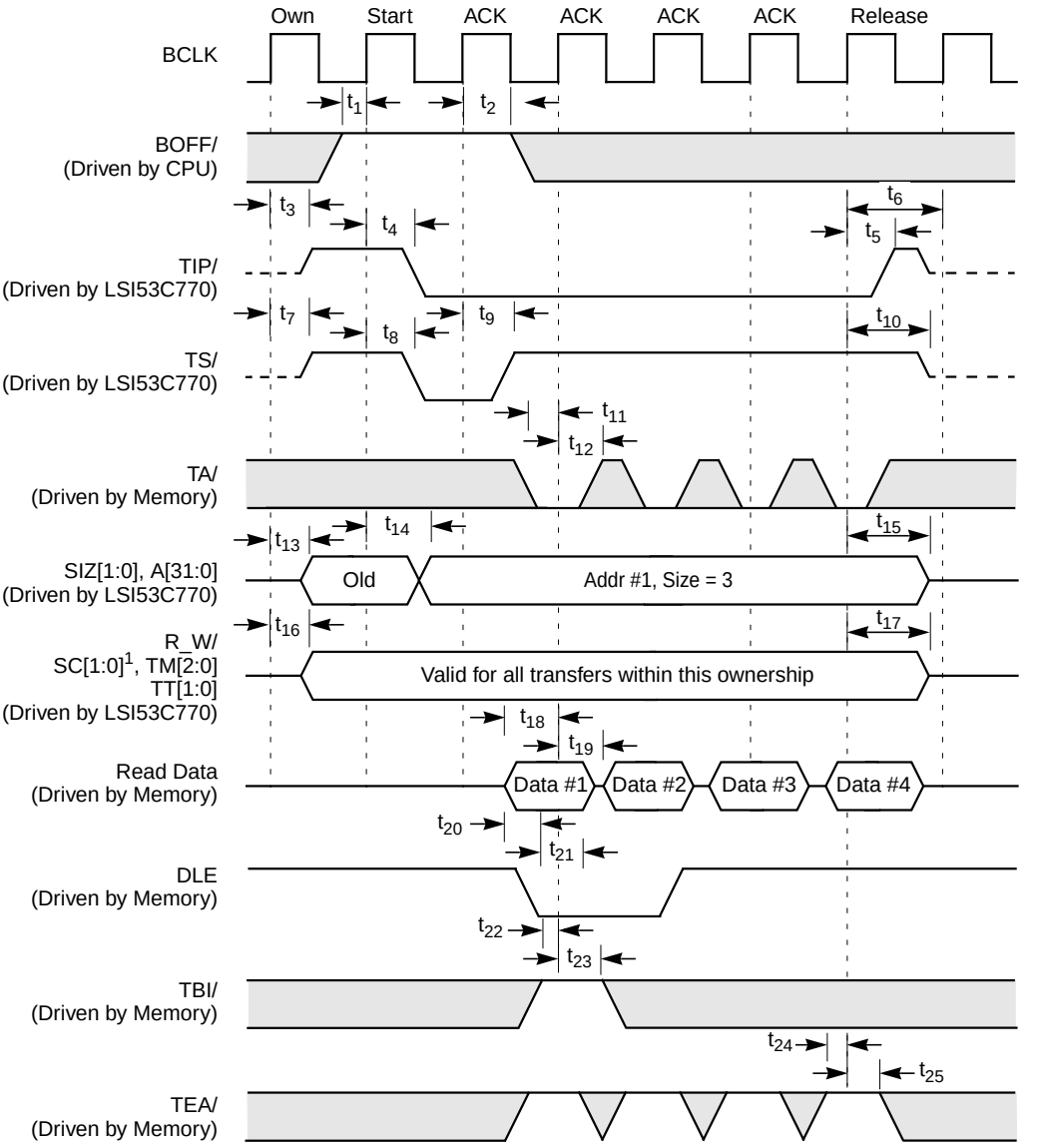
4. The LSI53C770 deasserts Transfer Start.
5. The LSI53C770 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with noncache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the LSI53C770 requires more cycles, then return to Step 3b.
6. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master, Bus Busy, and Transfer in Progress.
7. The LSI53C770 floats the Control and Address lines.

Figure 6.21 Bus Mode 2 Bus Master Read (Cache Line Burst Requested but not Acknowledged)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Figure 6.22 Bus Mode 2 Bus Master Read (Cache Line Burst)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Table 6.26 Bus Mode 2 Bus Master Read Timing

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK HIGH to TS/ driven	5	30	ns
t_8	BCLK HIGH to TS/ LOW	3	17	ns
t_9	BCLK HIGH to TS/ HIGH	4	17	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	32	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	28	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	5	20	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	32	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], TM[2:0], TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], TM[2:0], TT[1:0] HIGH-Z	–	32	ns
t_{18}	Read data setup to BCLK HIGH	5	–	ns
t_{19}	Read data hold from BCLK HIGH	6	–	ns
t_{20}	Read data setup to DLE LOW	4	–	ns
t_{21}	Read data hold from DLE LOW	6	–	ns
t_{22}	TBI/ setup to BCLK HIGH	6	–	ns
t_{23}	TBI/ hold from BCLK HIGH	4	–	ns
t_{24}	TEA/ setup to BCLK HIGH	9	–	ns
t_{25}	TEA/ hold from BCLK HIGH	5	–	ns

6.11.2 Bus Mode 2 Bus Master Write Sequence

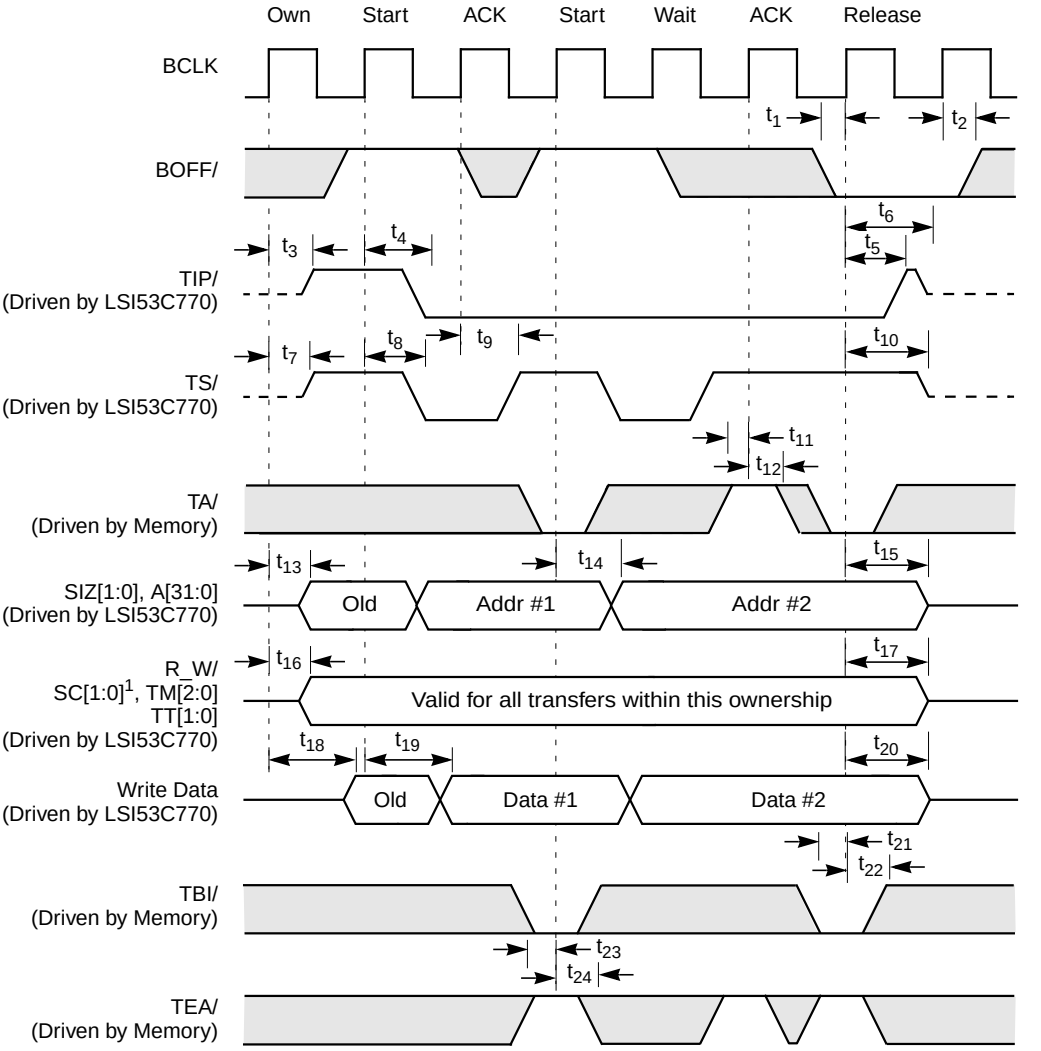
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the Read/Write, Snoop Control, Transfer Modifier, and Transfer Type Lines.

3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts Transfer Start, Address, Size lines, and Data lines.

4. The LSI53C770 deasserts Transfer Start.
5. The LSI53C770 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with noncache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the LSI53C770 requires more cycles, then return to Step 3b.
6. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master, Busy, and Transfer in Progress.
7. The LSI53C770 floats the Control, Address, and Data lines.

Figure 6.23 Bus Mode 2 Bus Master Write (Cache Line Burst Requested but not Acknowledged)



[1] SC[1:0] timing applies only if Snoop Mode bit 0 of Chip Test Three (CTEST3) equals 0.

Table 6.27 Bus Mode 2 Bus Master Write Timing

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK HIGH to TS/ driven	5	30	ns
t_8	BCLK HIGH to TS/ LOW	3	17	ns
t_9	BCLK HIGH to TS/ HIGH	3	17	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	32	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	30	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	3	20	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	32	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], TM[2:0], TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], TM[2:0], TT[1:0] HIGH-Z	5	32	ns
t_{18}	BCLK HIGH to write data driven	5	34	ns
t_{19}	BCLK HIGH to write data valid	7	24	ns
t_{20}	BCLK HIGH to write data HIGH-Z	5	30	ns
t_{21}	TBI/ setup to BCLK HIGH	6	–	ns
t_{22}	TBI/ hold from BCLK HIGH	4	–	ns
t_{23}	TEA/ setup to BCLK HIGH	9	–	ns
t_{24}	TEA/ hold from BCLK HIGH	5	–	ns

6.12 Bus Mode 2 Mux Mode Cycle

6.12.1 Mux Mode Read Sequence

1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

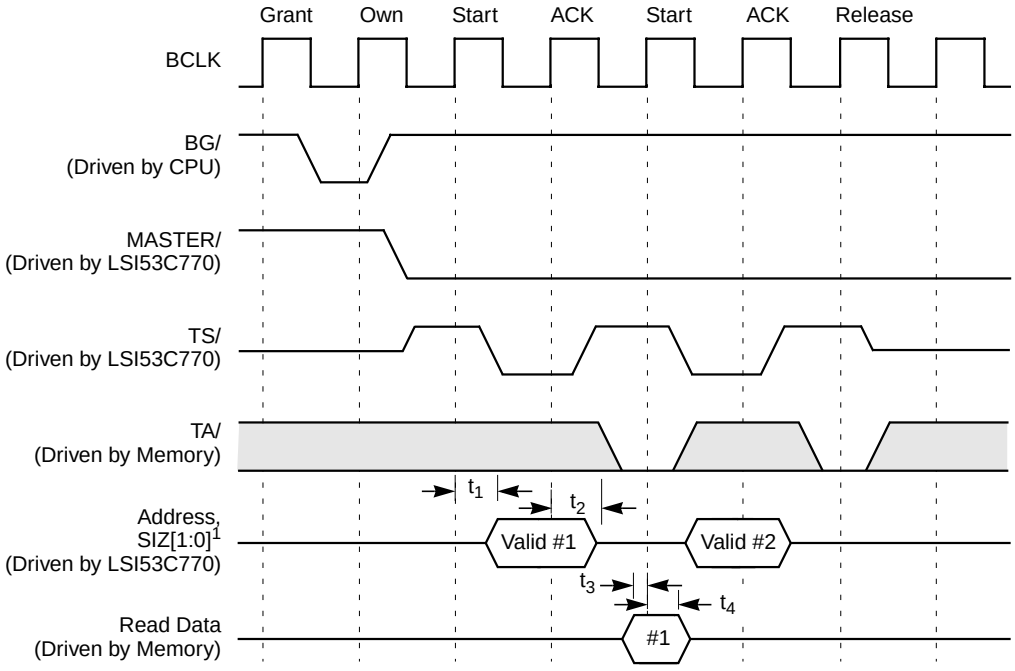
3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts the Transfer Start, Address, and Size lines.

4. The LSI53C770 deasserts Transfer Start and floats the Address lines.
5. The LSI53C770 waits for Transfer Acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with noncache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the LSI53C770 requires more cycles, then return to Step 3b.
6. The LSI53C770 deasserts the Control lines.
7. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master and Bus Grant Acknowledge.

   Note: This mode of operation expects D[31:0] to be physically tied to A[31:0], respectively.

Figure 6.24 Mux Mode Read Cycle (Cache Line Burst Requested but not Acknowledged)



[1] For cache line bursting, the value of the SIZ[1:0] bits must be 0x03.

Figure 6.25 Mux Mode Read Cycle (Cache Line Burst)

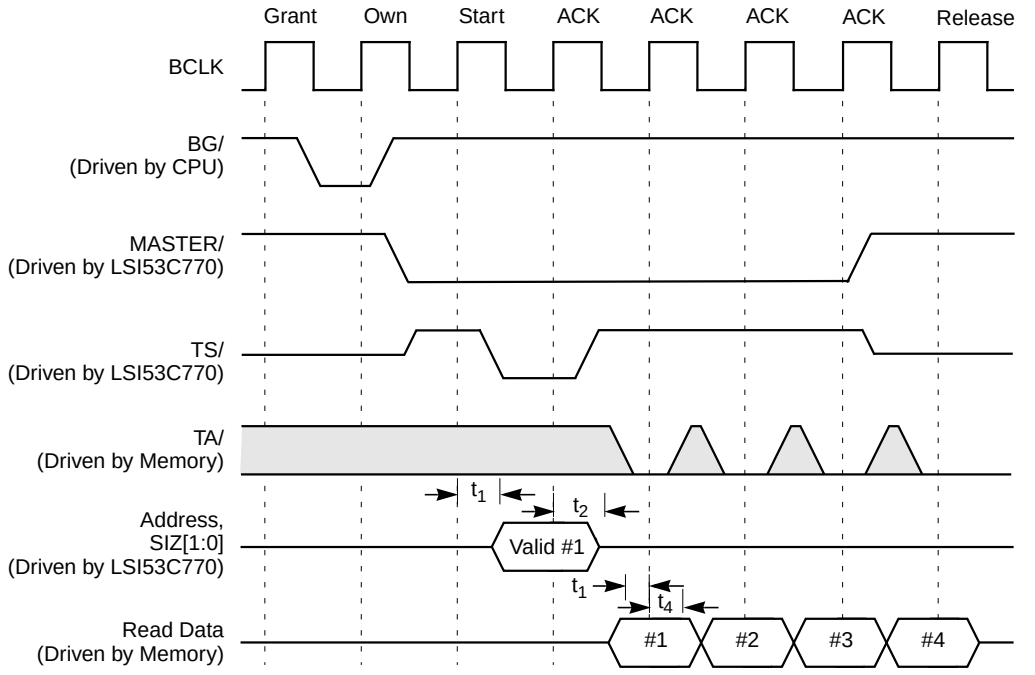


Table 6.28 Bus Mode 2 Mux Mode Read Timing

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to address driven	5	22	ns
t_2	BCLK HIGH to address HIGH-Z	–	23	ns
t_3	Read data setup to BCLK HIGH	5	–	ns
t_4	Read data hold from BCLK HIGH	6	–	ns

6.12.2 Mux Mode Write Sequence

1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts Transfer Start, Address, Size lines, and floats the Data lines.

4. The LSI53C770 deasserts Transfer Start, floats the address bus, and asserts the data bus.
5. The LSI53C770 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with noncache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the LSI53C770 requires more cycles, return to Step 3b.
6. The LSI53C770 deasserts the Control and Data lines.
7. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master and Bus Grant Acknowledge.

   Note: This mode of operation expects D[31:0] to be physically tied to A[31:0], respectively.

Figure 6.26 Mux Mode Write Cycle (Noncache Line Burst)

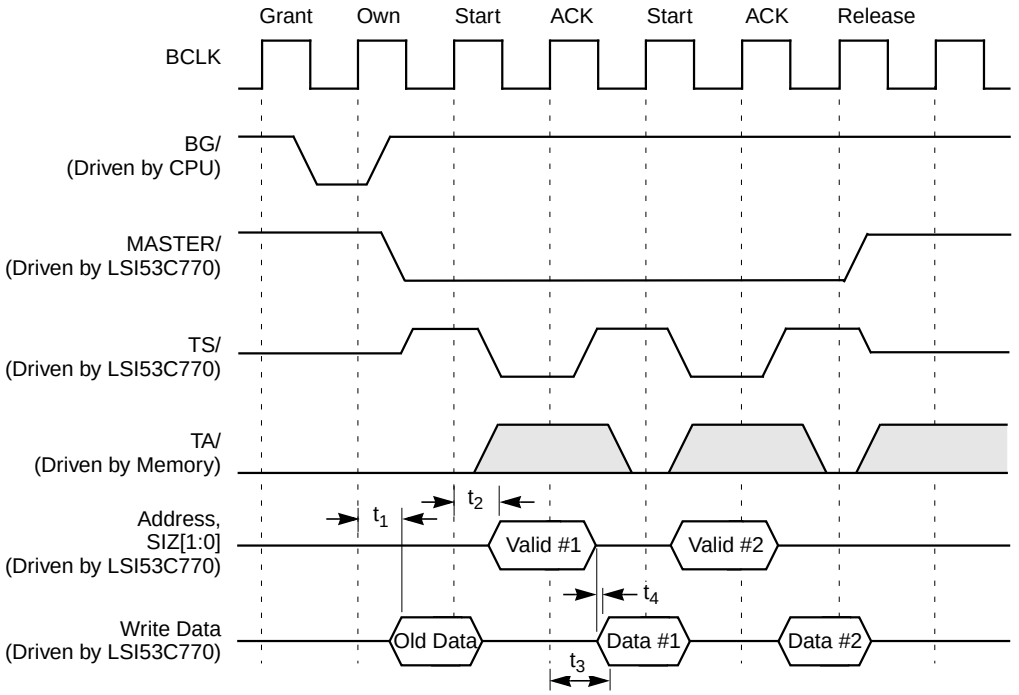


Figure 6.27 Mux Mode Write Cycle (Cache Line Burst)

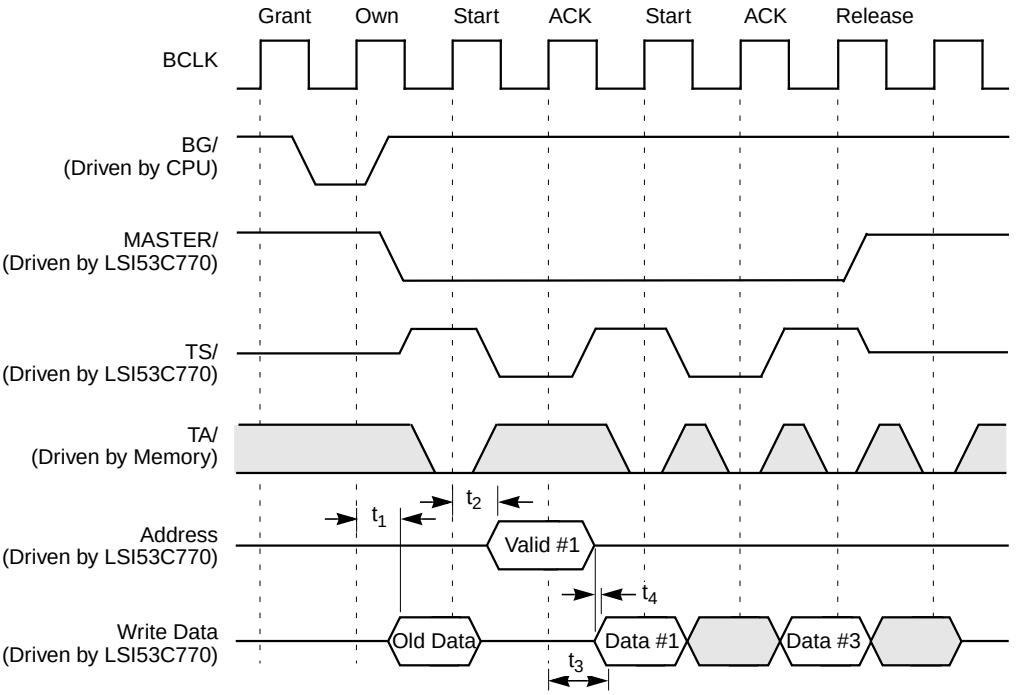


Table 6.29 Bus Mode 2 Mux Mode Write Timing

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to old data driven	–	34	ns
t_2	BCLK HIGH to address driven	5	22	ns
t_3	BCLK HIGH to new data driven	8	24	ns
t_4	Write data HIGH-Z to driven switching time	1	–	ns
t_5	BCLK HIGH to next data	–	24	ns

6.13 Bus Mode 3 and 4 Slave Cycle

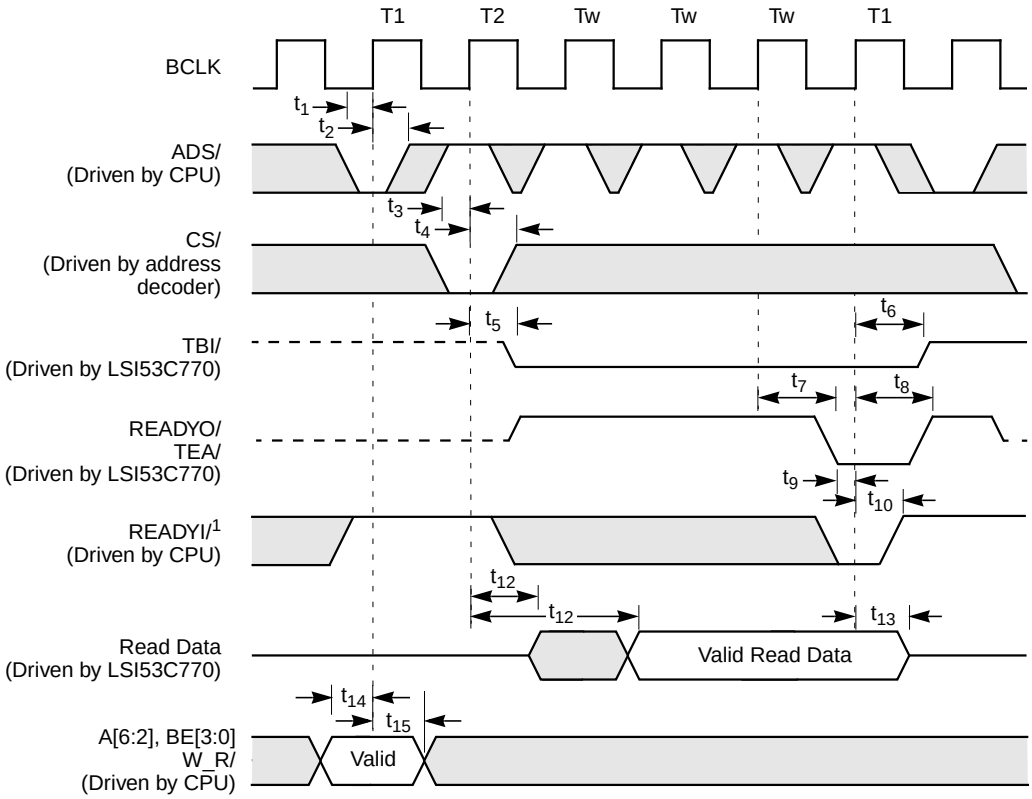
6.13.1 Bus Mode 3 and 4 Slave Read Sequence

1. Address, Address Status, Read, and the Byte Enable signals are asserted by the CPU. The waveforms in this section show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A[31:0], BHE/.
2. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. Three clock cycles of wait-state are inserted (these wait-states are required) and the Data lines are asserted.
6. Ready Out is asserted by LSI53C770, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Ready Out or Transfer Error Acknowledge is deasserted.
9. The LSI53C770 waits for Ready In to be asserted and then ends the slave cycle, if no errors are detected.
10. The Data lines are 3-stated by the LSI53C770.

6.13.1.1 Recommended Setup for Bus Mode 3 and 4

1. Disable Cache Line Burst Mode (if cache line is not supported; set Chip Test Zero (CTEST0), bit 7).
2. Set the Bus Mode bit (DMA Control (DCNTL), bit 6).
3. Set the Snoop Mode bit (Chip Test Three (CTEST3), bit 0).
4. Tie BB/ high resistively.
5. Tie TEA/ high resistively.

Figure 6.28 Bus Mode 3 and 4 Slave Read Cycle



[1] This signal may be driven by the LSI53C770 if the Enable Acknowledge bit is set (DMA Control (DCNTL), bit 5). See the explanation in Chapter 2 for use of this signal as an output.

Table 6.30 Bus Mode 3 and 4 Slave Read Timing

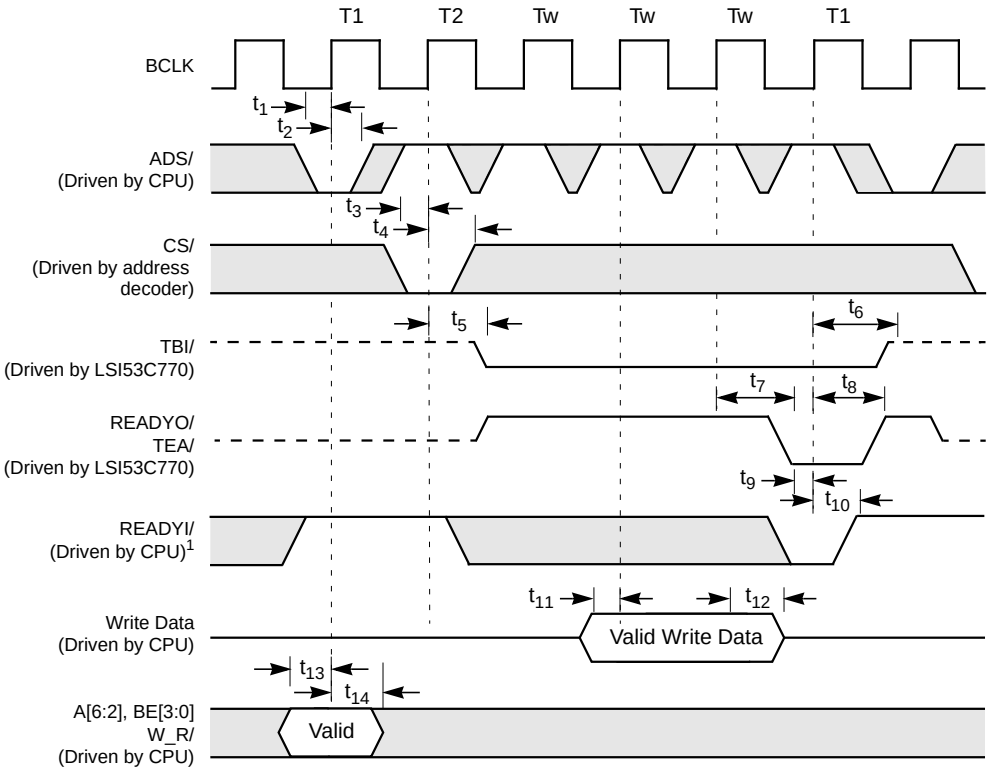
Symbol	Parameter	Min	Max	Units
t_1	ADS/ setup to BCLK HIGH	4	–	ns
t_2	ADS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after ADS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after ADS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to READYO/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to READYO/, TEA/ HIGH	4	20	ns
t_9	READYI/ setup to BCLK HIGH during or after READYO/, TEA/	9	–	ns
t_{10}	READYI/ hold from BCLK HIGH during or after READYO/, TEA/	5	–	ns
t_{11}	BCLK HIGH to data bus driven	8	28	ns
t_{12}	BCLK HIGH to read data valid	–	75	ns
t_{13}	BCLK HIGH to data bus HIGH-Z	7	34	ns
t_{14}	A[6:2], BE[3:0], R_W/ setup to BCLK HIGH[1]	4	–	ns
	A[2:6], [3:0]			
t_{15}	A[6:2], BE[3:0], R_W/ hold from BCLK HIGH[1]	12	–	ns

1. The waveforms in these selections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines, A[31:0], BHE/.

6.13.2 Bus Mode 3 and 4 Slave Write Sequence

1. The Read/Write, the address lines, and the Address Status and Byte Enable signals are asserted by the CPU. (The waveforms in this section show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A[31:0], BHE/.)
2. Chip Select is validated by the LSI53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait-state are inserted (these wait-states are required).
7. Ready Out is asserted by the LSI53C770, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. Ready Out or Transfer Error Acknowledge is deasserted.
10. The LSI53C770 waits for Ready In to be asserted and then ends the slave cycle, if there are no errors.

Figure 6.29 Bus Mode 3 and 4 Slave Write Cycle



[1] This signal may be driven by the LSI53C770 if the Enable Acknowledge bit is set (DMA Control (DCNTL), bit 5). See the explanation in Chapter 2 for use of this signal as an output.

Table 6.31 Bus Mode 3 and 4 Slave Write Timing

Symbol	Parameter	Min	Max	Units
t_1	ADS/ setup to BCLK HIGH	4	–	ns
t_2	ADS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after ADS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after ADS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to READYO/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to READYO/, TEA/ HIGH	4	20	ns
t_9	READYI/ setup to BCLK HIGH during or after READYO/, TEA/	9	–	ns
t_{10}	READYI/ hold from BCLK HIGH during or after READYO/, TEA/	5	–	ns
t_{11}	Valid write data setup to BCLK HIGH	6	–	ns
t_{12}	Valid write data hold from BCLK HIGH	14	–	ns
t_{13}	A[6:2], BE[3:0], W_R/ setup to BCLK HIGH[1]	4	–	ns
t_{14}	A[6:2], BE[3:0], W_R/ hold from BCLK HIGH[1]	12	–	ns

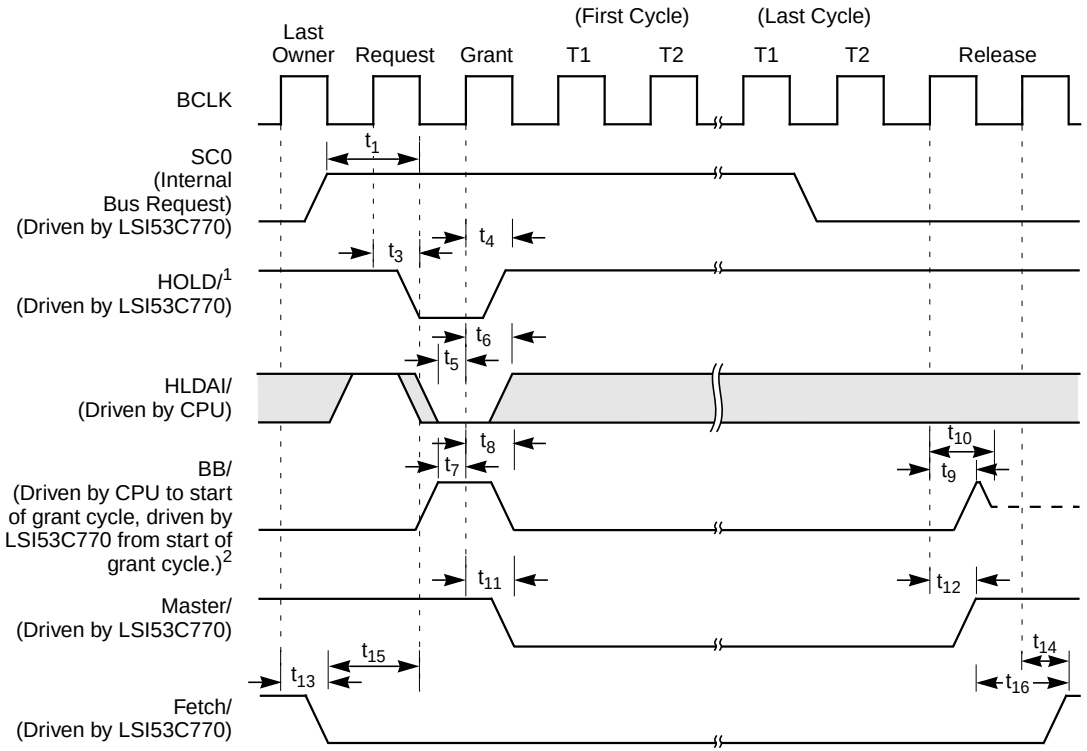
1. The waveforms in these selections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines, A[31:0], BHE/.

6.14 Bus Mode 3 and 4 Host Bus Arbitration

6.14.1 Bus Arbitration Sequence

1. The LSI53C770 internally determines bus mastership is required. FETCH/ is asserted during cycles in which the LSI53C770 is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The LSI53C770 waits for Hold Acknowledge and checks that Bus Busy is deasserted. Then the LSI53C770 asserts Hold Acknowledge and Master, and deasserts Hold.

Figure 6.30 Bus Modes 3 and 4 Host Bus Arbitration



[1] HOLD/ may be NANDed with Master/ to obtain HOLD required by the 80286 or 80386 processors.

[2] BB/ should be tied high resistively if not used.

Note: The LSI53C770 will periodically assert the HOLD/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the HLDAI/ signal to complete the normal bus arbitration and handshake. The chip no longer wants host bus access - it desasserts the HOLD/, Master/, and all control lines after on BCLK, and does not assert ADS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may then service.

Table 6.32 Bus Mode 3 and 4 Bus Arbitration Timing

Symbol	Parameter	Min	Max	Units
t_1	SC0 HIGH to HOLD/ LOW[1]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on last cycle[1]	5	28	ns
t_3	BCLK HIGH to BR/ LOW	4	20	ns
t_4	BCLK HIGH to BR/ HIGH	5	25	ns
t_5	HLDAI/ setup to BCLK HIGH (any rising edge after HOLD/)	4	–	ns
t_6	HLDAI/ hold from BCLK HIGH (any rising edge after HOLD/)	5	–	ns
t_7	BB/ setup to BCLK HIGH (any rising edge after HOLD/)	4	–	ns
t_8	BCLK HIGH to BB/ LOW	4	24	ns
t_9	BCLK HIGH to BB/ HIGH	3	19	ns
t_{10}	BCLK HIGH to BB/ HIGH-Z	7	32	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	22	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	26	ns
t_{13}	BCLK HIGH to FETCH/ LOW	5	36	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	36	ns
t_{15}	FETCH/ LOW to HOLD/ LOW	1	2	BCLK
t_{16}	BB/ HIGH to FETCH/ HIGH[2]	1	2	BCLK

1. When the Snoop Mode bit 0 of Chip Test Three (CTEST3) is set to 1.
2. During a retry operation, FETCH/ will remain low until successful completion of an opcode fetch or a fatal bus error.

6.15 Bus Mode 3 and 4 Fast Arbitration

6.15.1 Fast Arbitration Sequence

1. The LSI53C770 internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the LSI53C770 is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The LSI53C770 waits for Hold Acknowledge (HLDAI). The LSI53C770 becomes bus master asynchronously on the leading edge of HLDAI/. The the LSI53C770 asynchronously asserts Bus Busy and Master, and deasserts HOLD/.
4. The LSI53C770 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the LSI53C770 will take bus ownership on the assertion of HLDAI, regardless of the state of HOLD/ or BB/.

Figure 6.31 Bus Mode 3 and 4 Fast Arbitration

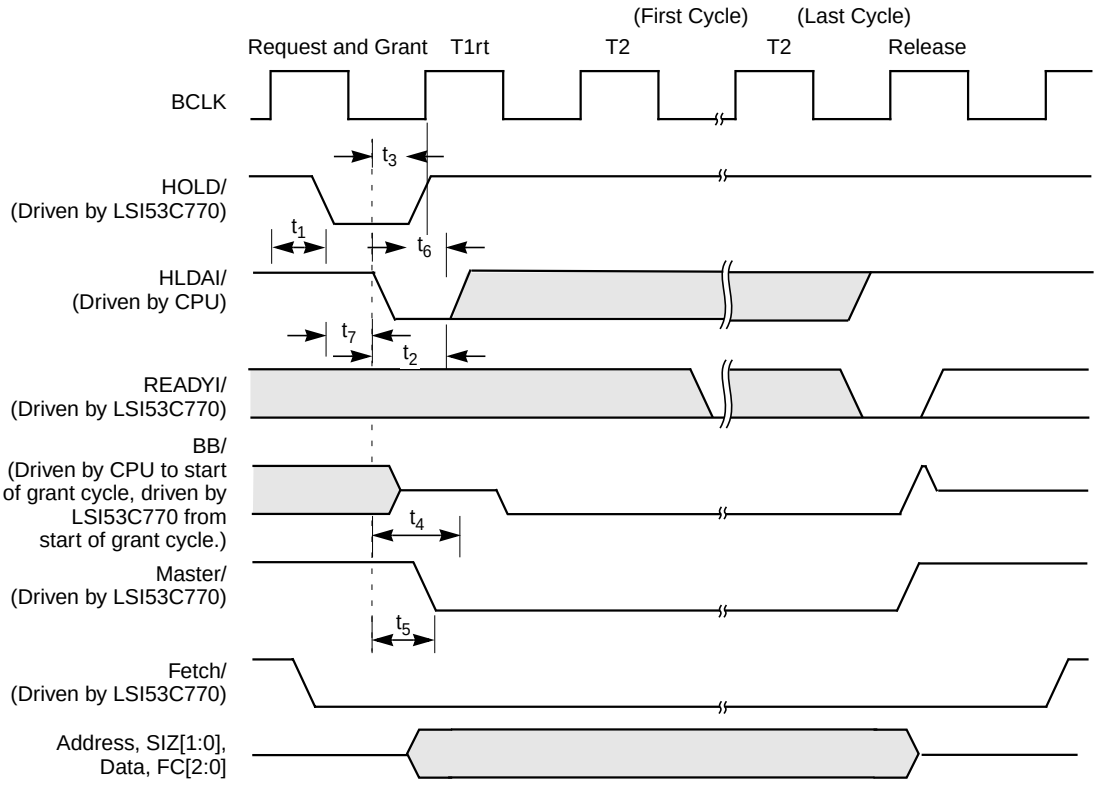


Table 6.33 Bus Mode 3 and 4 Fast Arbitration

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to HOLD/ asserted	–	20	ns
t_2	HLDAI/ setup to BCLK HIGH	12	–	ns
t_3	HLDAI/ asserted to BR/ deasserted	–	22	ns
t_4	HLDAI/ asserted to BB/ asserted	–	20	ns
t_5	HLDAI/ asserted to MASTER/ asserted	–	16	ns
t_6	HLDAI/ hold after HOLD/ deasserted[1]	0	–	ns
t_7	HOLD/ asserted to HLDAI/ asserted	0	–	ns

1. HLDAI/ may not be asserted prior to HOLD/.

6.16 Bus Mode 3 and 4 Master Cycle

6.16.1 Bus Mode 3 and 4 Bus Master Read Sequence

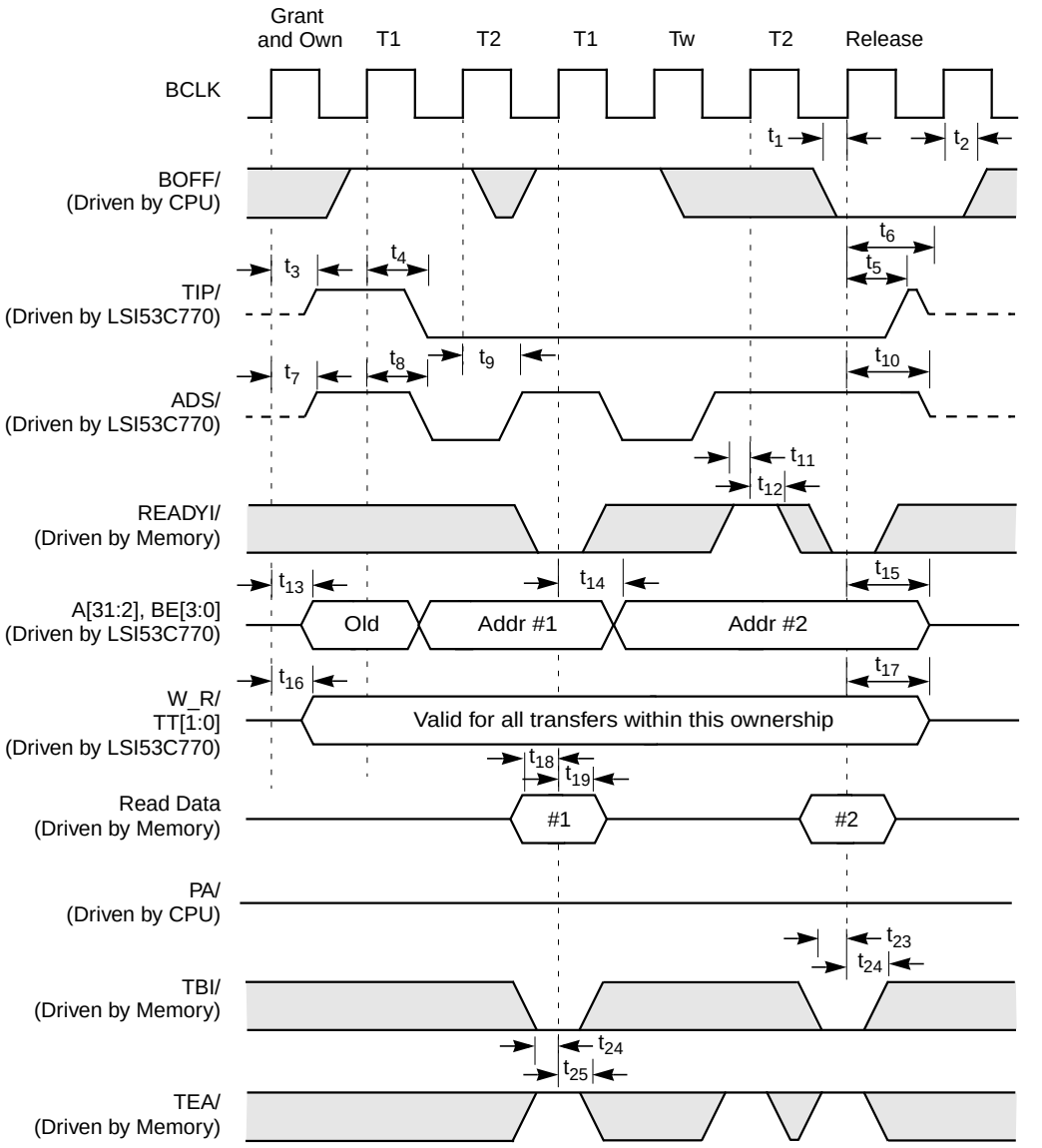
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the W_R/, Transfer Modifier and Transfer Type lines.

3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts Address Status, Address, and Byte Enable signals. The waveforms in this section show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A[31:0], BHE/.

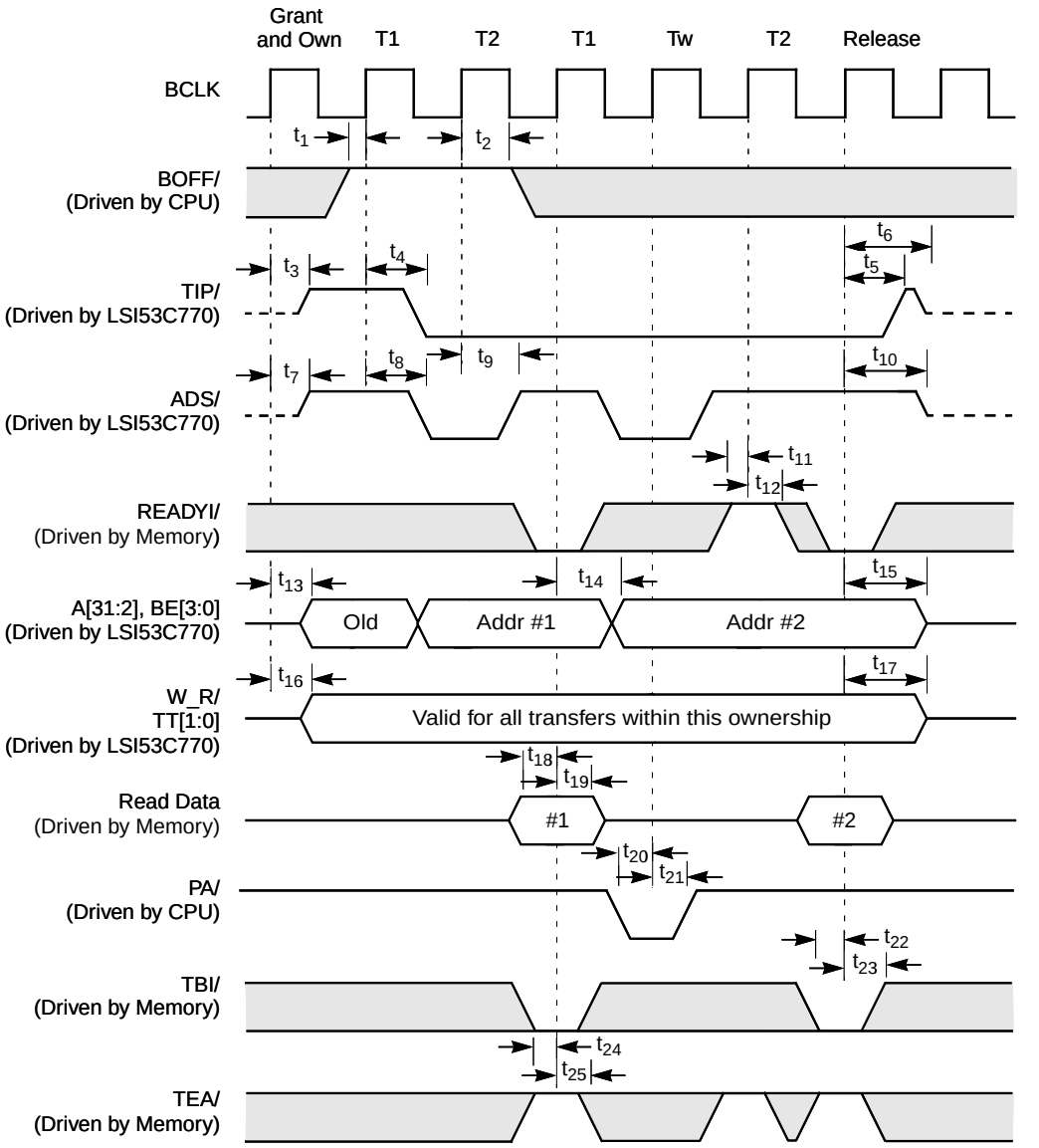
4. The LSI53C770 deasserts Address Status.
5. The LSI53C770 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted attempt cache bursting. Otherwise, proceed with noncache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Ready In is asserted and Transfer Error Acknowledge is not asserted and the LSI53C770 requires more cycles, then return to Step 3b.
6. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master, Bus Busy, and Transfer in Progress.
7. The LSI53C770 floats the Control and Address lines.

Figure 6.32 Bus Mode 3 and 4 Bus Master Read (Nonpreview of Address)



Note: This diagram shows two back-to-back cycles for a burst size of two.

Figure 6.33 Bus Mode 3 and 4 Bus Master Read (Preview of Address)



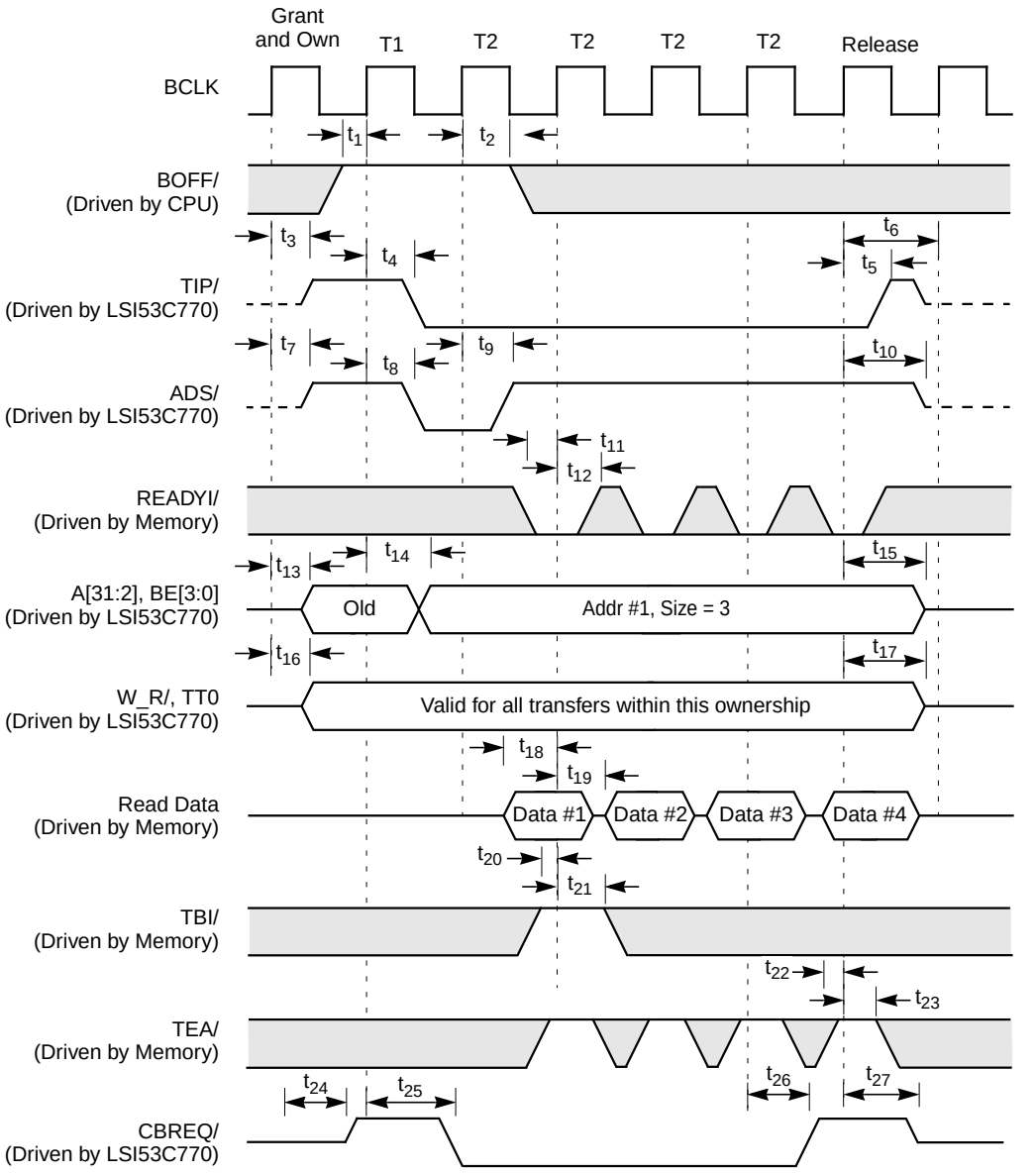
Note: This diagram shows two back-to-back cycles for a burst size of two.

Table 6.34 Bus Mode 3 and 4 Bus Master Read Timing

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK/ HIGH to ADS/ driven	5	30	ns
t_8	BCLK/ HIGH to ADS/ LOW	3	17	ns
t_9	BCLK HIGH to ADS/ HIGH	3	17	ns
t_{10}	BCLK HIGH to ADS/ HIGH-Z	7	32	ns
t_{11}	READYI/ setup to BCLK HIGH	9	–	ns
t_{12}	READYI/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:2], BE[3:0] driven[1]	5	28	ns
t_{14}	BCLK HIGH to A[31:2], BE[3:0] valid[1]	3	20	ns
t_{15}	BCLK HIGH to A[31:2], BE[3:0] HIGH-Z[1]	7	32	ns
t_{16}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	5	30	ns
t_{17}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	–	32	ns
t_{18}	Read data setup to BCLK HIGH	6	–	ns
t_{19}	Read data hold from BCLK HIGH	6	–	ns
t_{20}	PA/ setup to BCLK HIGH	5	–	ns
t_{21}	PA/ hold from BCLK HIGH	5	–	ns
t_{22}	TBI/ setup to BCLK HIGH	6	–	ns
t_{23}	TBI/ hold from BCLK HIGH	4	–	ns
t_{24}	TEA/ setup to BCLK HIGH	9	–	ns
t_{25}	TEA/ hold from BCLK HIGH	5	–	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines A[31:0], BHE/.

Figure 6.34 Bus Mode 4 Bus Master Read (Cache Line Burst)



Note: This diagram shows one cache line burst of four.

Table 6.35 Bus Mode 4 Bus Master Read Timing (Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK/ HIGH to ADS/ driven	5	30	ns
t_8	BCLK/ HIGH to ADS/ LOW	3	17	ns
t_9	BCLK HIGH to ADS/ HIGH	3	17	ns
t_{10}	BCLK HIGH to ADS/ HIGH-Z	7	32	ns
t_{11}	READYI/ setup to BCLK HIGH	9	–	ns
t_{12}	READYI/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:2], BE[3:0] driven[1]	5	28	ns
t_{14}	BCLK HIGH to A[31:2], BE[3:0] valid[1]	3	20	ns
t_{15}	BCLK HIGH to A[31:2], BE[3:0] HIGH-Z[1]	7	32	ns
t_{16}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	5	30	ns
t_{17}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	5	32	ns
t_{18}	Read data setup to BCLK HIGH	6	–	ns
t_{19}	Read data hold from BCLK HIGH	6	–	ns
t_{20}	TBI/ setup to BCLK HIGH	6	–	ns
t_{21}	TBI/ hold from BCLK HIGH	4	–	ns
t_{22}	TEA/ setup to BCLK HIGH	9	–	ns
t_{23}	TEA/ hold from BCLK HIGH	5	–	ns
t_{24}	BCLK HIGH to CBREQ/ driven	5	28	ns
t_{25}	BCLK HIGH to CBREQ/ LOW	5	20	ns
t_{26}	BCLK HIGH to CBREQ/ HIGH	5	20	ns
t_{27}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines A[31:0], BHE/.

6.16.2 Bus Mode 3 and 4 Bus Master Write Sequence

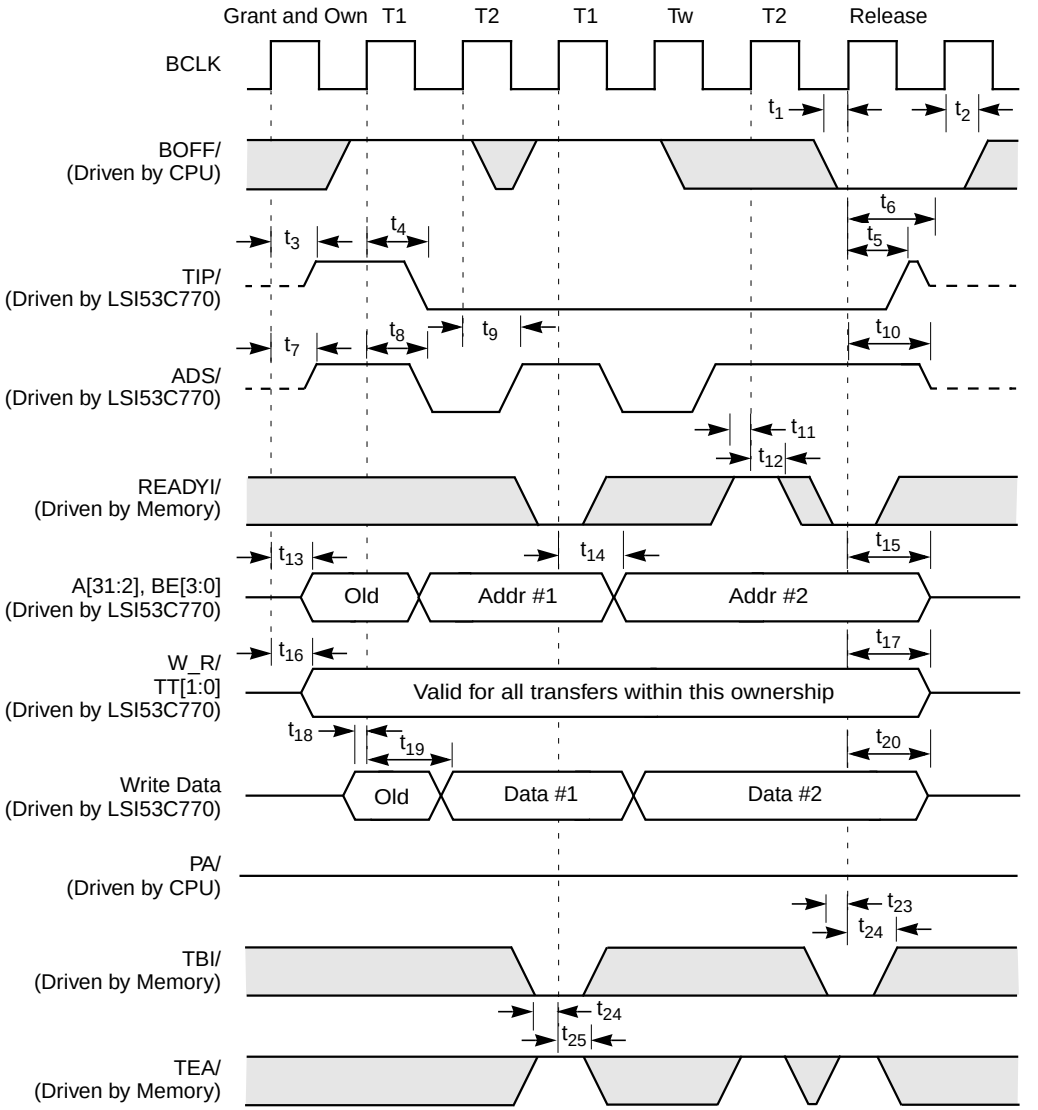
1. The LSI53C770 has attained bus mastership.
2. The LSI53C770 asserts the W_R/, Transfer Modifier, and Transfer Type lines.

3a. The LSI53C770 asserts Transfer in Progress.

3b. The LSI53C770 asserts the Address Status and Byte Enable signals, and the Address and Data lines.

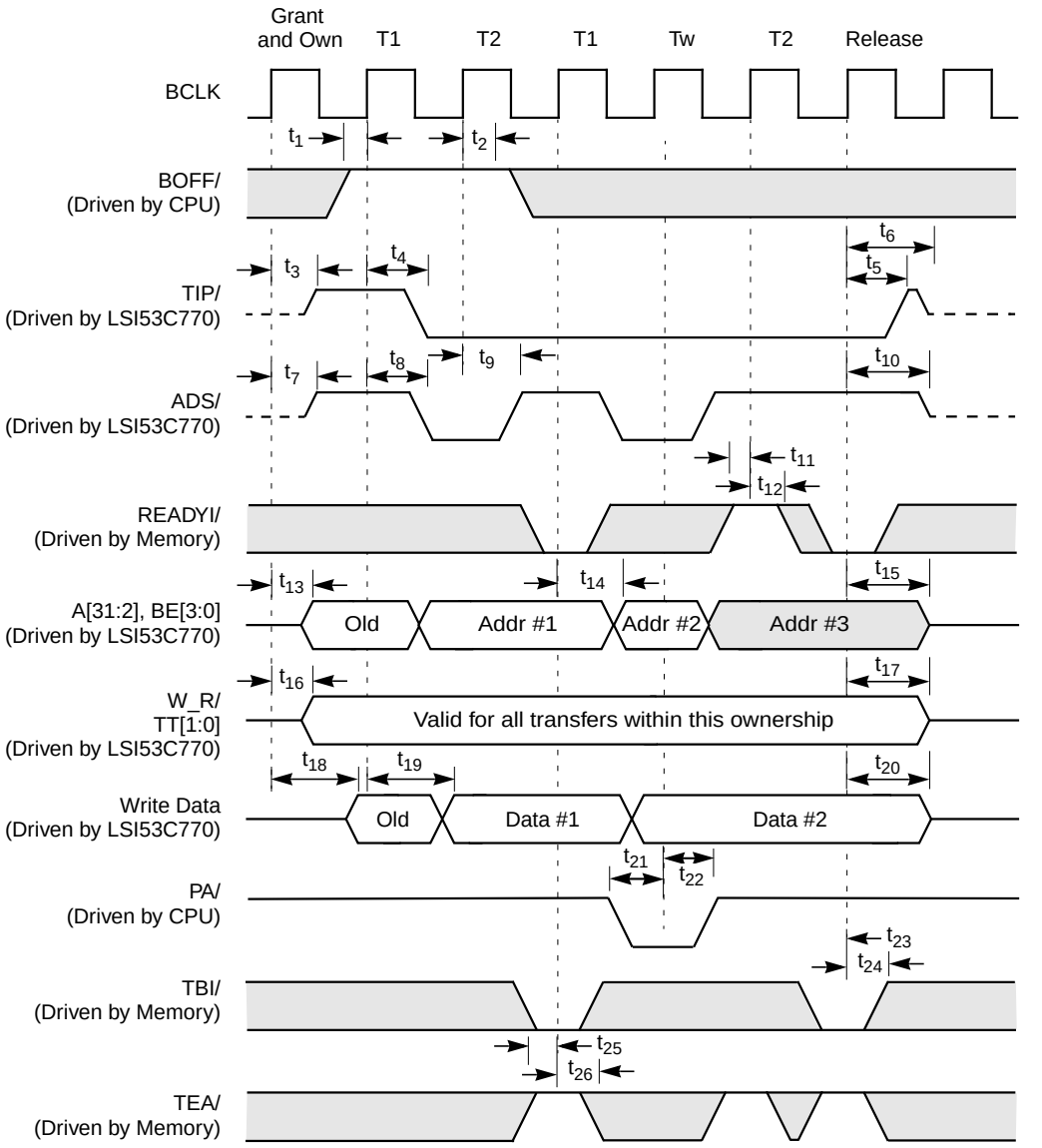
4. The LSI53C770 deasserts Address Status.
5. The LSI53C770 waits for Ready In, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted and the LSI53C770 requires more cycles, then return to Step 3b.
6. Upon acknowledgment of the last bus cycle, the LSI53C770 deasserts Master, Busy, and Transfer in Progress.
7. The LSI53C770 floats the Control, Address, and Data Lines.

Figure 6.35 Bus Mode 3 and 4 Bus Master Write (Nonpreview of Address)



Note: This diagram shows two back-to-back transfers for a transfer size of two.

Figure 6.36 Bus Mode 3 and 4 Bus Master Write (Preview of Address)



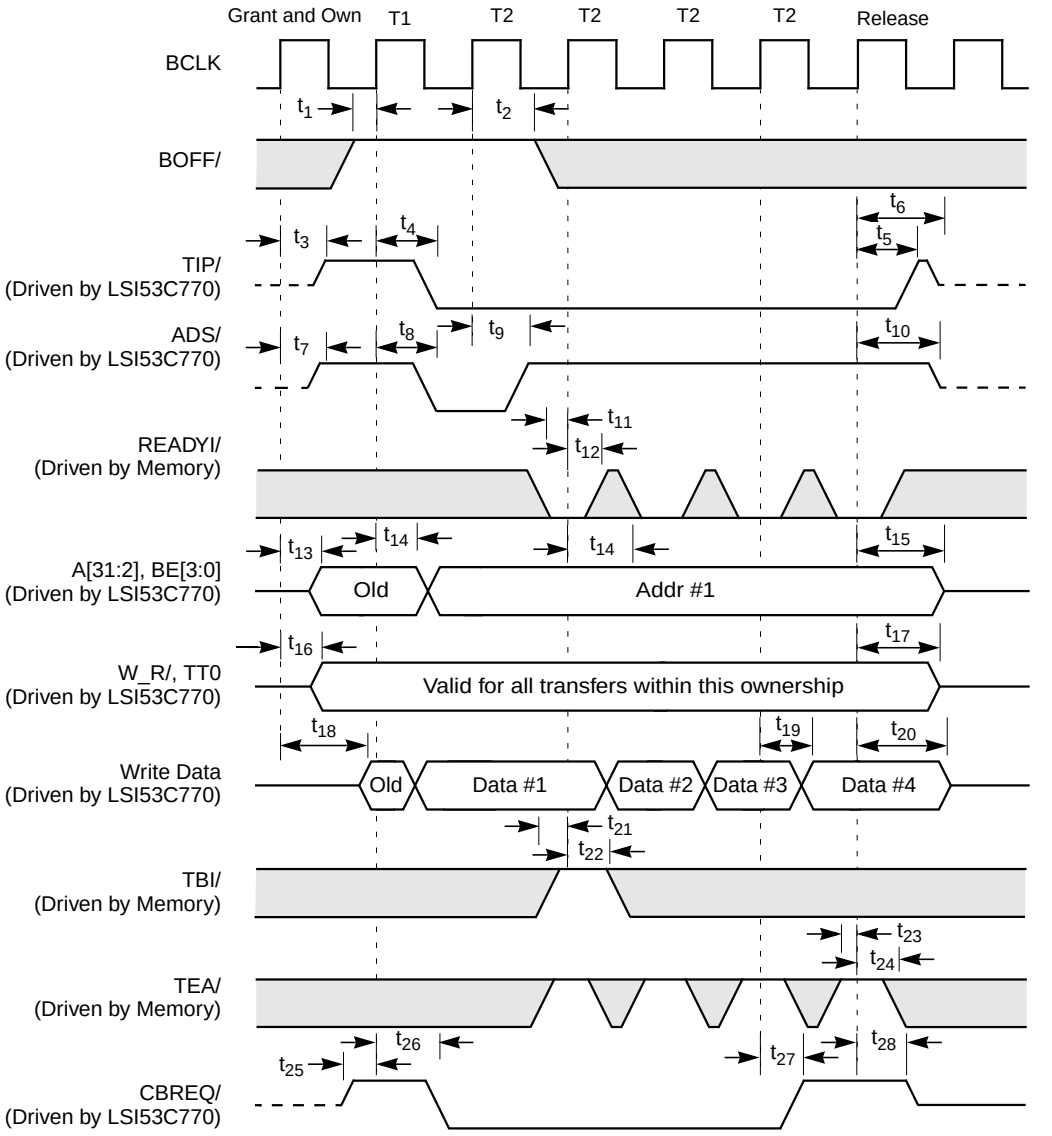
Note: This diagram shows two back-to-back transfers for a burst size of two.

Table 6.36 Bus Mode 3 and 4 Bus Master Write Timing

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK/ HIGH to ADS/ driven	5	30	ns
t_8	BCLK/ HIGH to ADS/ LOW	3	17	ns
t_9	BCLK HIGH to ADS/ HIGH	4	17	ns
t_{10}	BCLK HIGH to ADS/ HIGH-Z	7	32	ns
t_{11}	READYI/ setup to BCLK HIGH	9	–	ns
t_{12}	READYI/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:2], BE[3:0] driven[1]	5	28	ns
t_{14}	BCLK HIGH to A[31:2], BE[3:0] valid[1]	3	20	ns
t_{15}	BCLK HIGH to A[31:2], BE[3:0] HIGH-Z[1]	7	32	ns
t_{16}	BCLK HIGH to W_R/, TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	5	32	ns
t_{18}	BCLK HIGH to write data driven	5	34	ns
t_{19}	BCLK HIGH to write data valid	5	24	ns
t_{20}	BCLK HIGH to write data HIGH-Z	5	30	ns
t_{21}	PA/ setup to BCLK HIGH	5	–	ns
t_{22}	PA/ hold from BCLK HIGH	5	–	ns
t_{23}	TBI/ setup to BCLK HIGH	6	–	ns
t_{24}	TBI/ hold from BCLK HIGH	4	–	ns
t_{25}	TEA/ setup to BCLK HIGH	9	–	ns
t_{26}	TEA/ hold from BCLK HIGH	5	–	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines A[31:0], BHE/.

Figure 6.37 Bus Mode 4 Bus Master Write (Cache Line Burst)



Note: This diagram shows one cache line burst of four.

Table 6.37 Bus Mode 4 Bus Master Write Timing (Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	20	ns
t_5	BCLK HIGH to TIP/ HIGH	3	20	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK/ HIGH to ADS/ driven	5	30	ns
t_8	BCLK/ HIGH to ADS/ LOW	3	17	ns
t_9	BCLK HIGH to ADS/ HIGH	3	17	ns
t_{10}	BCLK HIGH to ADS/ HIGH-Z	7	32	ns
t_{11}	READYI/ setup to BCLK HIGH	9	–	ns
t_{12}	READYI/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:2], BE[3:0] driven[1]	5	28	ns
t_{14}	BCLK HIGH to A[31:2], BE[3:0] valid[1]	3	20	ns
t_{15}	BCLK HIGH to A[31:2], BE[3:0] HIGH-Z[1]	7	32	ns
t_{16}	BCLK HIGH to W_R/, TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to W_R/, TT[1:0] HIGH-Z	5	32	ns
t_{18}	BCLK HIGH to write data driven	5	34	ns
t_{19}	BCLK HIGH to write data valid	5	24	ns
t_{20}	BCLK HIGH to write data HIGH-Z	5	30	ns
t_{21}	TBI/ setup to BCLK HIGH	6	–	ns
t_{22}	TBI/ hold from BCLK HIGH	4	–	ns
t_{23}	TEA/ setup to BCLK HIGH	9	–	ns
t_{24}	TEA/ hold from BCLK HIGH	5	–	ns
t_{25}	BCLK/ HIGH to CBREQ/ driven	5	28	ns
t_{26}	BCLK/ HIGH to CBREQ LOW	5	20	ns
t_{27}	BCLK HIGH to CBREQ/ HIGH	5	20	ns
t_{26}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A[31:2], BE[3:0]. These waveforms also apply to the Bus Mode 3 address/byte enable lines A[31:0], BHE/.

6.17 SCSI Timing Diagrams

Figure 6.38 through Figure 6.42 and Table 6.38 through Table 6.47 describe the LSI53C770 SCSI timing.

Figure 6.38 Initiator Asynchronous Send

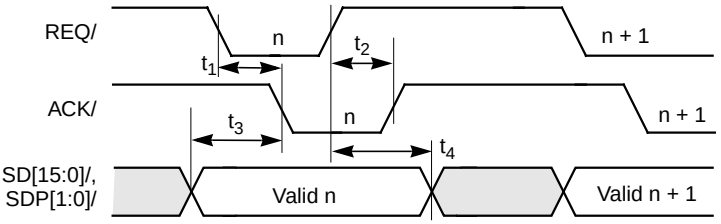


Table 6.38 Initiator Asynchronous Send Timing

Symbol	Parameter	Min	Max	Units
t_1	ACK/ asserted from REQ/ asserted	10	–	ns
t_2	ACK/ deasserted from REQ/ deasserted	10	–	ns
t_3	Data setup to ACK/ asserted	55	–	ns
t_4	Data hold from REQ/ deasserted	20	–	ns

Figure 6.39 Initiator Asynchronous Receive

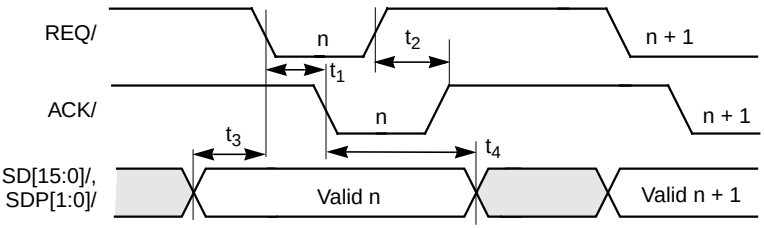


Table 6.39 Initiator Asynchronous Receive Timing

Symbol	Parameter	Min	Max	Units
t_1	ACK/ asserted from REQ/ asserted	10	–	ns
t_2	ACK/ deasserted from REQ/ deasserted	10	–	ns
t_3	Data setup to REQ/ asserted	0	–	ns
t_4	Data hold from ACK/ deasserted	0	–	ns

Figure 6.40 Target Asynchronous Send

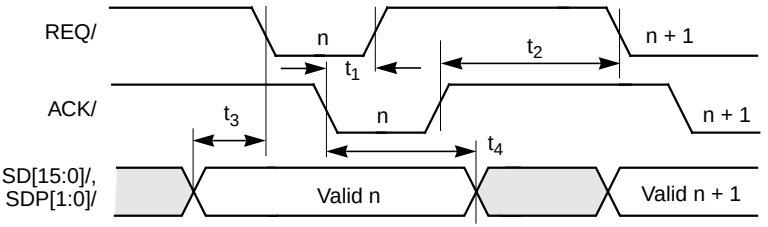


Table 6.40 Target Asynchronous Send Timing

Symbol	Parameter	Min	Max	Units
t_1	REQ/ deasserted from ACK/ asserted	10	–	ns
t_2	REQ/ asserted from ACK/ deasserted	10	–	ns
t_3	Data setup to REQ/ asserted	55	–	ns
t_4	Data hold from ACK/ asserted	20	–	ns

Figure 6.41 Target Asynchronous Receive

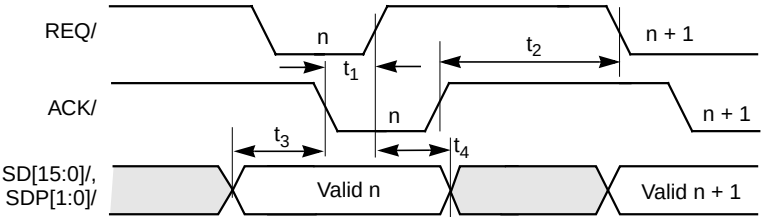


Table 6.41 Target Asynchronous Receive Timing

Symbol	Parameter	Min	Max	Units
t_1	REQ/ deasserted from ACK/ asserted	10	–	ns
t_2	REQ/ asserted from ACK/ deasserted	10	–	ns
t_3	Data setup to ACK/ asserted	0	–	ns
t_4	Data hold from REQ/ deasserted	0	–	ns

Figure 6.42 Initiator and Target Synchronous Transfers

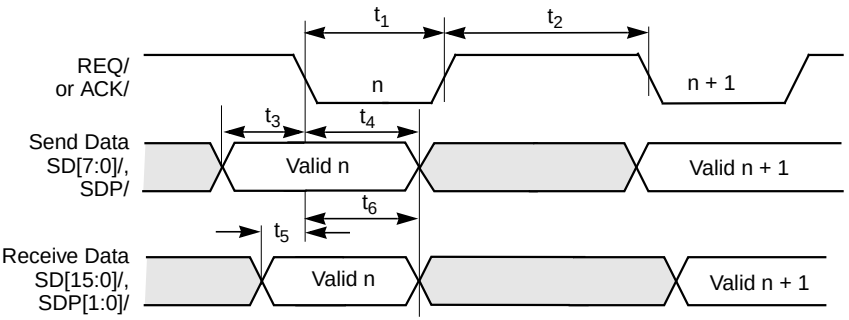


Table 6.42 SCSI-1 Transfers (SE 5.0 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	90	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	90	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	90	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	90	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	55	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	100	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	45	–	ns

Table 6.43 SCSI-1 Transfers (Differential, 4.17 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	96	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	96	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	84	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	84	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	65	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	110	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	45	–	ns

Table 6.44 SCSI-2 Fast Transfers (10.0 Mbytes/s, 40 MHz Clock)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	35	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	35	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	20	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	33	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	45	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	10	–	ns

Table 6.45 SCSI-2 Fast Transfers (10.0 Mbytes/s, 50 MHz Clock)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	35	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	35	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	20	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	33	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	40[1]	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	10	–	ns

1. Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.

Note: For fast SCSI, the TolerANT Enable bit (SCSI Test Register Three (STEST3), bit 7) should be set. Transfer period bits (Bits [6:4] in SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (Bit 7 in SCSI Control One (SCNTL1)) is set.

Table 6.46 Ultra SCSI SE Transfers (20.0 Mbytes/s (8-Bit Transfers) or 40.0 Mbytes/s (16-Bit Transfers), 80 or 100 MHz Clock)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

Note: For fast SCSI, the TolerANT Enable bit (SCSI Test Register Three (STEST3), bit 7) should be set. During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (SCSI Test Register Two (STEST2), bit 1) has no effect. Transfer period bits (Bits [6:4] in SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (Bit 7 in SCSI Control One (SCNTL1)) is set.

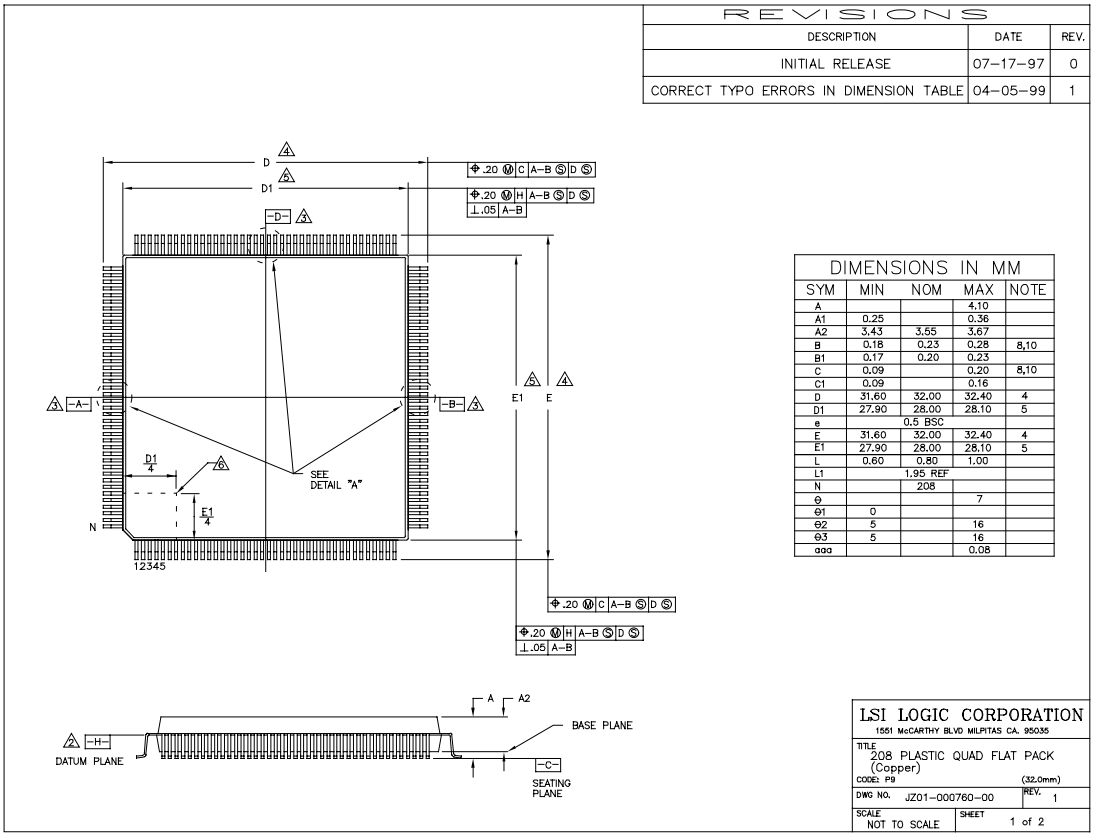
Table 6.47 Ultra SCSI Differential Transfers (20.0 Mbytes/s (8-Bit Transfers) or 40.0 Mbytes/s (16-Bit Transfers), 80 or 100 MHz Clock)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	16	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	21	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

Note: For fast SCSI, the TolerANT Enable bit (SCSI Test Register Three (STEST3), bit 7) should be set. During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (SCSI Test Register Two (STEST2), bit 1) has no effect. Transfer period bits (Bits [6:4] in SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (Bit 7 in SCSI Control One (SCNTL1)) is set.

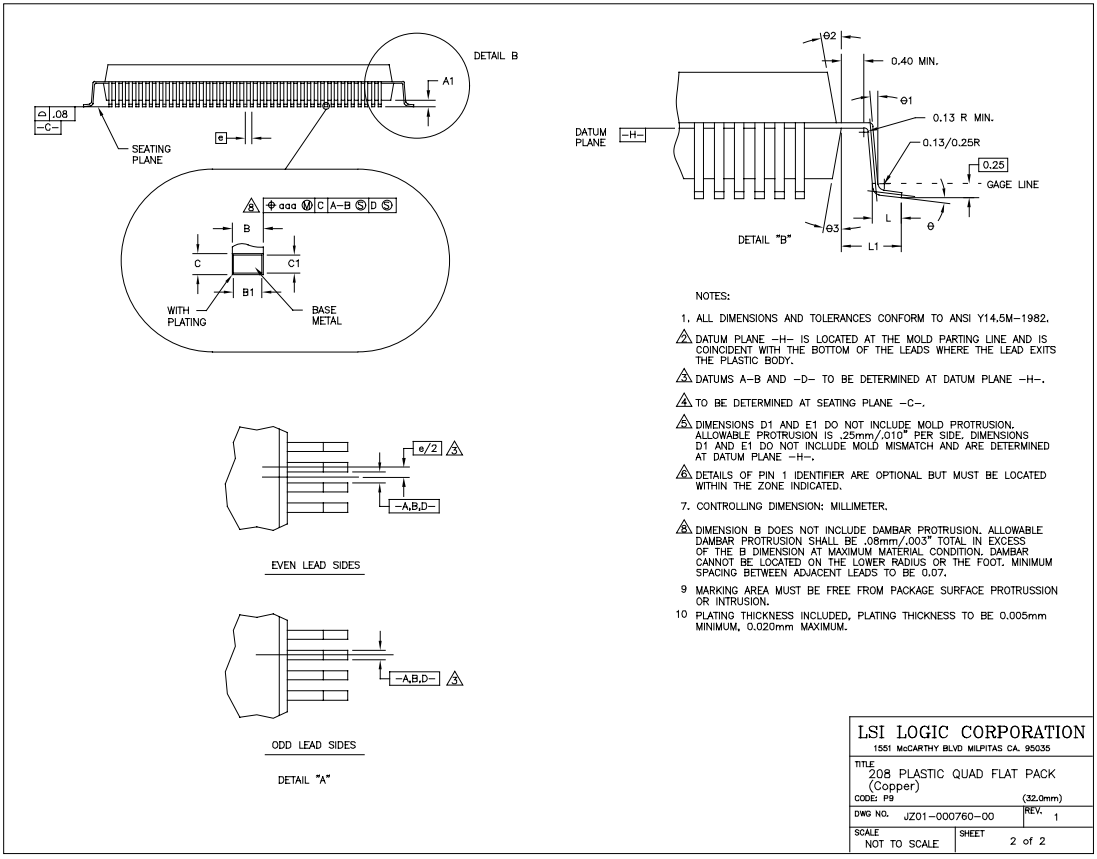
6.18 Package Drawings

Figure 6.43 208-Pin PQFP (P9) Mechanical Drawing (Sheet 1 of 2)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code P9.**

Figure 6.43 208-Pin PQFP (P9) Mechanical Drawing (Sheet 2 of 2)



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Appendix A
Register Summary

Table A.1 lists the LSI53C770 registers by register name.

Table A.1 LSI53C770 Register Summary

Register Name	Little Endian/Big Endian	Read/Write	Page
Adder Sum Output (ADDER)	0x3C–0x3F (0x3C–0x3F)	Read Only	4-56
Chip Test Five (CTEST5)	0x22 (0x21)	Read/Write	4-42
Chip Test Four (CTEST4)	0x21 (0x22)	Read/Write	4-40
Chip Test One (CTEST1)	0x19 (0x1A)	Read Only	4-36
Chip Test Six (CTEST6)	0x23 (0x20)	Read/Write	4-44
Chip Test Three (CTEST3)	0x1B (0x18)	Read/Write	4-38
Chip Test Two (CTEST2)	0x1A (0x19)	Read Only	4-37
Chip Test Zero (CTEST0)	0x18 (0x1B)	Read/Write	4-34
Data Structure Address (DSA)	0x10–0x13 (0x10–0x13)	Read/Write	4-30
DMA Byte Counter (DBC)	0x24–0x26 (0x25–0x27)	Read/Write	4-45
DMA Command (DCMD)	0x27 (0x24)	Read/Write	4-46
DMA Control (DCNTL)	0x3B (0x38)	Read/Write	4-54
DMA FIFO (DFIFO)	0x20 (0x23)	Read/Write	4-40
DMA Interrupt Enable (DIEN)	0x39 (0x3A)	Read/Write	4-52
DMA Mode (DMODE)	0x38 (0x3B)	Read/Write	4-48
DMA Next Data Address (DNAD)	0x28–0x2B (0x28–0x2B)	Read/Write	4-46
DMA SCRIPTS Pointer (DSP)	0x2C–0x2F (0x2C–0x2F)	Read/Write	4-46
DMA SCRIPTS Pointer Save (DSPS)	0x30–0x33 (0x30–0x33)	Read/Write	4-47

Table A.1 LSI53C770 Register Summary (Cont.)

Register Name	Little Endian/Big Endian	Read/Write	Page
DMA Status (DSTAT)	0x0C (0x0F)	Read Only	4-23
DMA Watchdog Timer (DWT)	0x3A (0x39)	Read/Write	4-53
General Purpose (GPREG)	0x07 (0x04)	Read/Write	4-20
General Purpose Control (GPCNTL)	0x47 (0x44)	Read/Write	4-68
Interrupt Status (ISTAT)	0x14 (0x17)	Read/Write	4-30
Memory Access Control (MACNTL)	0x46 (0x45)	Read/Write	4-67
Response ID One (RESPID1)	0x4B (0x48)	Read/Write	4-71
Response ID Zero (RESPID0)	0x4A (0x49)	Read/Write	4-71
Scratch Register A (SCRATCHA)	0x34–0x37 (0x34–0x37)	Read/Write	4-47
Scratch Register B (SCRATCHB)	0x5C–0x5F	Read/Write	4-80
Scratch Registers C–J (SCRATCHC–J)	0x60–0x7F	Read/Modify/Write	4-80
SCSI Bus Control Lines (SBCL)	0x0B (0x08)	Read Only	4-23
SCSI Bus Data Lines (SBDL)	0x58–0x59 (0x5A–0x5B)	Read Only	4-79
SCSI Chip ID (SCID)	0x04 (0x07)	Read/Write	4-14
SCSI Control One (SCNTL1)	0x01 (0x02)	Read/Write	4-6
SCSI Control Register Two (SCNTL2)	0x02 (0x01)	Read/Write	4-10
SCSI Control Three (SCNTL3)	0x03 (0x00)	Read/Write	4-12
SCSI Control Zero (SCNTL0)	0x00 (0x03)	Read/Write	4-3
SCSI Destination ID (SDID)	0x06 (0x05)	Read/Write	4-19
SCSI First Byte Received (SFBR)	0x08 (0x0B)	Read/Write	4-20
SCSI Input Data Latch (SIDL)	0x50–0x51 (0x52–0x53)	Read Only	4-78
SCSI Interrupt Enable One (SIEN1)	0x41 (0x42)	Read/Write	4-59
SCSI Interrupt Enable Zero (SIEN0)	0x40 (0x43)	Read/Write	4-57
SCSI Interrupt Status One (SIST1)	0x43 (0x40)	Read Only	4-64
SCSI Interrupt Status Zero (SIST0)	0x42 (0x41)	Read Only	4-61

Table A.1 LSI53C770 Register Summary (Cont.)

Register Name	Little Endian/Big Endian	Read/Write	Page
SCSI Longitudinal Parity (SLPAR)	0x44 (0x47)	Read/Write	4-65
SCSI Output Control Latch (SOCL)	0x09 (0x0A)	Read/Write	4-21
SCSI Output Data Latch (SODL)	0x54–0x55 (0x56–0x57)	Read/Write	4-79
SCSI Selector ID Register (SSID)	0x0A (0x09)	Read Only	4-22
SCSI Status One (SSTAT1)	0x0E (0x0D)	Read Only	4-27
SCSI Status Two (SSTAT2)	0x0F (0x0C)	Read Only	4-28
SCSI Status Zero (SSTAT0)	0x0D (0x0E)	Read Only	4-25
SCSI Test Register One (STEST1)	0x4D (0x4E)	Read Only	4-73
SCSI Test Register Three (STEST3)	0x4F (0x4C)	Read/Write	4-76
SCSI Test Register Two (STEST2)	0x4E (0x4D)	Read/Write	4-74
SCSI Test Register Zero (STEST0)	0x4C (0x4F)	Read Only	4-72
SCSI Timer Register 0 (STIME0)	0x48 (0x4B)	Read/Write	4-69
SCSI Timer Register One (STIME1)	0x49 (0x4A)	Read/Write	4-70
SCSI Transfer (SXFER)	0x05 (0x06)	Read/Write	4-15
SCSI Wide Residue Data (SWIDE)	0x45 (0x46)	Read Only	4-67
Temporary Stack (TEMP)	0x1C–0x1F (0x1C–0x1F)	Read/Write	4-39

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B. M. Tel: 770.980.4922
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I. E. Tel: 678.584.0812

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A. E. Tel: 801.365.3800
W. E. Tel: 801.974.9953

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Tel: 314.291.5350
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B. M. Tel: 847.413.8530
W. E. Tel: 800.853.9953
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I. E. Tel: 847.885.9700

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I. E. Tel: 219.436.4250
W. E. Tel: 888.358.9953
Indianapolis
A. E. Tel: 317.575.3500

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W. E. Tel: 612.853.2280
Cedar Rapids
A. E. Tel: 319.393.0033

Kansas
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A. E. Tel: 913.663.7900
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I. E. Tel: 913.492.0408

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W. E. Tel: 937.436.9953
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Tel: 800.767.0329
Tel: 800.829.0146

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W. E. Tel: 713.854.9953
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A. E. Tel: 800.231.0253
Tel: 800.231.5575

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A. E. Tel: 800.272.9255
W. E. Tel: 781.271.9953

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W. E. Tel: 800.863.9953
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B. M. Tel: 800.673.7461
I. E. Tel: 410.381.3131

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I. E. Tel: 612.525.9999

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W. E. Tel: 256.830.1119

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A. E. Tel: 314.291.5350
I. E. Tel: 314.872.2182

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I. E. Tel: 609.222.9566
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W. E. Tel: 800.862.9953
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W. E. Tel: 973.237.9010

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A. E. Tel: 505.293.5119

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A. E. Tel: 516.434.7400
W. E. Tel: 800.861.9953
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A. E. Tel: 716.475.9130
I. E. Tel: 716.242.7790
W. E. Tel: 800.319.9953
Smithtown
B. M. Tel: 800.543.2008
Syracuse
A. E. Tel: 315.449.4927

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I. E. Tel: 919.873.9922
W. E. Tel: 800.560.9953

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W. E. Tel: 612.853.2280

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Cleveland
A. E. Tel: 216.498.1100
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A. E. Tel: 614.888.3313
I. E. Tel: 937.253.7501
W. E. Tel: 800.575.9953
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B. M. Tel: 440.238.0404
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I. E. Tel: 216.520.4333

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W. E. Tel: 972.235.9953
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A. E. Tel: 918.459.6000
I. E. Tel: 918.665.4664

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Beavertonr
B. M. Tel: 503.524.0787
I. E. Tel: 503.644.3300
Portland
A. E. Tel: 503.526.6200
W. E. Tel: 800.879.9953

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Mercer
I. E. Tel: 412.662.2707
Pittsburgh
A. E. Tel: 412.281.4150
W. E. Tel: 440.248.9996
Philadelphia
A. E. Tel: 800.526.4812
B. M. Tel: 215.741.4080
W. E. Tel: 800.871.9953

Rhode Island
A. E. 800.272.9255
W. E. Tel: 781.271.9953

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A. E. Tel: 919.872.0712
W. E. Tel: 919.469.1502

South Dakota
A. E. Tel: 800.829.0116
W. E. Tel: 612.853.2280

Tennessee
W. E. Tel: 256.830.1119
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A. E. Tel: 800.241.8182
Tel: 800.633.2918

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W. E. Tel: 800.955.9953
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W. E. Tel: 800.888.9953
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I. E. Tel: 972.783.0800
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A. E. Tel: 210.412.2047
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B. M. Tel: 801.295.3900
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Salt Lake City
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SGY Synergy Associates, Inc.

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E. A. Tel: 480.921.3305

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Calabasas
I. S. Tel: 818.880.6480
Irvine
I. S. Tel: 714.833.0300
San Diego
E. A. Tel: 619.278.5441

Illinois
Elmhurst
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Indiana
Cicero
R. A. Tel: 317.984.8608
Ligonier
R. A. Tel: 219.894.3184
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R. A. Tel: 317.838.0360

Massachusetts
Burlington
SGY Tel: 781.238.0870

Michigan
Byron Center
R. A. Tel: 616.554.1460
Good Rich
R. A. Tel: 810.636.6060
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R. A. Tel: 810.615.4000

North Carolina
Cary
GRP Tel: 919.481.1530

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Columbus
R. A. Tel: 614.457.2242
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Independence
R. A. Tel: 216.447.8825

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R. A. Tel: 814.445.6976

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ION Tel: 817.695.8000
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ION Tel: 281.376.2000

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