NEC

MOS INTEGRATED CIRCUIT
μPD23C16300

16M-BIT MASK-PROGRAMMABLE ROM
2M-WORD BY 8-BIT (BYTE MODE) / 1M-WORD BY 16-BIT (WORD MODE)

Description

The μPD23C16300 is a 16,777,216 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 2,097,152 words by 8 bits, WORD mode : 1,048,576 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C16300 is packed in 48-pin PLASTIC TSOP(I) and 48-pin TAPE FBGA.

Features

- Pin compatible with NOR Flash Memory
- Word organization
  - 2,097,152 words by 8 bits (BYTE mode)
  - 1,048,576 words by 16 bits (WORD mode)
- Operating supply voltage : V_{CC} = 2.7 V to 3.6 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
3.0 V ± 0.3 V	90	30	30
3.3 V ± 0.3 V	85		

Ordering Information

Part Number	Package
μPD23C16300GZ-xxx-MJH	48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)
μPD23C16300F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)

(xxx : ROM code suffix No.)

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The mark ★ shows major revised points.

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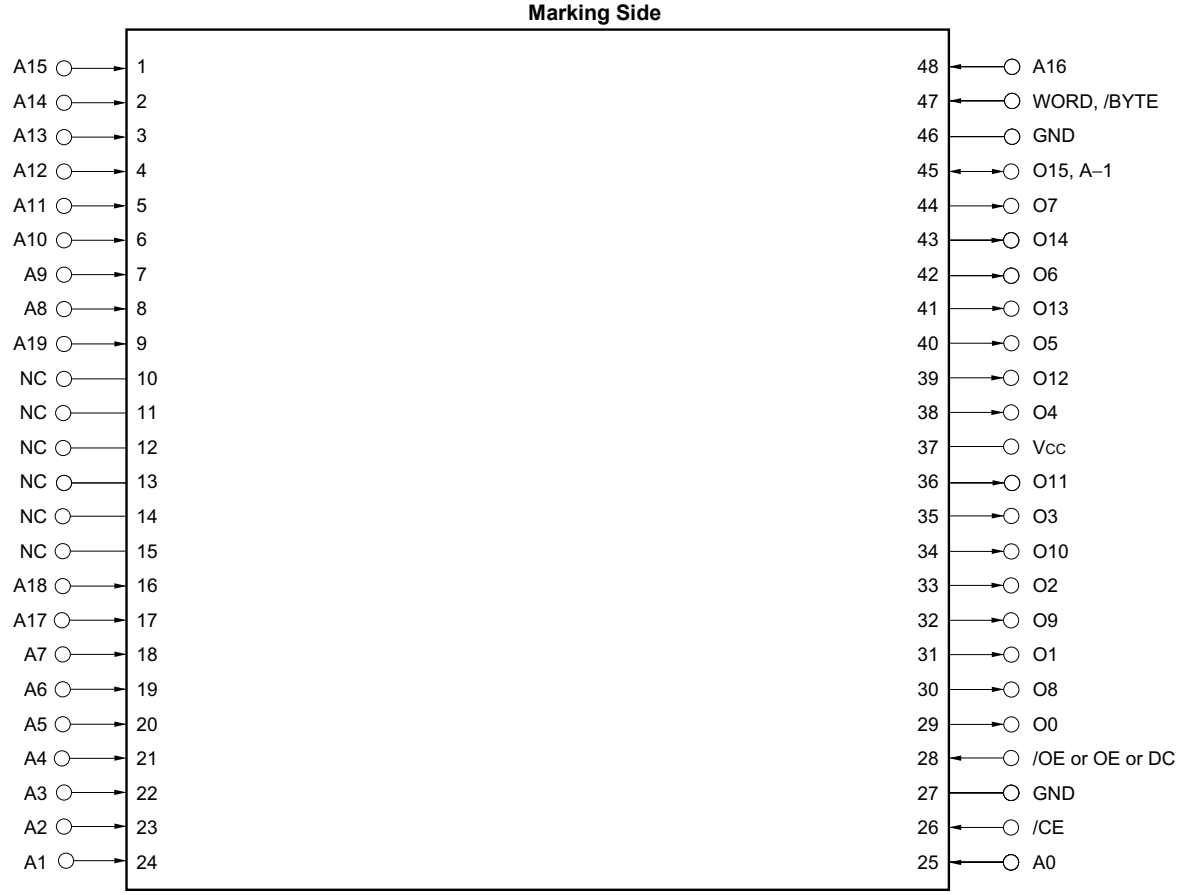
Pin Configurations

/xxx indicates active low signal.

48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

[μPD23C16300GZ-xxx-MJH]

Marking Side



A0 to A19	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE or OE	:	Output Enable
V_{CC}	:	Supply voltage
GND	:	Ground
NC [Note]	:	No Connection
DC	:	Don't Care

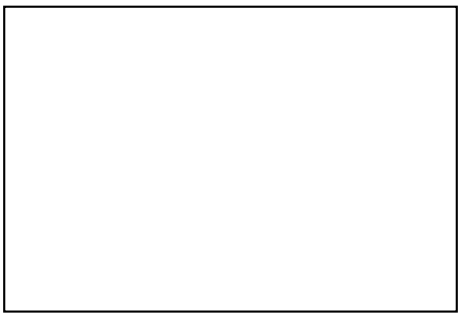
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin TAPE FBGA (8 x 6)

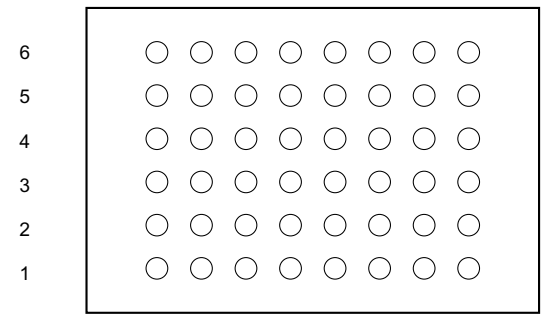
[μPD23C16300F9-xxx-BC3]

Top View



A B C D E F G H

Bottom View



H G F E D C B A

	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	WORD, /BYTE	O15, A–1	GND
5	A9	A8	A10	A11	O7	O14	O13	O6
4	NC	NC	NC	A19	O5	O12	V_{CC}	O4
3	NC	NC	A18	NC	O2	O10	O11	O3
2	A7	A17	A6	A5	O0	O8	O9	O1
1	A3	A4	A2	A1	A0	/CE	/OE or OE	GND

	H	G	F	E	D	C	B	A
6	GND	O15, A–1	WORD, /BYTE	A16	A15	A14	A12	A13
5	O6	O13	O14	O7	A11	A10	A8	A9
4	O4	V_{CC}	O12	O5	A19	NC	NC	NC
3	O3	O11	O10	O2	NC	A18	NC	NC
2	O1	O9	O8	O0	A5	A6	A17	A7
1	GND	/OE or OE	/CE	A0	A1	A2	A4	A3

A0 to A19 : Address inputs
O0 to O7, O8 to O14 : Data outputs
O15, A–1 : Data output 15 (WORD mode),
LSB Address input (BYTE mode)
WORD, /BYTE : Mode select
/CE : Chip Enable
/OE or OE : Output Enable
V_{CC} : Supply voltage
GND : Ground
NC [Note] : No Connection
DC : Don't Care

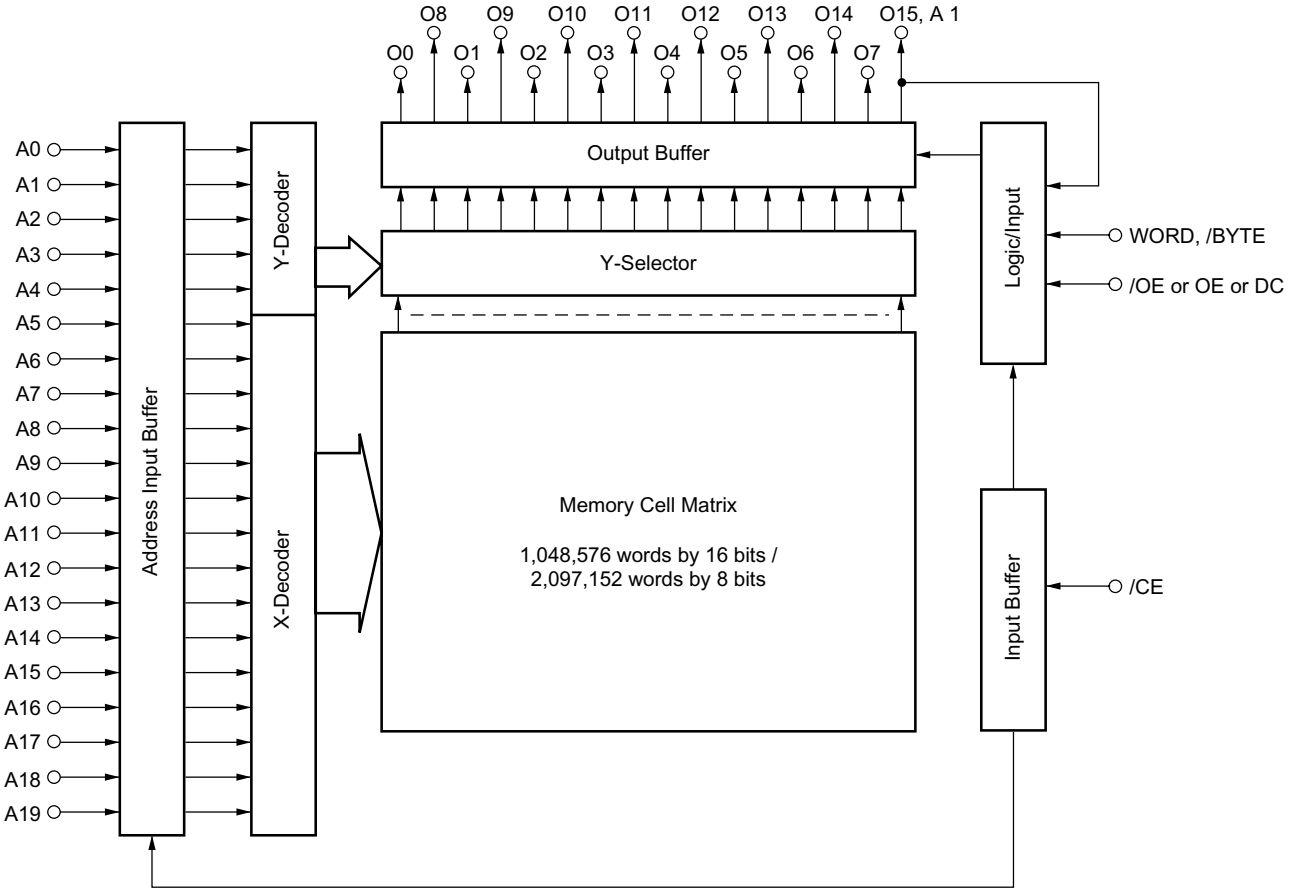
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the index mark.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. **High level** : WORD mode (1M-word by 16-bit) **Low level** : BYTE mode (2M-word by 8-bit)
A0 to A19 (Address inputs)	Input	Address input pins. A0 to A19 are used differently in the WORD mode and the BYTE mode. **WORD mode (1M-word by 16-bit)** A0 to A19 are used as 20 bits address signals. **BYTE mode (2M-word by 8-bit)** A0 to A19 are used as the upper 20 bits of total 21 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (1M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (2M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15, LSB Address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (1M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (2M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High-Z **Low level** : Data out
/OE or OE or DC (Output Enable, Don't care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected. (The signal can be connected.)

Block Diagram



Mask Option

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	V_{CC} = 3.0 V ± 0.3 V	–0.3		+0.5	V
		V_{CC} = 3.3 V ± 0.3 V	–0.3		+0.8	
High level output voltage	V_{OH}	I_{OH} = –100 μA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode), I_O = 0 mA			30	mA
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)			30	μA

AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

	Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	Address access time	t_{ACC}				90			85	ns
★	Address skew time	t_{SKEW}	**Note**			10			10	ns
	Chip enable access time	t_{CE}				90			85	ns
	Output enable access time	t_{OE}				25			25	ns
	Output hold time	t_{OH}		0			0			ns
	Output disable time	t_{DF}		0		25	0		25	ns
	WORD, /BYTE access time	t_{WB}				90			85	ns

★ **Note** t_{SKEW} indicates the following three types of time depending on the condition.

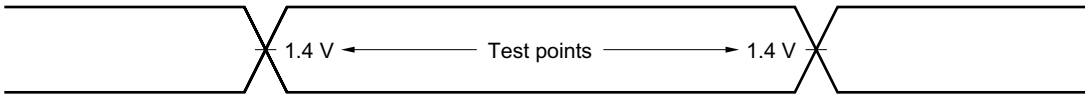
1) When switching /CE from high level to low level, t_{SKEW} is the time from the /CE low level input point until the next address is determined.
2) When switching /CE from low level to high level, t_{SKEW} is the time from the address change start point to the /CE high level input point.
3) When /CE is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CE is active, t_{SKEW} is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

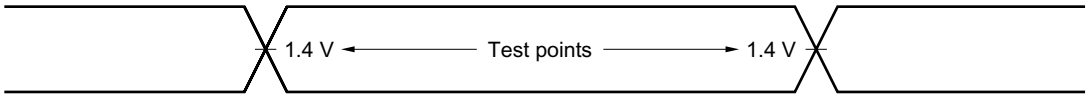
Remark t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

AC Test Conditions

Input waveform (Rise / Fall time ≤ 5 ns)



Output waveform



Output load

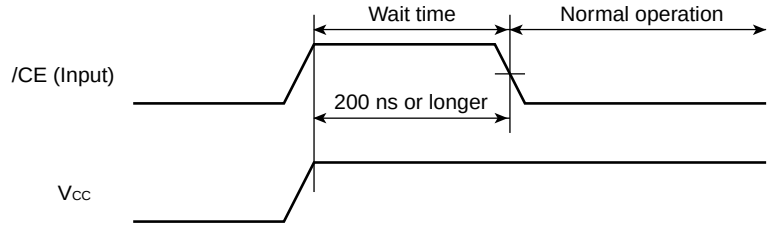
1TTL + 100 pF

★ **Cautions on power application**

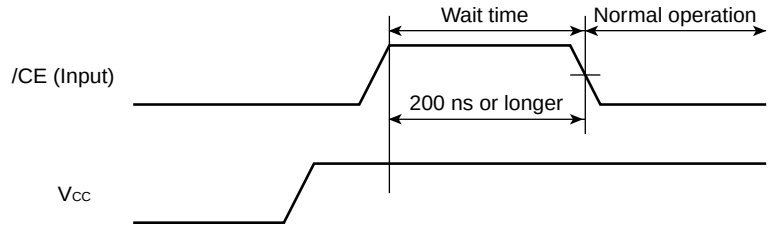
To ensure normal operation, always apply power using /CE following the procedure shown below.

1) Input a high level to /CE during and after power application.
2) Hold the high level input to /CE for 200 ns or longer (wait time).
3) Start normal operation after the wait time has elapsed.

Power Application Timing Chart 1 (When /CE is made high at power application)

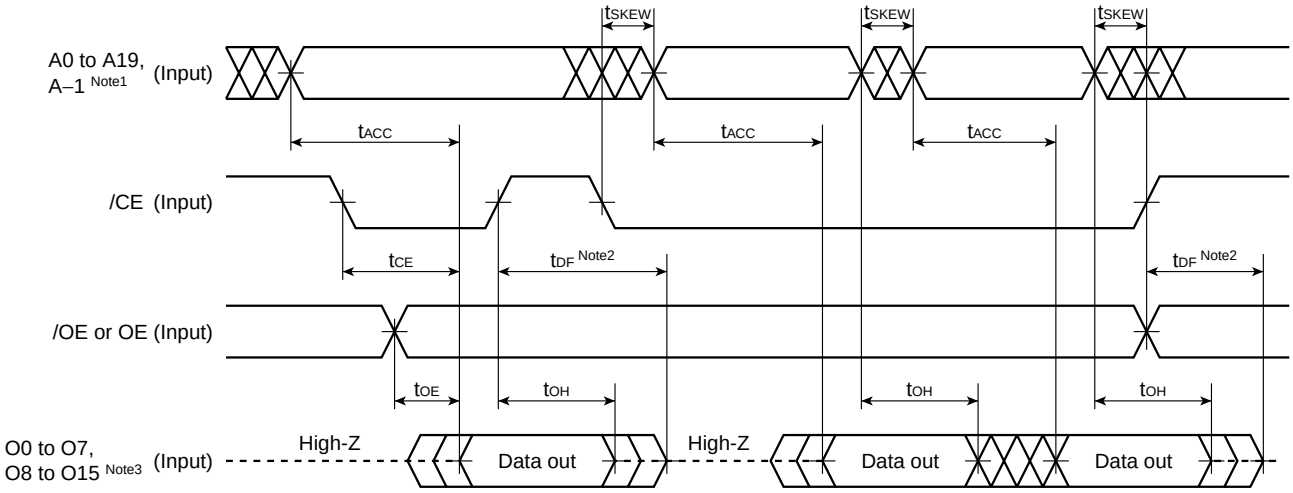


Power Application Timing Chart 2 (When /CE is made high after power application)



Caution Other signals can be either high or low during the wait time.

★ **Read Cycle Timing Chart**

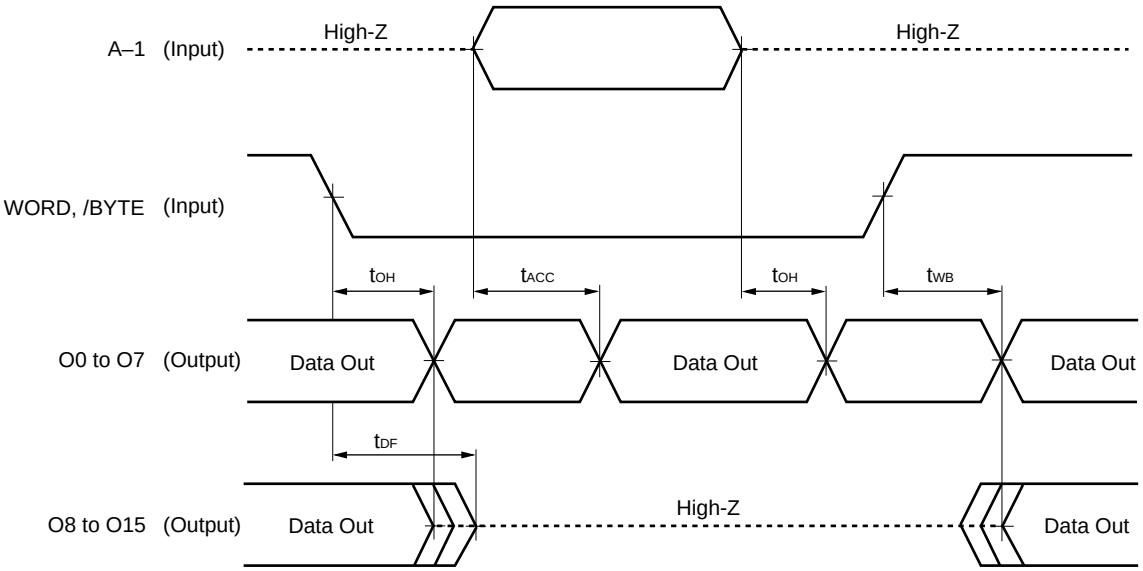


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

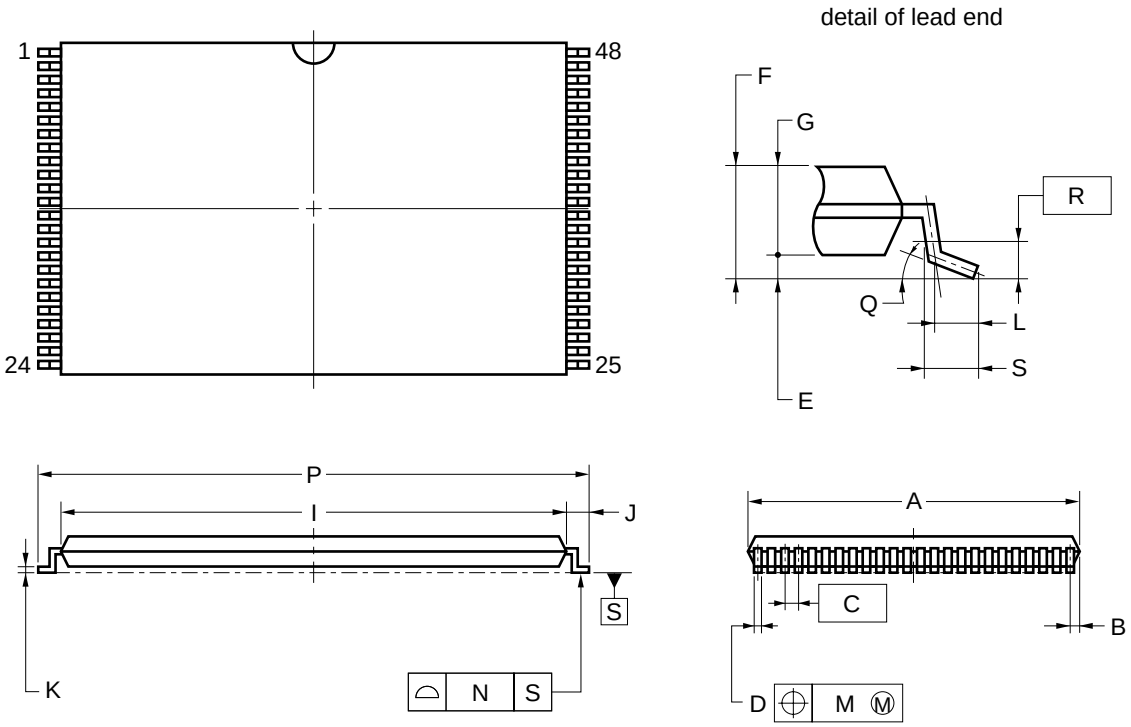
WORD, /BYTE Switch Timing Chart



Remark Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawings

48-PIN PLASTIC TSOP (I) (12x20)



NOTES

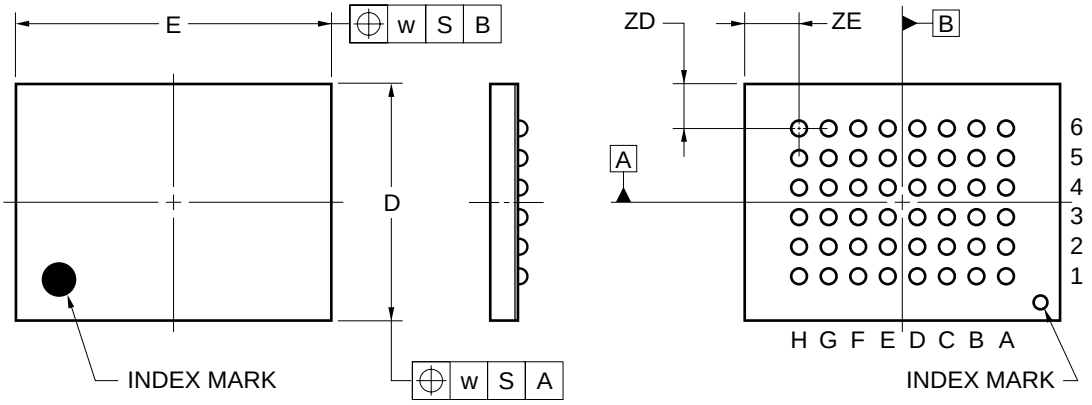
1) Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

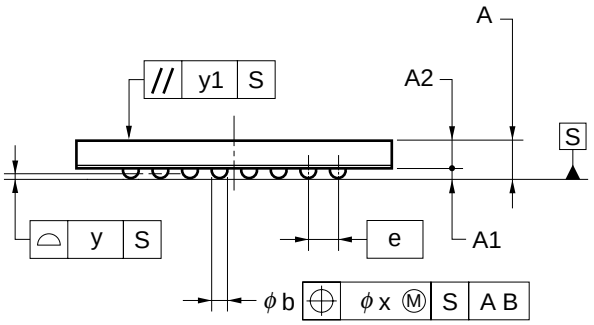
2) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GZ-50-MJH-1

★ 48-PIN TAPE FBGA(8x6)





ITEM	MILLIMETERS
D	6.0±0.1
E	8.0±0.1
w	0.2
e	0.80
A	0.97±0.10
A1	0.27±0.05
A2	0.70
b	0.45±0.05
x	0.08
y	0.1
y1	0.2
ZD	1.00
ZE	1.20

P48F9-80-BC3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C16300.

Types of Surface Mount Device

μPD23C16300GZ-MJH : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

μPD23C16300F9-BC3 : 48-pin TAPE FBGA (8 x 6)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
2nd edition/ Feb. 2003	Throughout	Throughout	Modification		Preliminary Data Sheet → Data Sheet
	p.8	p.8	Addition	AC Characteristics	Address skew time (t_{SKEW}) Note
	p.9	–	Addition		Cautions on power application
	p.10	p.9	Modification		Read Cycle Timing Chart
	p.12	p.11	Modification	Package Drawings	Preliminary version → Standard version

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF THE APPLIED WAVEFORM OF INPUT PINS AND THE UNUSED INPUT PINS FOR CMOS

Note:

Input levels of CMOS devices must be fixed. CMOS devices behave differently than Bipolar or NMOS devices. If the input of a CMOS device stays in an area that is between V_{IL} (MAX.) and V_{IH} (MIN.) due to the effects of noise or some other irregularity, malfunction may result. Therefore, not only the input waveform is fixed, but also the waveform changes, it is important to use the CMOS device under AC test conditions. For unused input pins in particular, CMOS devices should not be operated in a state where nothing is connected, so input levels of CMOS devices must be fixed to high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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