

# OKI Semiconductor

## MSM5116100A

16,777,216-Word × 1-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

### DESCRIPTION

The MSM5116100A is a new generation dynamic organized as 16,777,216 word × 1-bit. The technology used to fabricate the MSM5116100A is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

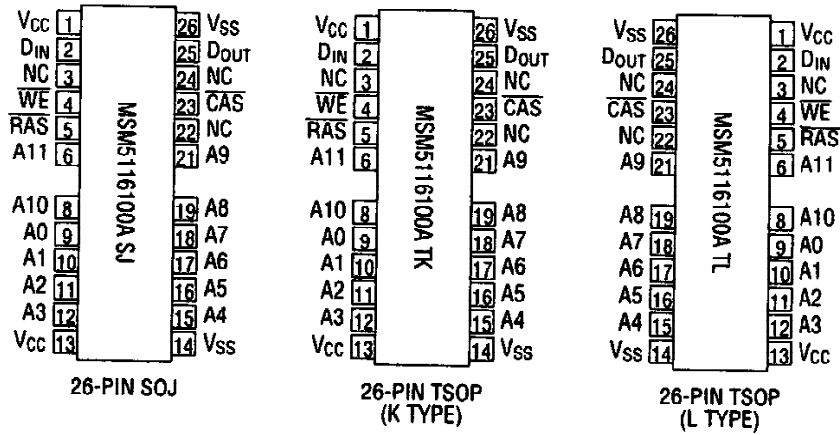
### FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 16,777,216 word × 1 bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 4096 cycles/64ms
- Common I/O capability using "Early-Write" operation
- Fast Page Mode, Read Modify Write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, Hidden refresh,  $\overline{\text{RAS}}$  only refresh capability
- Multi bit test mode capability
- Package:
  - 26-Pin 300mil Plastic SOJ (SOJ26/24-P-300)
  - 26-Pin 300mil Plastic TSOP (TSOP26/24-P-300-K) (TSOP26/24-P-300-L)

### PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>		Operating (Max.)	Standby (Max.)
MSM5116100A-60	60ns	30ns	15ns	110ns	495mW	5.5mW
MSM5116100A-70	70ns	35ns	20ns	130ns	440mW	
MSM5116100A-80	80ns	40ns	20ns	150ns	385mW	

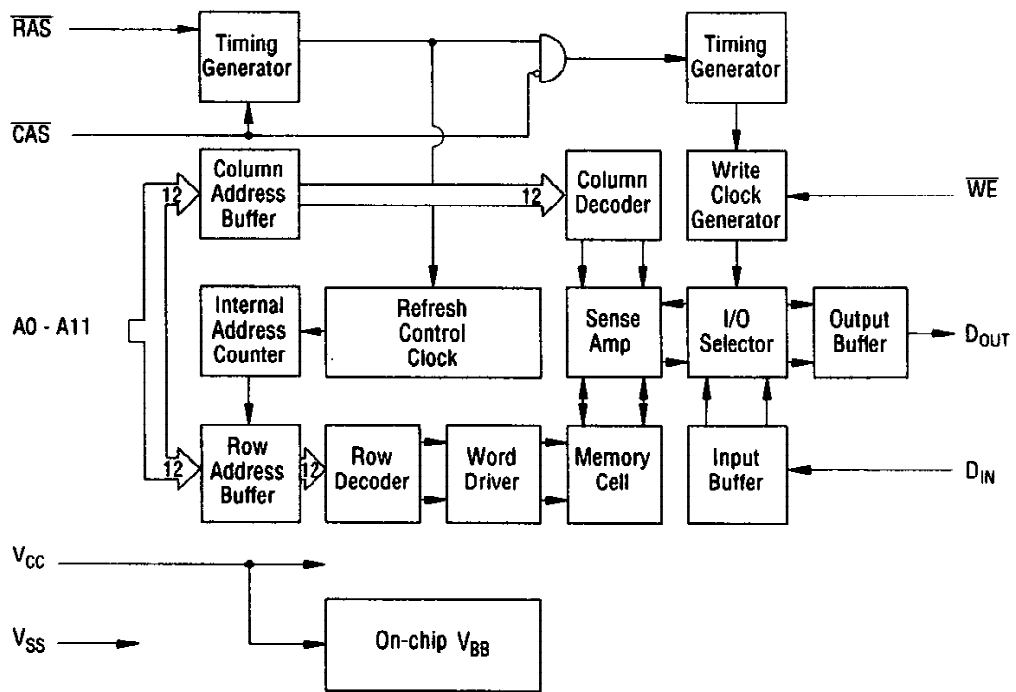
**PIN CONFIGURATION (TOP VIEW)**



Pin Names	Function
A0 - A11	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output
WE	Write Enable
V <sub>CC</sub>	Power Supply (5V)
V <sub>SS</sub>	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V<sub>CC</sub> pin, and same GND voltage level must be provided to every V<sub>SS</sub> pin.

**FUNCTIONAL BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-1.0 to 7.0	V
Short Circuit Output Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub> *	1	W
Operating Temperature	T <sub>opr</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

\*: T<sub>a</sub> = 25°C**Recommended Operating Conditions**(T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V
Input Low Voltage	V <sub>IL</sub>	-1.0	—	0.8	V

**Capacitance**(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A11, D <sub>IN</sub> )	C <sub>IN1</sub>	—	6	pF
Input Capacitance (R <sub>AS</sub> , C <sub>AS</sub> , W <sub>E</sub> )	C <sub>IN2</sub>	—	7	pF
Output Capacitance (D <sub>OUT</sub> )	C <sub>OUT</sub>	—	7	pF

DC Characteristics

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0$  to  $70^\circ C$ )

Parameter	Symbol	Condition	MSM 5116100A-60		MSM 5116100A-70		MSM 5116100A-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	$V_{OH}$	$I_{OH} = -5.0mA$	2.4	$V_{CC}$	2.4		
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_i \leq 6.5V$ ; All other pins not under test = $0V$	-10	10	-10	10	-10	10	$\mu A$	
Output Leakage Current	$I_{LO}$	$D_{OUT} = \text{Disable}$ $0V \leq V_o \leq 5.5V$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{RAS}, \overline{CAS}$ cycling $t_{RC} = \text{Min.}$	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS}, \overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2V$	—	1	—	1	—	1		
Average Power Supply Current (RAS Only Refresh)	$I_{CC3}$	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$ $t_{RC} = \text{Min.}$	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	—	5	—	5	—	5	mA	1
Average Power Supply Current (CAS Before RAS Refresh)	$I_{CC6}$	$\overline{RAS}$ cycling $\overline{CAS}$ before $\overline{RAS}$	—	90	—	80	—	70	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ $\overline{CAS}$ cycling $t_{PC} = \text{Min.}$	—	80	—	70	—	60	mA	1, 3

- Notes:
1. Specified values are obtained with the output open.
  2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .
  3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C) Note 1, 2, 3, 10, 11

Parameter	Symbol	MSM 5116100A-60		MSM 5116100A-70		MSM 5116100A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t <sub>RC</sub>	110	—	130	—		
Read Modify Write Cycle Time	t <sub>RMW</sub>	130	—	155	—	175	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRMW</sub>	85	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	35	—	40	—	45	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	15	0	20	0	20	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	64	—	64	—	64	ms	
RAS Precharge Time	t <sub>RP</sub>	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t <sub>CP</sub>	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	10	—	10	—	10	—	ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t <sub>RC<math>\overline{\text{D}}</math></sub>	20	45	20	50	20	60	ns	5
RAS to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	30	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	35	—	40	—	45	—	ns	

AC Characteristics (2/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C) Note 1, 2, 3, 10, 11

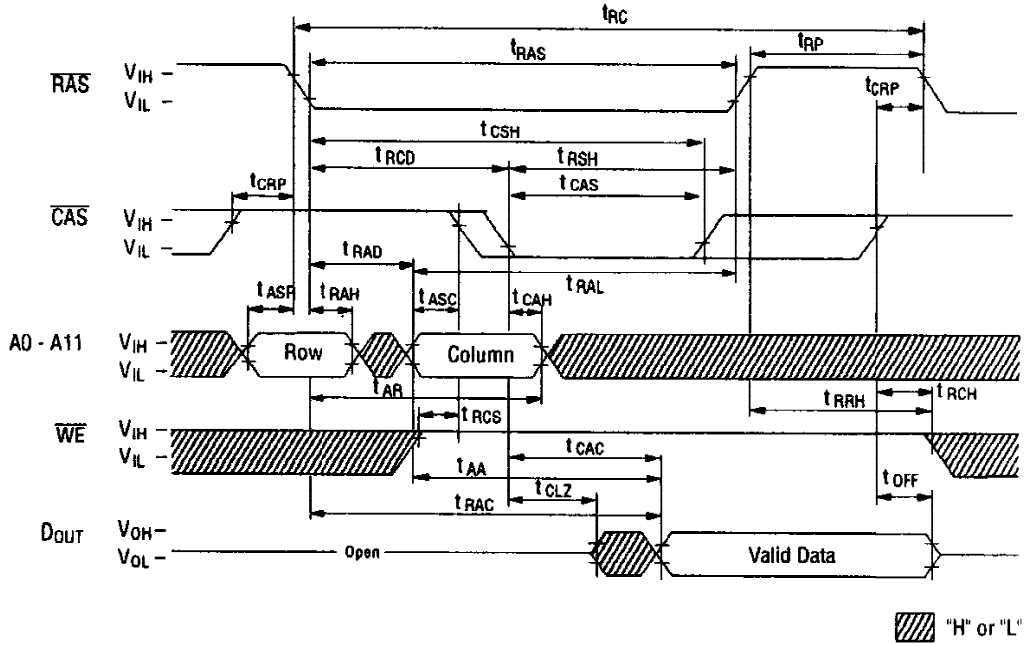
Parameter	Symbol	MSM 5116100A-60		MSM 5116100A-70		MSM 5116100A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	8
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	9
Write Command Hold Time	t <sub>WCH</sub>	10	—	15	—	15	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	10	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t <sub>WCR</sub>	45	—	55	—	60	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	15	—	20	—	20	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	12
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	15	—	ns	12
Data-in Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	50	—	55	—	60	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	15	—	20	—	20	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	30	—	35	—	40	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	60	—	70	—	80	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	35	—	40	—	45	—	ns	9
$\overline{\text{CAS}}$ Active Delay from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t <sub>CPT</sub>	40	—	40	—	40	—	ns	
$\overline{\text{We}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>WRP</sub>	10	—	10	—	10	—	ns	
$\overline{\text{We}}$ Hold Time from ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>WRH</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t <sub>WSR</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t <sub>WHR</sub>	20	—	20	—	20	—	ns	

- Notes:
1. An initial pause of 200 $\mu$ s is required after power-up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$  only refresh cycle or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle) before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  initialization cycles is required.
  2. The AC characteristics assume  $t_{\tau} = 5\text{ns}$ .
  3.  $V_{IH}(\text{Min.})$  and  $V_{IL}(\text{Max.})$  are reference levels of input signals for timing measurement. Transition times ( $t_{\tau}$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
  5. Operation within the  $t_{\text{RCD}}(\text{Max.})$  limit insures that  $t_{\text{RAC}}(\text{Max.})$  can be met.  $t_{\text{RCD}}(\text{Max.})$  is specified as a reference point only; If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{Max.})$  limit, then access time is controlled by  $t_{\text{CAC}}$ .
  6. Operation within the  $t_{\text{RAD}}(\text{Max.})$  limit insures that  $t_{\text{RAC}}(\text{Max.})$  can be met.  $t_{\text{RAD}}(\text{Max.})$  is specified as a reference point only; If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{Max.})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
  7.  $t_{\text{OFF}}(\text{Max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
  9.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPWD}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{Min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{Min.})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{Min.})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{Min.})$ , and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{Min.})$ , the cycle is a read modify write cycle and data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  10. The test mode is initiated by performing a  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. The test mode specified in this data sheet is 16-bit parallel test function. CA0, CA1, CA10 and CA11 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, the data output pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a  $\overline{\text{RAS}}$  only refresh cycle or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.
  11. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to specified value in this data sheet.
  12. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle or to  $\overline{\text{WE}}$  leading edge in a read modify write cycle.

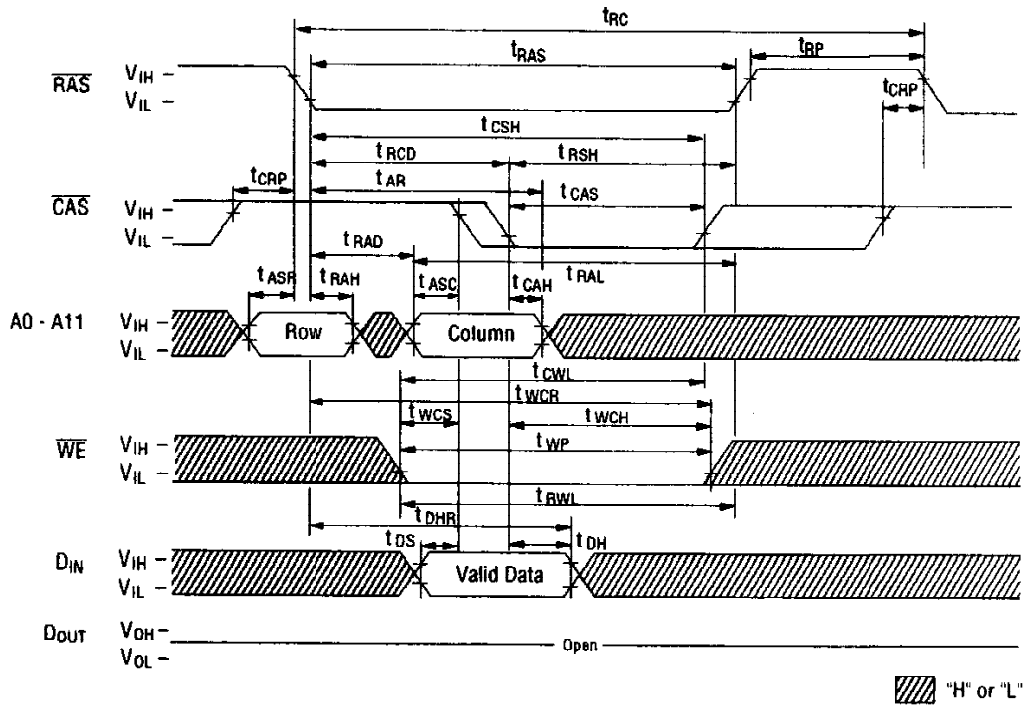


### TIMING WAVEFORM

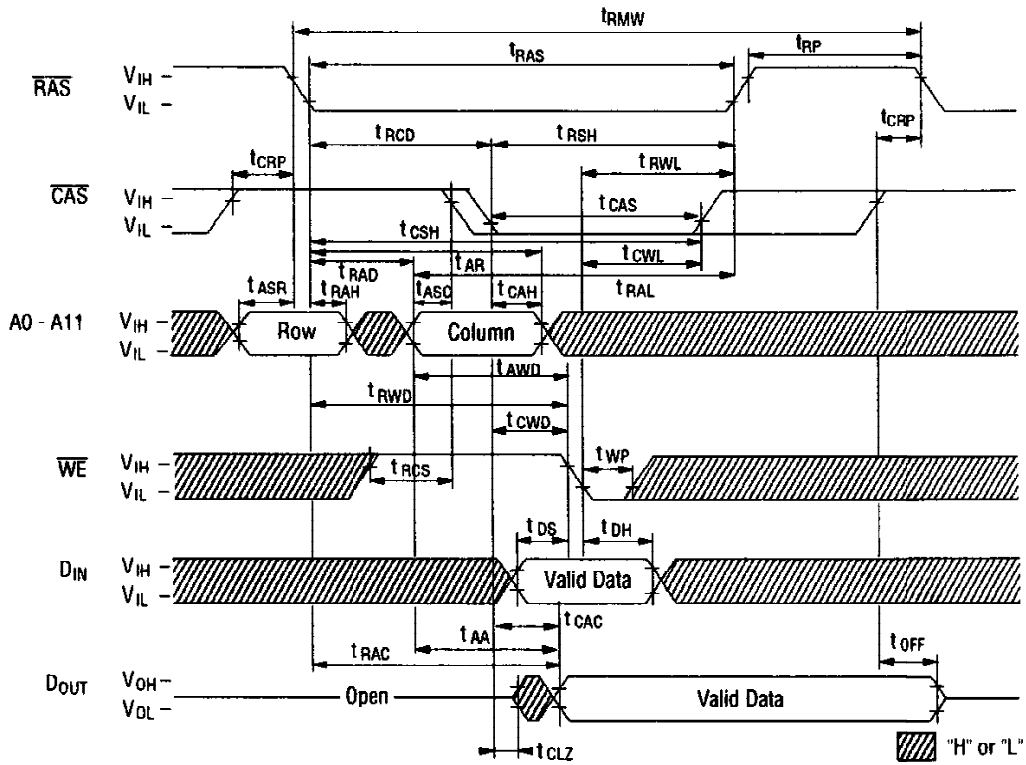
#### Read Cycle



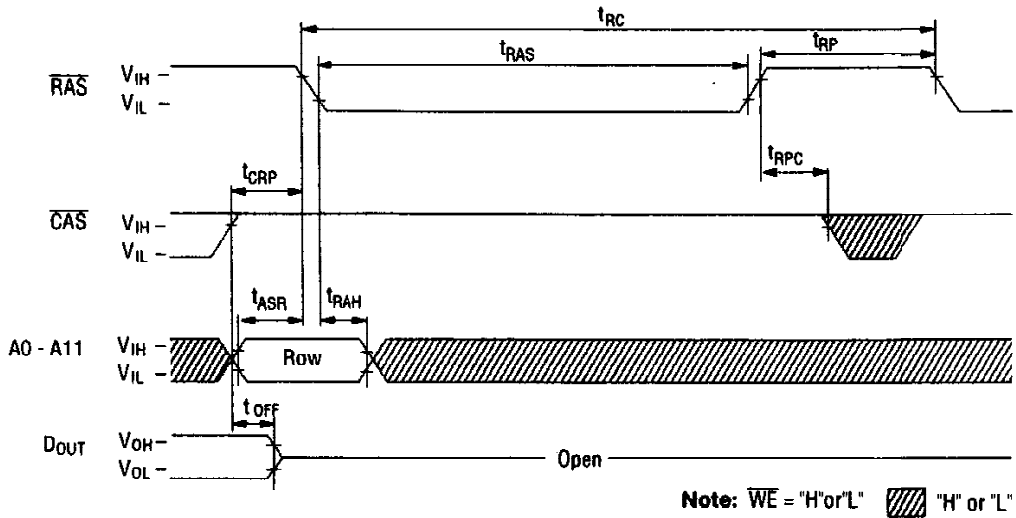
#### Write Cycle (Early Write)



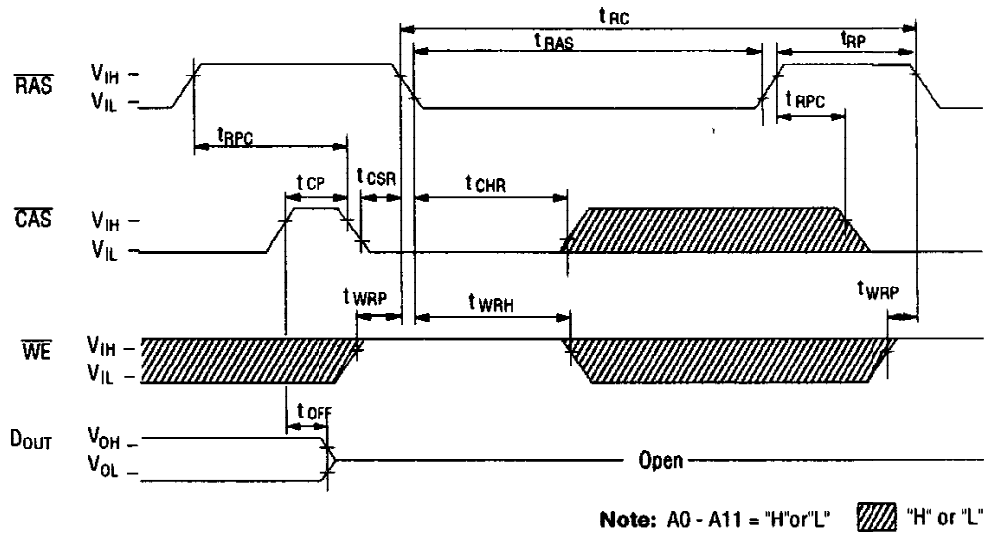
**Read Modify Write Cycle**



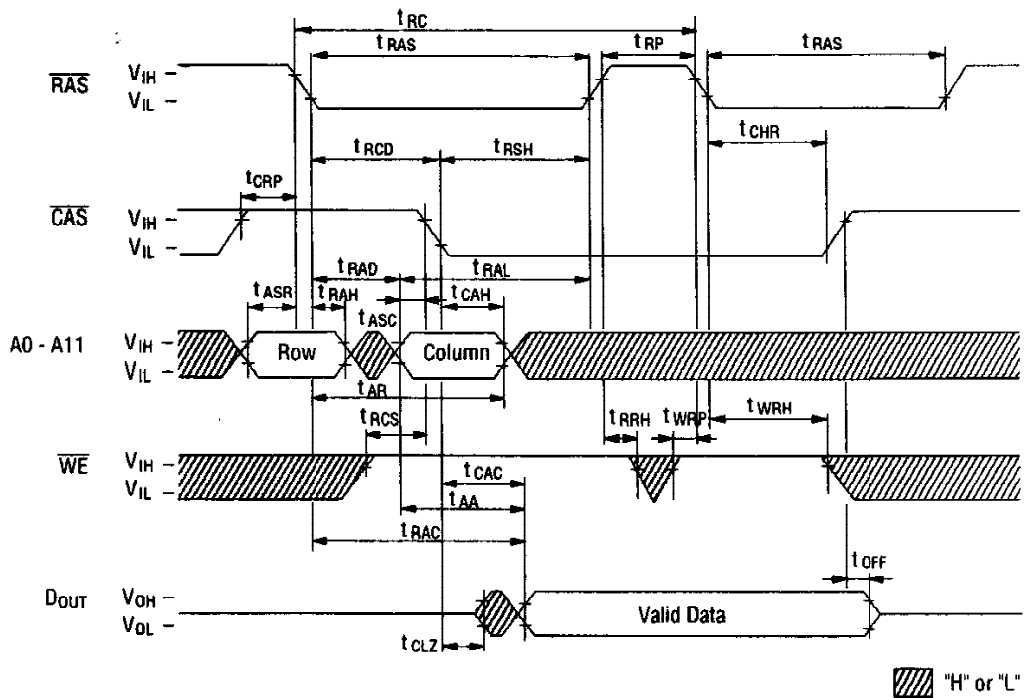
**RAS Only Refresh Cycle**



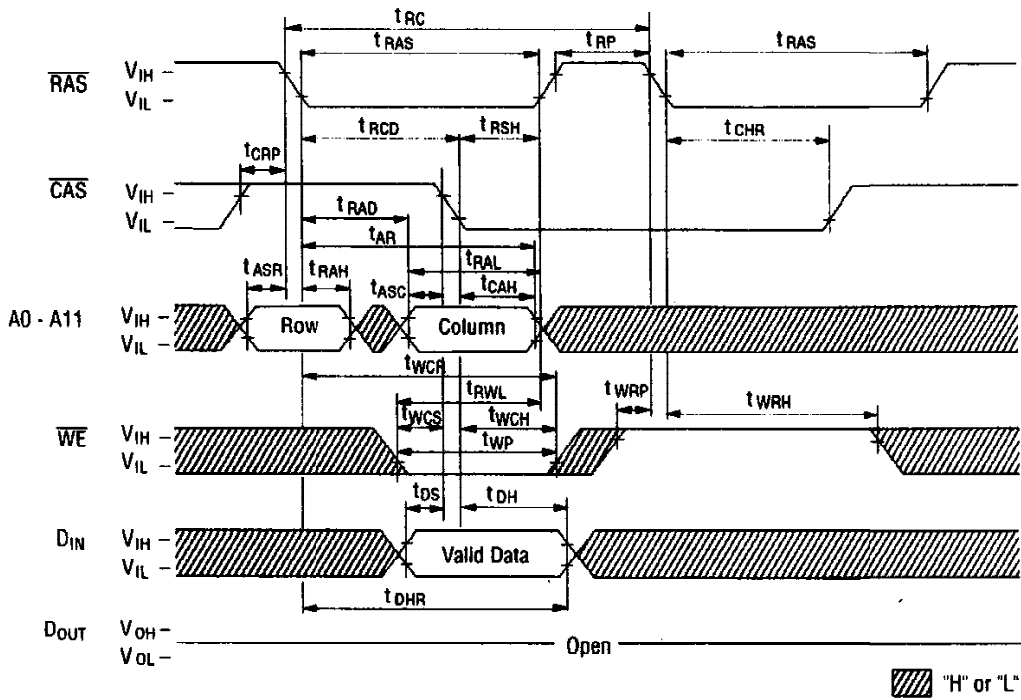
**CAS Before RAS Refresh Cycle**



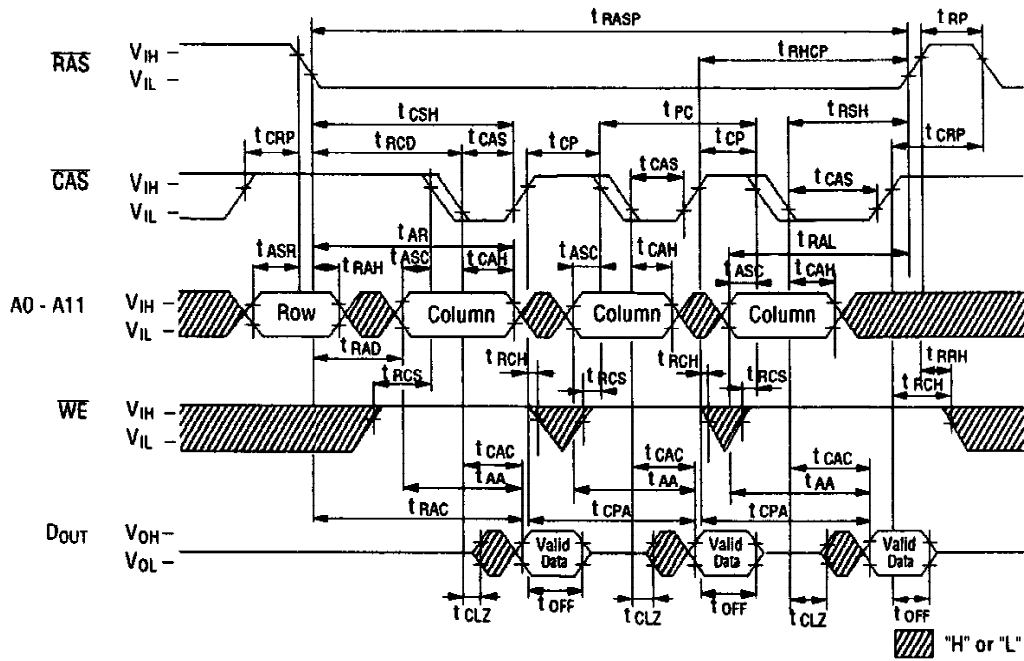
**Hidden Refresh Read Cycle**



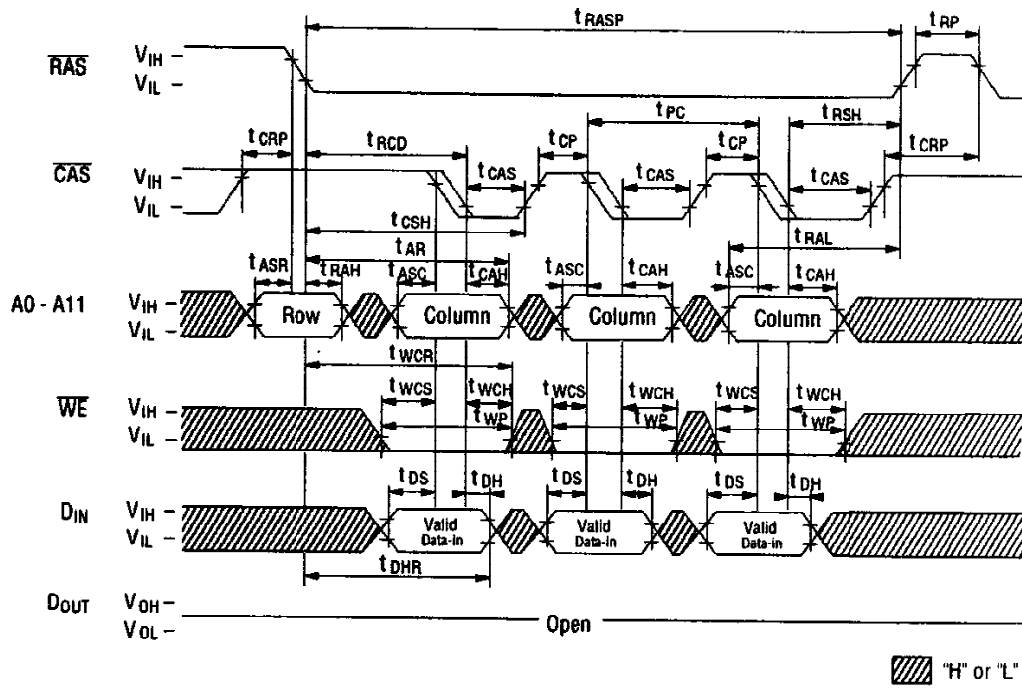
Hidden Refresh Write Cycle



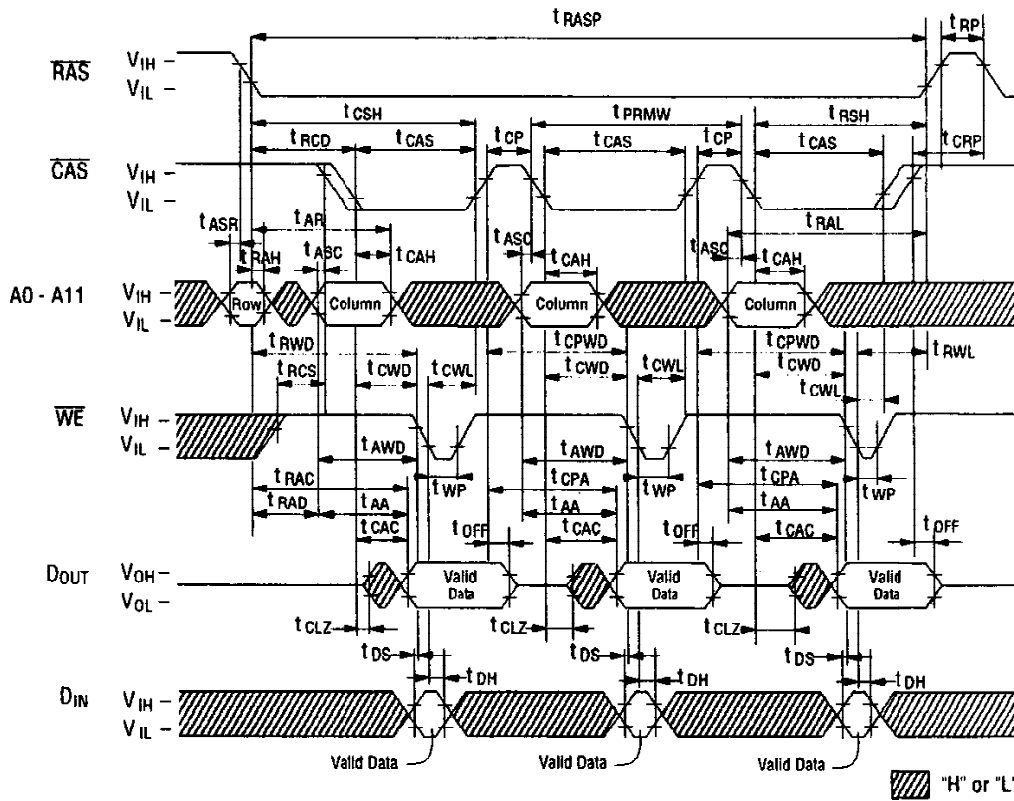
Fast Page Mode Read Cycle



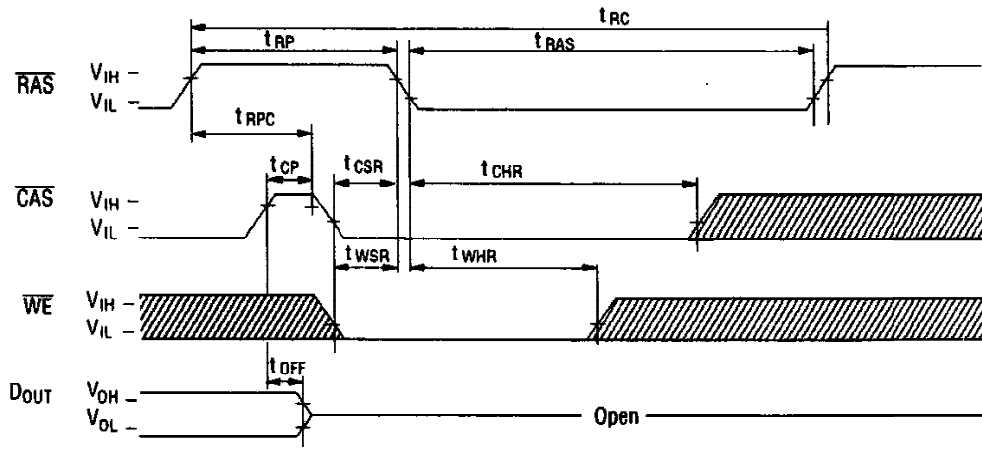
Fast Page Mode Write Cycle



Fast Page Mode Read Modify Write Cycle



Test Mode In Cycle



Note: A0 - A11, D<sub>IN</sub> = "H" or "L" "H" or "L"

CAS Before RAS Refresh Counter Test Cycle

