Preliminary

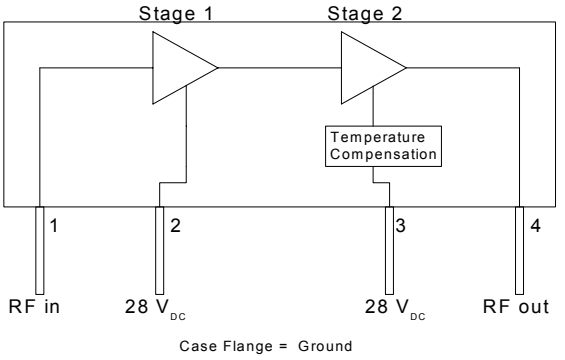
XD010-42S-D4F

869-894 MHz Class A
10W Power Amplifier Module

Product Description

The **XD010-42S-D4F** 10W power module is a 2-stage Class A amplifier module for use in the driver stages of linear RF power amplifiers of cellular base stations. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. This unit operates from a single voltage and has internal temperature compensation of the bias voltage to ensure stable performance over the full temperature range.

Functional Block Diagram



Product Features

- **50 Ω RF impedance**
- **8W Output P_{1dB} Typical**
- **Single Voltage Operation**
- **High Gain: 30 dB Typical**
- **Advanced, XeMOS II LDMOS FETS**
- **Temperature Compensation**

Applications

- **Base Station PA driver**
- **Repeater**
- **CDMA**
- **GSM / EDGE**

Key Specifications

Parameter	Description: Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DD1} = 230mA$, $I_{DD2} = 700mA$, $T_{Flange} = 25°C$	Unit	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	869		894
P_{1dB}	Output Power at 1dB Compression, 880 MHz	W		8	
Gain	Gain at 1W Output Power	dB		30	
Gain Flatness	Over Frequency at 1W Output (CW)	dB		0.4	
IRL	Input Return Loss at 1W Output (CW) (50Ω Ref)	dB		20	
Efficiency	Drain Efficiency at 8W CW Output	%		24	
	Drain Efficiency at 1W CDMA (Single Carrier IS-95)	%		3.5	
Linearity	ACPR at 1W CDMA Output (Single Carrier IS-95)	dB		-50	
	ALT-1 PR at 1W CDMA (Single Carrier IS-95)	dB		-75	
	3rd Order IMD at 8W PEP (Two Tone 1MHz Spacing)	dBc		-30	
	3rd Order IMD at 1W PEP (Two Tone 1MHz Spacing)	dBc		-50	
Delay	Signal Delay from Pin 1 to Pin 4	nS		3.9	
Phase Linearity	Deviation from Linear Phase (Peak to Peak)	Deg		0.5	
$R_{TH, j-l}$	Thermal Resistance Stage 1 (Junction to Case)	°C/W		11	
$R_{TH, j-2}$	Thermal Resistance Stage 2 (Junction to Case)	°C/W		4	

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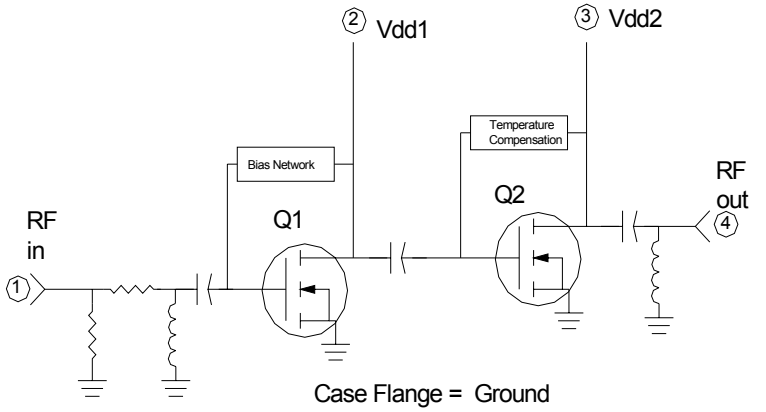
Pin Out Description

Pin #	Function	Description
1	RF Input	Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
2	V_{DD1}	This is the bias feed for the 1st stage of the amplifier module.
3	V_{DD2}	This is the bias feed for the 2nd stage of the amplifier module. The gate bias is temperature compensated to maintain constant current over the operating temperature range. See Note 1.
4	RF Output	Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
Flange	Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

Simplified Device Schematic



Absolute Maximum Ratings

Parameters	Value	Unit
1st Stage Bias Voltage (V_{DD1})	35	V
2nd Stage Bias Voltage (V_{DD2})	35	V
RF Input Power	+20	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Base Plate Temperature: Operating with no RF present	90	°C
Output Device Channel Temperature	+200	°C
Lead Temperature During Solder Reflow	+210	°C
Operating Temperature Range	-20 to +90	°C
Storage Temperature Range	-40 to +100	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Note 1:

The internal generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module.

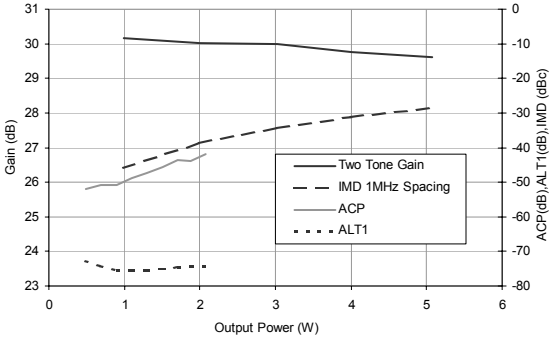
Note 2:

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

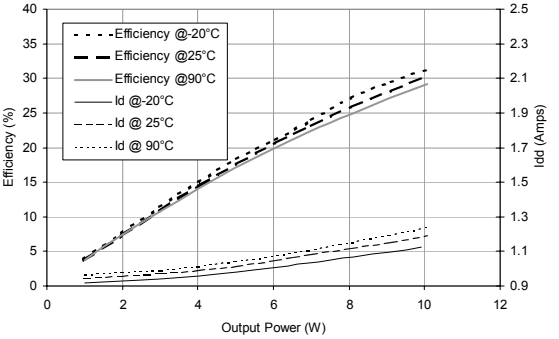
Caution: ESD Sensitive

Appropriate precaution in handling, packaging and testing devices must be observed.

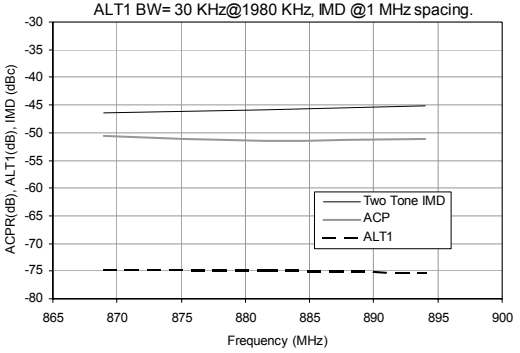
Gain, IMD, ACP, ALT1 vs. Output Power Freq=881 MHz,
Vdd=28V, T_{Flange}=25°C, IS-95 ADJ BW=30KHz @ 750 KHz
ALT1 BW=30KHz @1980 KHz, IMD @ 1 MHz spacing



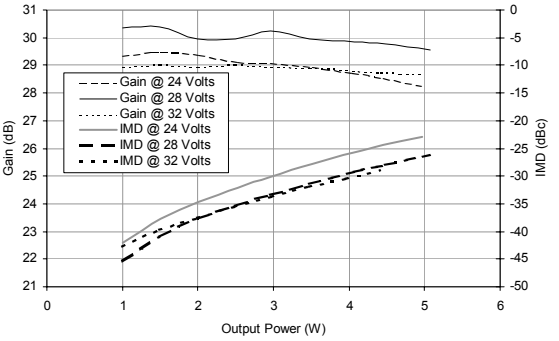
Efficiency and Idd vs. Output Power and Temperature
Freq=881 MHz, Vdd=28 V, T_{Flange}=-20°C, 25°C, 90°C



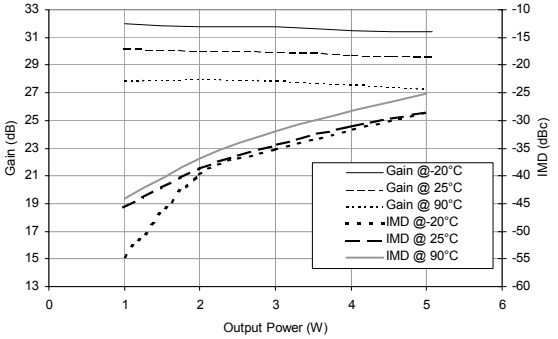
Two Tone IMD, ACP, ALT1 vs. Frequency
Output Power=1 Watt, Vdd=28 V, T_{Flange}=25°C
IS95 ADJ BW= 30 KHz@ 750 KHz
ALT1 BW= 30 KHz@1980 KHz, IMD @1 MHz spacing.



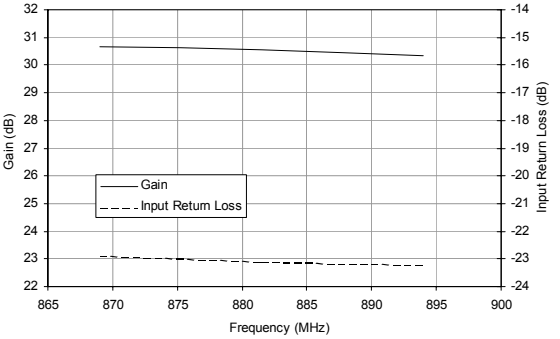
Gain and IMDs vs. Output Power and Voltage
Freq=881 and 882 MHz, Vdd=24 V, 28 V, 32 V
T_{Flange}=25°C



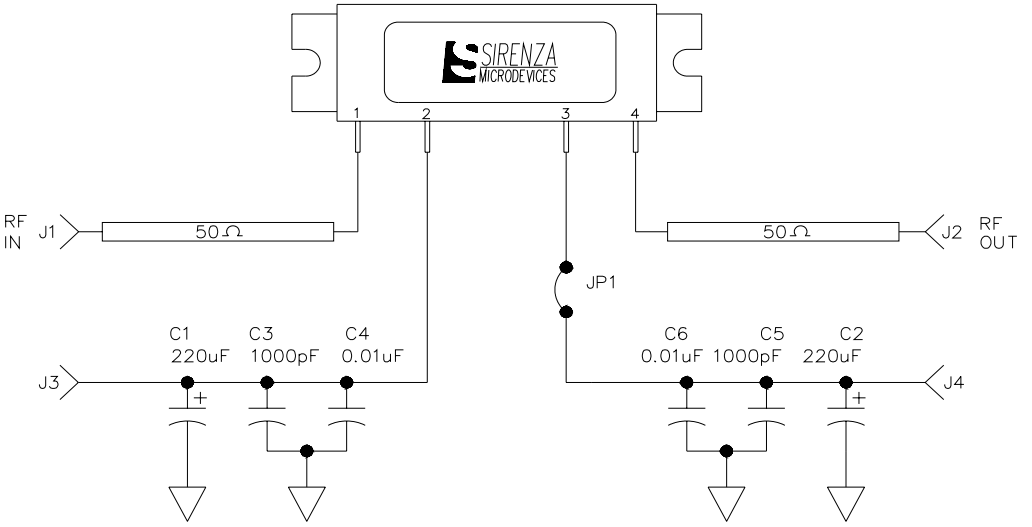
Gain and IMD vs. Output Power and Temperature
Freq=881 MHz, Vdd=28 V, T_{Flange}=-20°C, 25°C, 90°C



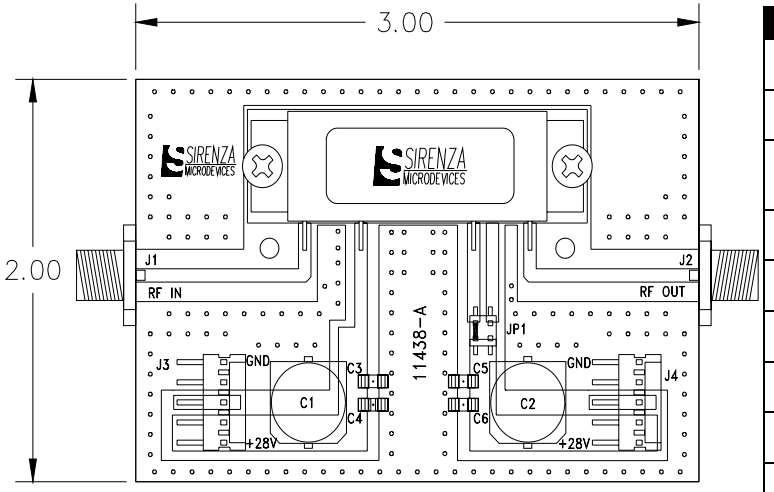
Gain and Input Return Loss vs. Frequency
Output Power=1 Watt, Vdd=28 V, T_{Flange}=25°C



Test Board Schematic with module attachments shown



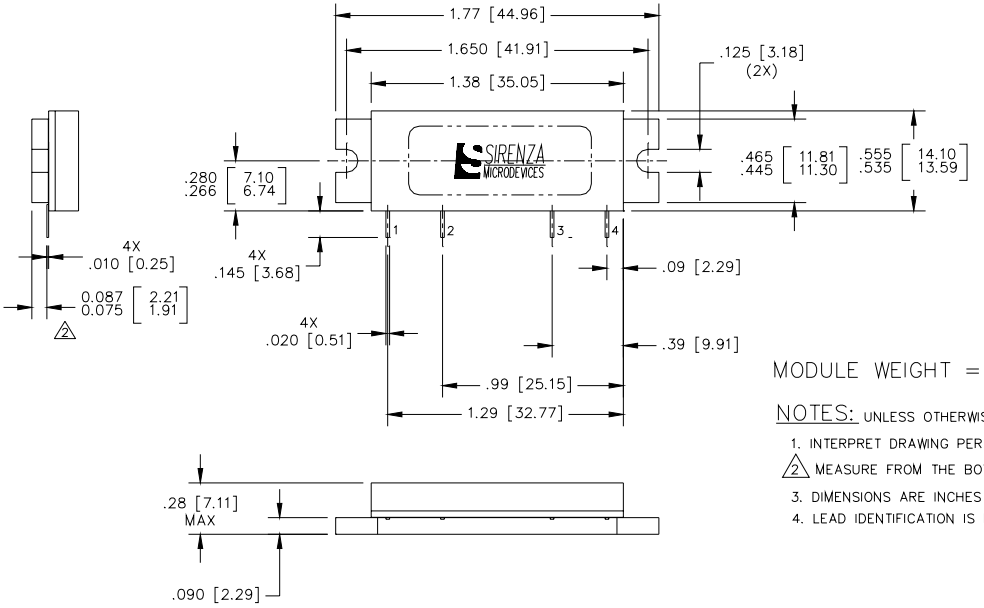
Test Board Layout and Bill of Materials



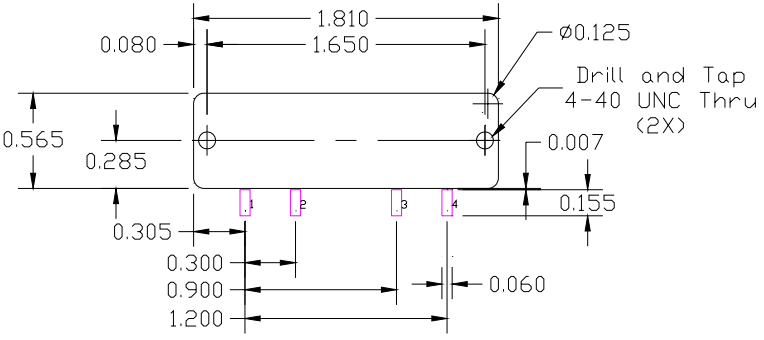
Component	Description	Manufacturer
PCB	Rogers4350, ε_r=3.5 Thickness=30mils	Rogers
J1, J2	SMA, RF, Panel Mount Tab W / Flange	AMP
J3, J4	MTA Post Header, 5 Pin, Rectangle, Polarized, Surface Mount	AMP
C1, C2	Cap, 220μF 50V, -40 to 85^{o}C, Electrolytic, G	Panasonic
C4, C6	Cap, 0.01μF, 100V, 10%, 1206	Johanson
C3, C5	Cap, 1000pF, 100V, 10%, 1206	Johanson
JP1 Header	SMT Header, Low Profile, 2mm	Specialty Electronics
JP1 Shunt	Shunt, Mate to Header, 2mm	Specialty Electronics
Mounting Screws	4-40 X 0.250"	Various

To download Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture click here

Package Outline Drawing



Recommended PCB Cutout and Landing Pads for the D4F Package



Note 3: Dimensions are in inches