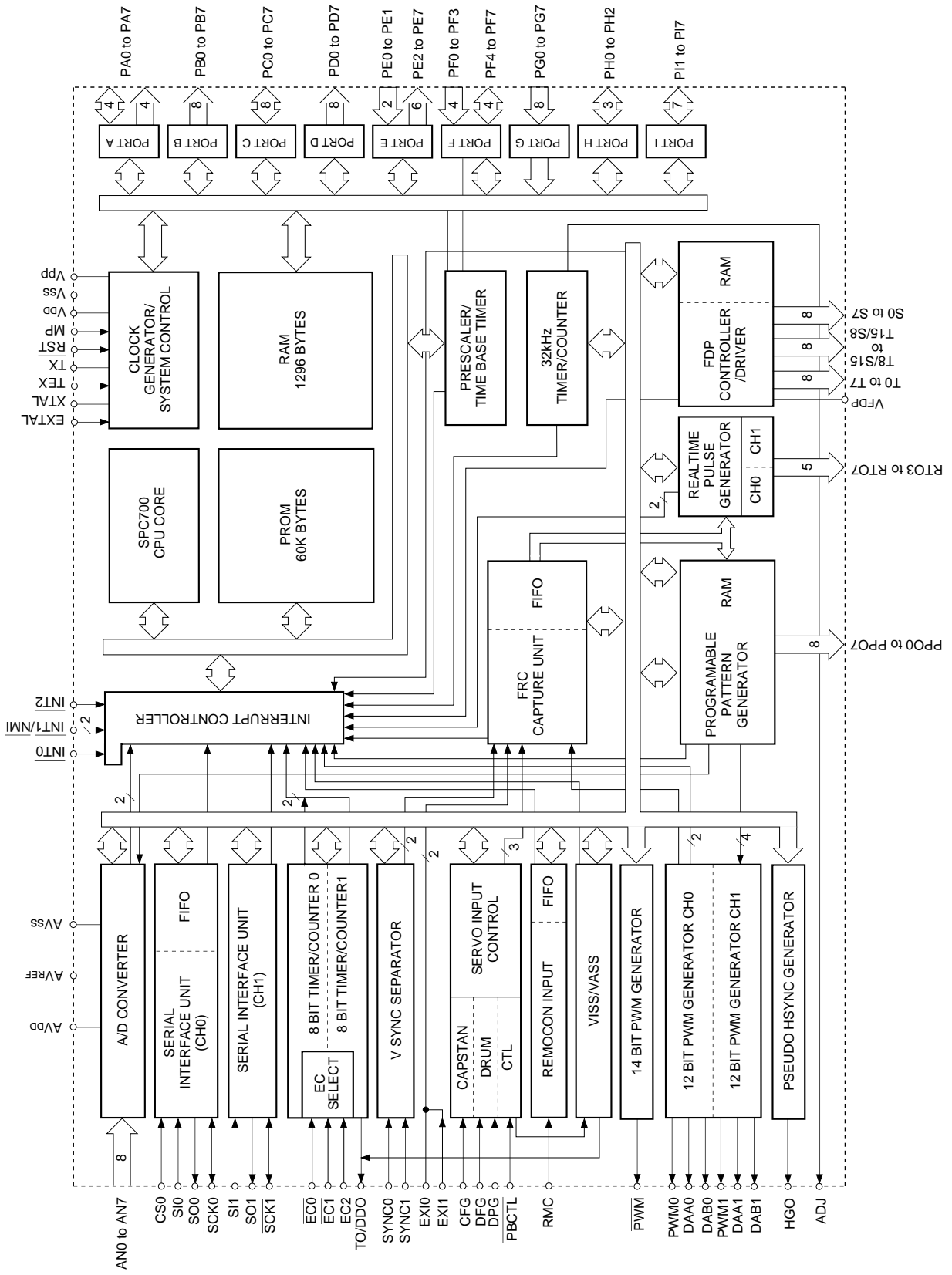
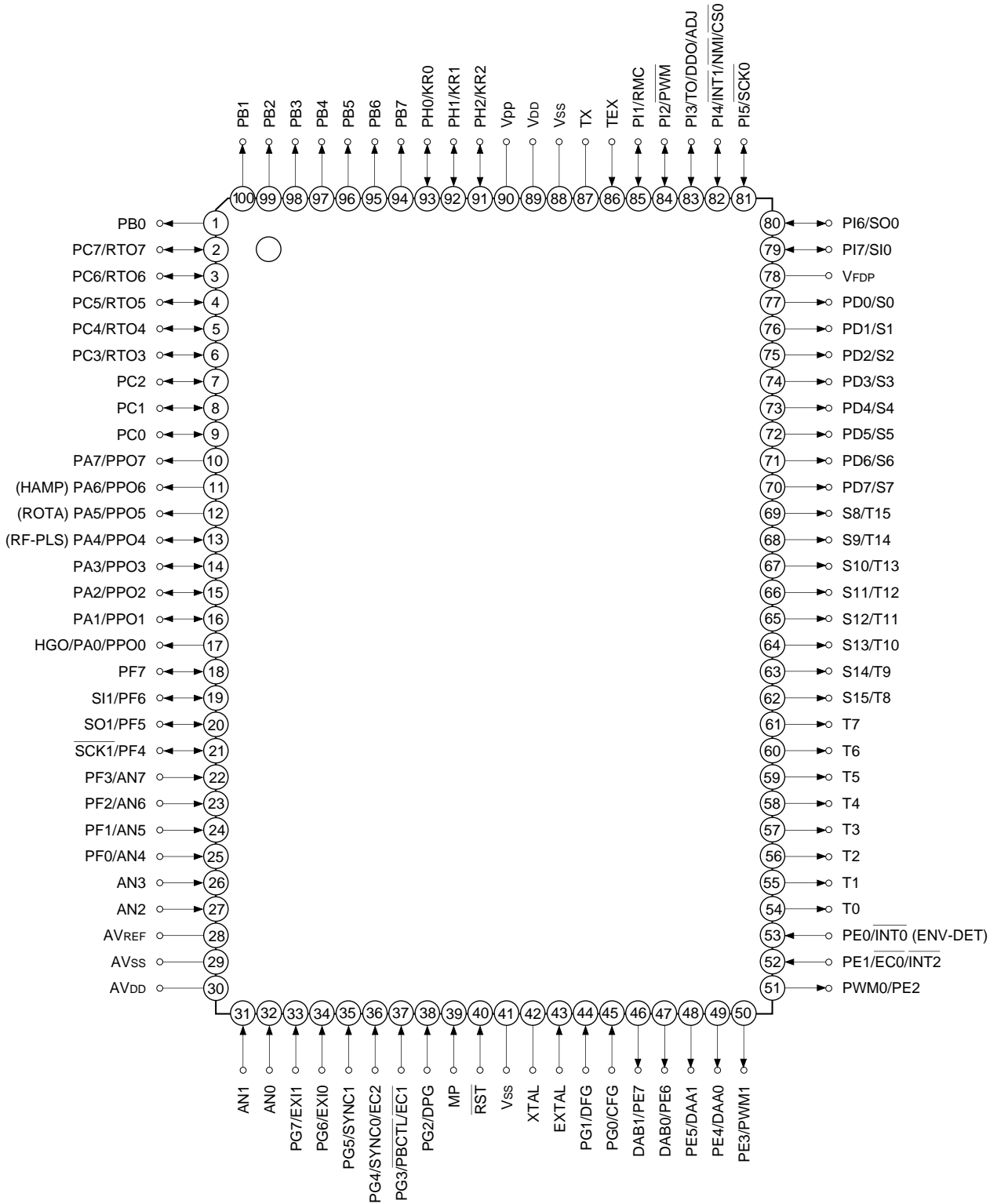


Block Diagram



Pin Configuration (Top View)



- Note)**
1. Vpp (Pin 90) is always connected to VDD.
 2. VSS (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) must be connected to GND.

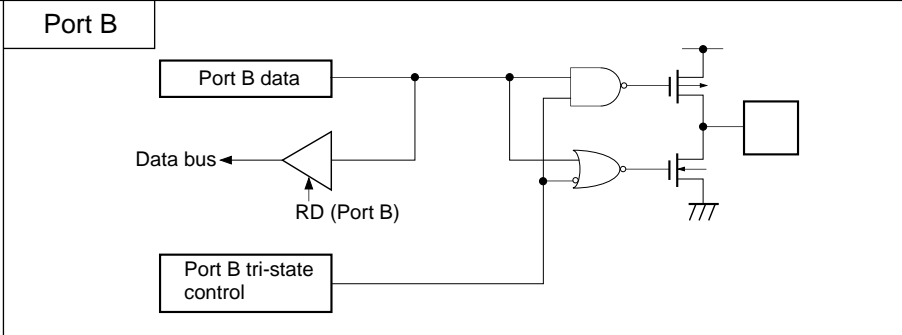
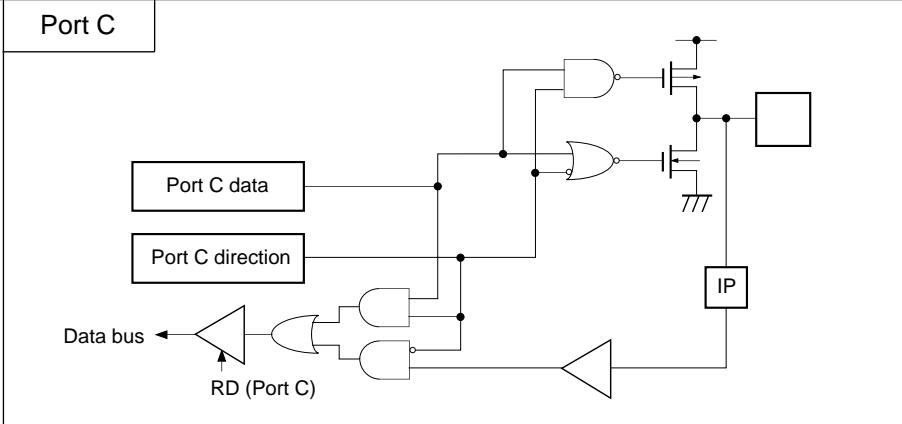
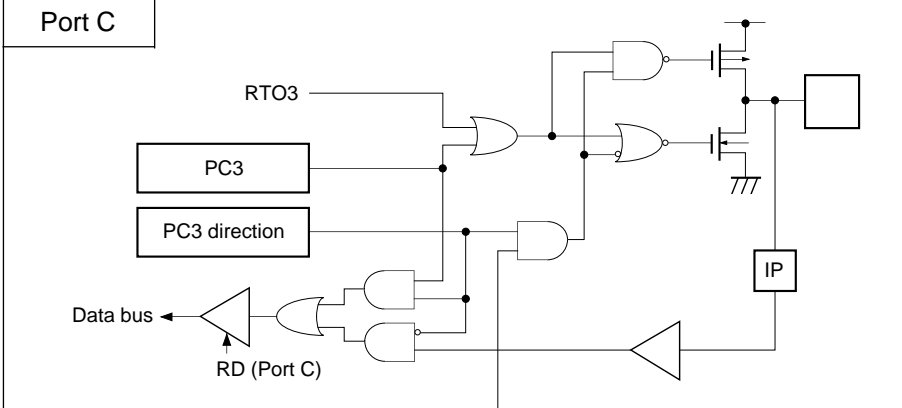
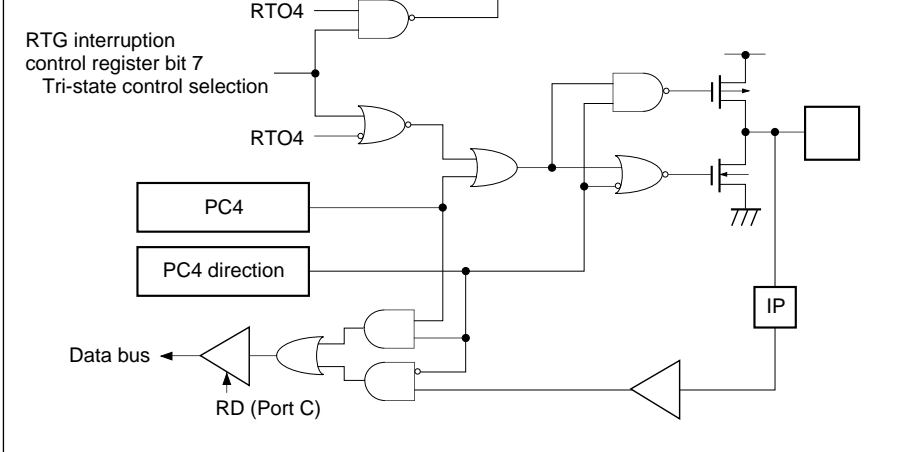
Pin Description

Symbol	I/O	Description			
PA0/PPO0/HGO	Output/Real time output/Output	(Port A) PA0 and PA5 to PA7 are for outputs; PA1 to PA4 are for I/O. I/O can be set in a unit of single bits. Data is gated with PPO content by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.		
PA1/PPO1	I/O/ Real time output		Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (8 pins)		
PA2/PPO2					
PA3/PPO3					
PA4/PPO4	Output/ Real time output			Head switching output pins. (2 pins)	
PA5/PPO5					
PA6/PPO6					
PA7/PPO7					
PB0 to PB7	Output	8-bit output port. Tri-state can be controlled. (8 pins)			
PC0 to PC2	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with RTO content by OR-gate and they are output. (8 pins)			
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)		
T0 to T7	Output	FDP timing signal output pin. (8 pins)			
T8/S15 to T15/S8	Output/Output	Output pins for FDP timing signal and segment signal. (8 pins)			
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal output pin. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are for inputs; upper 6 bits are for outputs. (8 pins)	Trigger pulse input pin for head switching output.	Input pin to request external interruption. Active when falling edge.	
PE1/ $\overline{\text{EC0}}$ / INT2	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.	
PE2/PWM0	Output/Output		PWM output pins. (2 pins)		
PE3/PWM1	Output/Output				
PE4/DAA0	Output/Output			DA gate pulse output pins. (4 pins)	
PE5/DAA1	Output/Output				
PE6/DAB0	Output/Output				
PE7/DAB1	Output/Output				
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for I/O. I/O can be set in a unit of single bits. (8 pins)			
PF4/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.		
PF5/SO1	I/O/Output		Serial data (CH1) output pin.		
PF6/SI1	I/O/Input		Serial data (CH1) input pin.		
PF7	I/O				

Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/ PBCTL/EC1	Input/Input/Input		Playback CTL input pin.	External event input pin for timer/counter.
PG4/ SYNC0/EC2	Input/Input/Input		Composite sync signal input pins.	External event input pin for timer/counter.
PG5/SYNC1	Input/Input		External input pins for FRC capture unit.	
PG6/EXI0	Input/Input			
PG7/EXI1	Input/Input			
PH0/KR0 to PH2/KR2	I/O/Input	(Port H) 3-bit I/O port. (3 pins)	Key return input signal for key scanning at FDP segment signal. (3 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O can be set in a unit of single bits. (7 pins)	Remote control reception circuit input pin.	
PI2/PWM	I/O/Input		14-bit PWM output pin.	
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.	
PI4/INT1/ NMI/CS0	I/O/Input/ Input/Input		Input pin to request external interruption, non-maskable interruption and for serial chip select (CH0). Active when falling edge.	
PI5/SCK0	I/O/I/O		Serial clock (CH0) I/O pin.	
PI6/SO0	I/O/Output		Serial data (CH0) output pin.	
PI7/SI0	I/O/Input		Serial data (CH0) input pin.	
EXTAL	Input		Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output			
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)		
TX	Output			
RST	Input	System reset pin of active "L" level.		
MP	Input	Test mode pin. Always connect to GND.		
V _{FDP}		FDP voltage supply pin when specifying internal resistor by mask option.		
AV _{DD}		Positive power supply pin of A/D converter.		
AV _{REF}	Input	Reference voltage input pin of A/D converter.		
AV _{SS}		GND pin of A/D converter.		
V _{DD}		Positive power supply pin.		
V _{pp}		Positive power supply pin for incorporated PROM writing connect to V _{DD} during normal operation.		
V _{SS}		GND pin. Connect both V _{SS} pins to GND.		

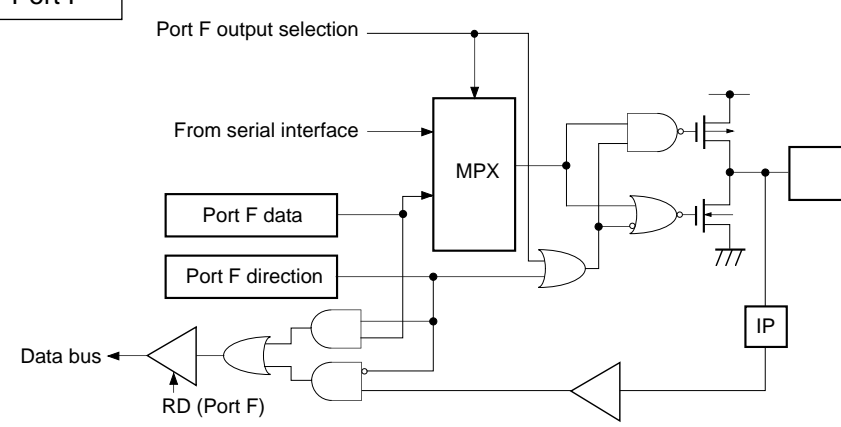
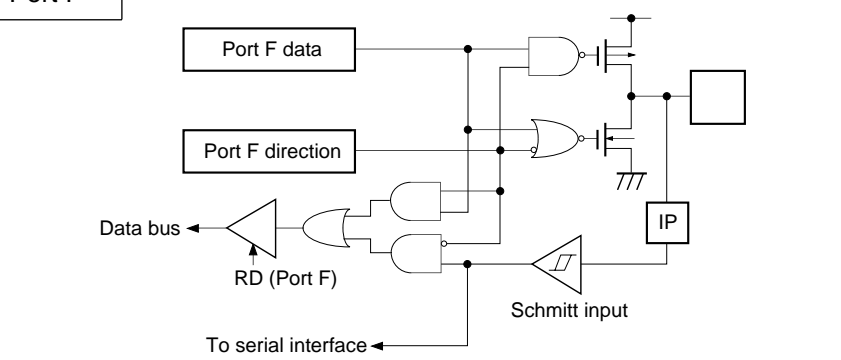
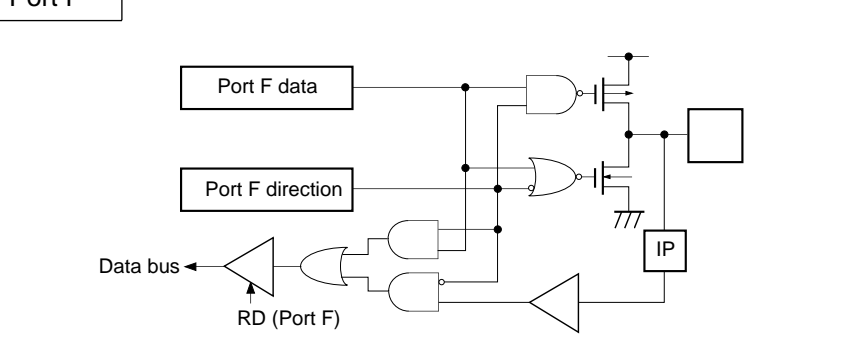
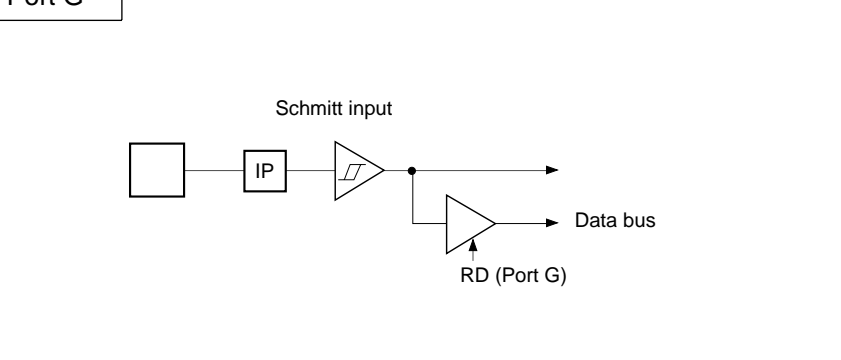
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/PPO0/ HGO</p> <p>1 pin</p>	<p>Port A</p> <p>HSEL HOUT PPO0</p> <p>MPX</p> <p>PA0</p> <p>Data bus</p> <p>RD (Port A)</p> <p>HSEL HOUTE</p> <p>MPX</p> <p>Output becomes active from high impedance by data writing to port register.</p> <p>PPO1</p> <p>PPG control status register bit 0 Tri-state control selection</p> <p>PA1</p> <p>PA1 direction</p> <p>Data bus</p> <p>RD (Port A)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PA1/PPO1</p> <p>1 pin</p>	<p>HSEL HOUTE</p> <p>MPX</p> <p>PA1</p> <p>Data bus</p> <p>RD (Port A)</p> <p>PPO1</p> <p>PPG control status register bit 0 Tri-state control selection</p> <p>PA1 direction</p> <p>IP</p>	<p>Hi-Z</p>
<p>PA2/PPO2 to PA4/PPO4</p> <p>3 pins</p>	<p>Port A</p> <p>PPO data</p> <p>Port A data</p> <p>Port A direction</p> <p>Data bus</p> <p>RD (Port A)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PA5/PPO5 to PA7/PPO7</p> <p>3 pins</p>	<p>Port A</p> <p>PPO data</p> <p>Port A data</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

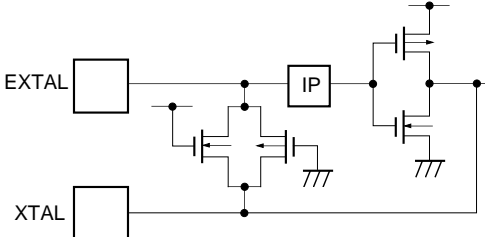
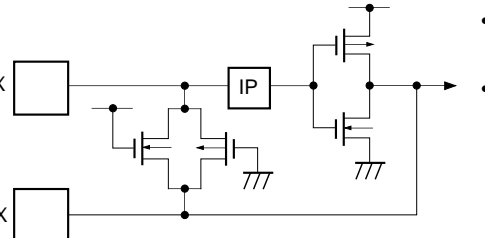
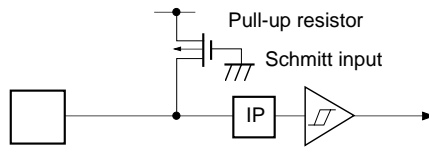
Pin	Circuit format	When reset
<p>PB0 to PB7</p> <p>8 pins</p>	<p>Port B</p> 	<p>Hi-Z</p>
<p>PC0 to PC2</p> <p>3 pins</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pin</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pin</p>	<p>Port C</p>  <p>RTG interruption control register bit 7 Tri-state control selection</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PC5/RTO5 to PC7/RTO7</p> <p>3 pins</p>	<p>Port C</p>	<p>Hi-Z</p>
<p>PD0/S0 to PD7/S7</p> <p>8 pins</p>	<p>Port D</p>	<p>Hi-Z</p>
<p>T0 to T7</p> <p>8 pins</p>		<p>Hi-Z</p>
<p>T8/S15 to T15/S8</p> <p>8 pins</p>		<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{EC0/INT2}}$</p> <p>2 pins</p>	<p>Port E</p> <p>Schmitt input</p> <p>IP</p> <p>$\overline{\text{INT0}}$ $\overline{\text{EC0/INT2}}$</p> <p>Data bus</p> <p>RD (Port E)</p>	Hi-Z
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> <p>Port E function select</p> <p>DA gate output or PWM output</p> <p>MPX</p> <p>Port E data</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Hi-Z control</p>	Hi-Z
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> <p>Port E function select</p> <p>DA gate output</p> <p>MPX</p> <p>Port E data</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Hi-Z control</p>	High level
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> <p>Input multiplexer</p> <p>IP</p> <p>To A/D converter</p> <p>Port F function select</p> <p>Data bus</p> <p>RD (Port F)</p>	Hi-Z
<p>PF4/$\overline{\text{SCK1}}$</p> <p>1 pin</p>	<p>Port F</p> <p>$\overline{\text{SCK1}}$ output enable</p> <p>From serial interface</p> <p>MPX</p> <p>Port F data</p> <p>Port F direction</p> <p>Data bus</p> <p>RD (Port F)</p> <p>To serial interface</p> <p>Schmitt input</p> <p>IP</p>	Hi-Z

Pin	Circuit format	When reset
<p>PF5/SO1</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF6/SI1</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF7</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL/ EC1 PG4/SYNC0/ EC2 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI2/$\overline{\text{PWM}}$ PI3/$\overline{\text{TO}}$/ DDO/ADJ</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>(PI2 ... From 14-bit PWM, timer/counter PI3 ... From CTL duty detection circuit, 32kHz timer)</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/RMC PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$/$\overline{\text{CS0}}$ PI7/SI0</p> <p>3 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>(PI1 ... To remote control circuit PI4 ... To interruption circuit PI7 ... To serial CH0)</p>	<p>Hi-Z</p>
<p>PI5/$\overline{\text{SCK0}}$ PI6/$\overline{\text{SO0}}$</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>From serial CH0</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>Schmitt input</p> <p>Note) PI5 is schmitt input</p> <p>PI5...To serial CH0</p> <p>IP</p>	<p>Hi-Z</p>
<p>PH0/KR0 to PH2/KR2</p> <p>3 pins</p>	<p>Port H</p> <p>Port H data</p> <p>Port H direction</p> <p>Data bus</p> <p>RD (Port H)</p> <p>MPX</p> <p>IP</p> <p>Key input signal</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. 	<p>Hi-Z</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13	V	Incorporated PROM
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Display output voltage	V _{OD}	V _{DD} -4.0 to V _{DD} +0.3	V	As P-channel transistor is open drain, V _{DD} is reference.
High level output current	I _{OH}	-5	mA	All pins excluding display outputs (value per pin)* ³
	I _{ODH1}	-15	mA	Display outputs S0 to S7 (value per pin)
	I _{ODH2}	-35	mA	Display outputs T0 to T7, and T8/S15 to T15/S8 (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all pins excluding display outputs
	∑I _{ODH}	-100	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	
Low level total output current	∑I _{OL}	130	mA	Total for all outputs
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) It specifies output current of general-purpose I/O port.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS}=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
	V _{pp}	V _{pp} = V _{DD}		V	*7
Analog power supply	AV _{DD}	4.5	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4
	V _{IHEX}	V _{DD} -0.4	V _{DD} +0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3
	V _{ILTS}	0	0.8	V	TTL schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	-10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) Normal input port (each pin of PA1 to PA4, PC, PF0 to PF3, PF5, PF7, PH, PI2, PI3 and PI6), MP pin

*3) Each pin of RST, PE0/INT0, PE1/EC0/INT2, PF4/SCK1, PF6/SI1, PI1/RMC, PI4/CS0/NMI/INT1, PI5/SCK0, PI7/SI1, PG0/CFG, PG1/DFG, PG2/DPG, PG3/PBCTL/EC, PG6/EXI0, PG7/EXI1.

*4) Each pin of PG4/SYNC0/EC2, PG5/SYNC1.

*5) It specifies only when the external clock is input.

*6) It specifies only when the external event is input.

*7) V_{pp} and V_{DD} should be set to the same voltage.

DC Characteristics

(Ta=-10 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PC, PE PF4 to PF7,	V _{DD} =4.5V, I _{OH} =-0.5mA	4.0			V
			V _{DD} =4.5V, I _{OH} =-1.2mA	3.5			V
Low level output voltage	V _{OL}	PH, PI1 to PI7	V _{DD} =4.5V, I _{OL} =1.8mA			0.4	V
			V _{DD} =4.5V, I _{OL} =3.6mA			0.6	V
Display output current	I _{OH}	S0 to S7		-8			mA
		S8/T15 to S15/T8, T0 to T7	V _{DD} =4.5V, V _{OH} =V _{DD} -2.5V	-20			mA
Open drain output leakage current (P-CH Tr OFF in state)	I _{LOL}	S0 to S7, S8/T15 to S15/T8, T0 to T7	V _{DD} =5.5V, V _{OL} =V _{DD} -35V V _{FDP} =V _{DD} -35V			-20	μA
Pull-down resistor	R _L	S8/T15 to S15/T8, T0 to T7	V _{DD} =5V, V _{OD} =V _{FDP} =30V	60	100	270	kΩ
Input current	I _{IHE}	EXTAL	V _{DD} =5.5V, V _{IH} =5.5V	0.5		40	μA
			V _{DD} =5.5V, V _{IL} =0.4V	-0.5		-40	μA
	I _{IIE}	TEX	V _{DD} =5.5V, V _{IH} =5.5V	0.1		10	μA
			V _{DD} =5.5V, V _{IL} =0.4V	-0.1		-10	μA
I _{ILR}	$\overline{\text{RST}}$	V _{DD} =5.5V, V _{IL} =0.4V	-1.5		-400	μA	
I/O leakage current	I _{IZ}	PA to PC, PE to PI, AN1 to AN3, MP	V _{DD} =5.5V, V _I =0, 5.5V			±10	μA
Supply current*1	I _{DD1}	V _{DD} , V _{SS}	16MHz crystal oscillation (C ₁ =C ₂ =15pF), V _{DD} =5V±0.5V*2		28	50	mA
	I _{DDS1}		16MHz crystal oscillation (C ₁ =C ₂ =15pF), V _{DD} =5V±0.5V, SLEEP mode		1.7	8	mA
	I _{DD2}		32kHz crystal oscillation (C ₁ =C ₂ =47pF), V _{DD} =3V±0.3V		0.8	2	mA
	I _{DDS2}		32kHz crystal oscillation (C ₁ =C ₂ =47pF), V _{DD} =3V±0.3V, SLEEP mode		3	35	μA
	I _{DDS3}		V _{DD} =5.5V, STOP mode (32kHz, 16MHz oscillation stop)				30
Input capacity	C _{IN}	PA1 to PA4 PC0 to PC7 PE0, PE1 AN0 to AN3 PF0 to PF7 PG0 to PG7 PH0 to PH2 PI1 to PI7	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) When entire output pins are open.

*2) When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=-10 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t _{XL} , t _{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t _{CR} , t _{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t _{EH} , t _{EL}	$\overline{EC0}$, $\overline{EC1}$, EC2	Fig. 3	t _{sys} +200*1			ns
Event count clock input rise and fall times	t _{ER} , t _{EF}	$\overline{EC0}$, $\overline{EC1}$, EC2	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V _{DD} =2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Fig. 1. Clock timing

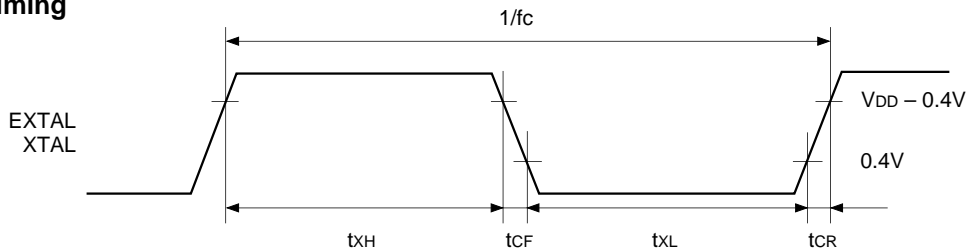


Fig. 2. Clock applied condition

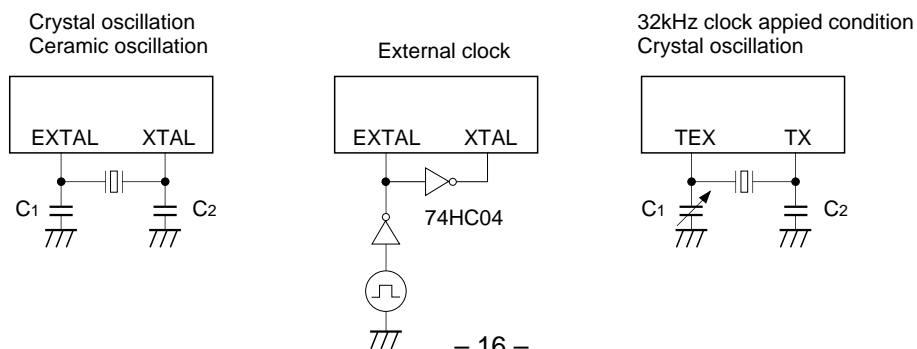
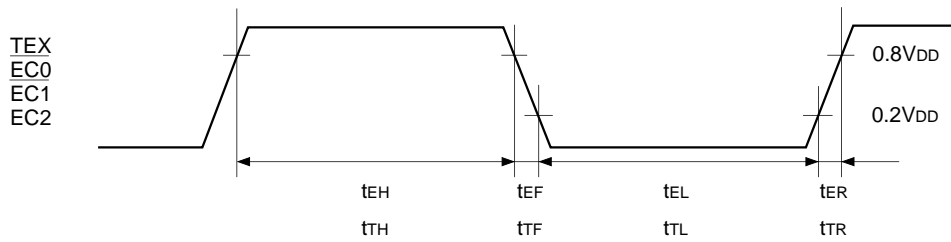


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta=-10 to +75°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

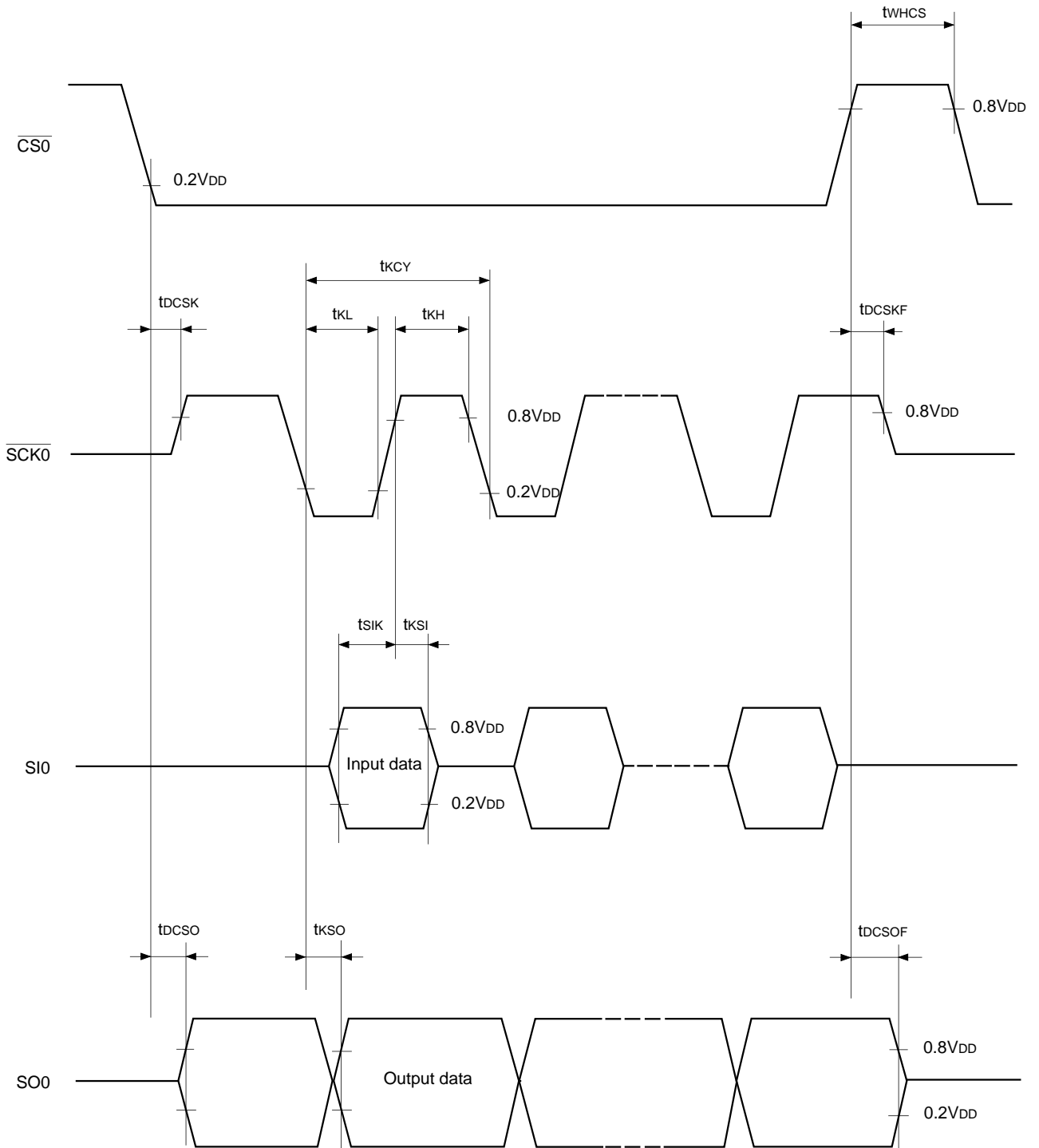
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ =output mode)		$t_{sys}+200$	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ =output mode)		$t_{sys}+200$	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys}+200$	ns
$\overline{CS0} \uparrow \rightarrow SO0$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys}+200$	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys}+200$		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys}+200$		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys}+100$		ns
			Output mode	8000/fc-50		ns
SI0 input set-up time (against $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	$t_{sys}+200$		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		$t_{sys}+200$	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1 t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2 The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF +1TTL.

Fig. 4. Serial transfer timing (CH0)



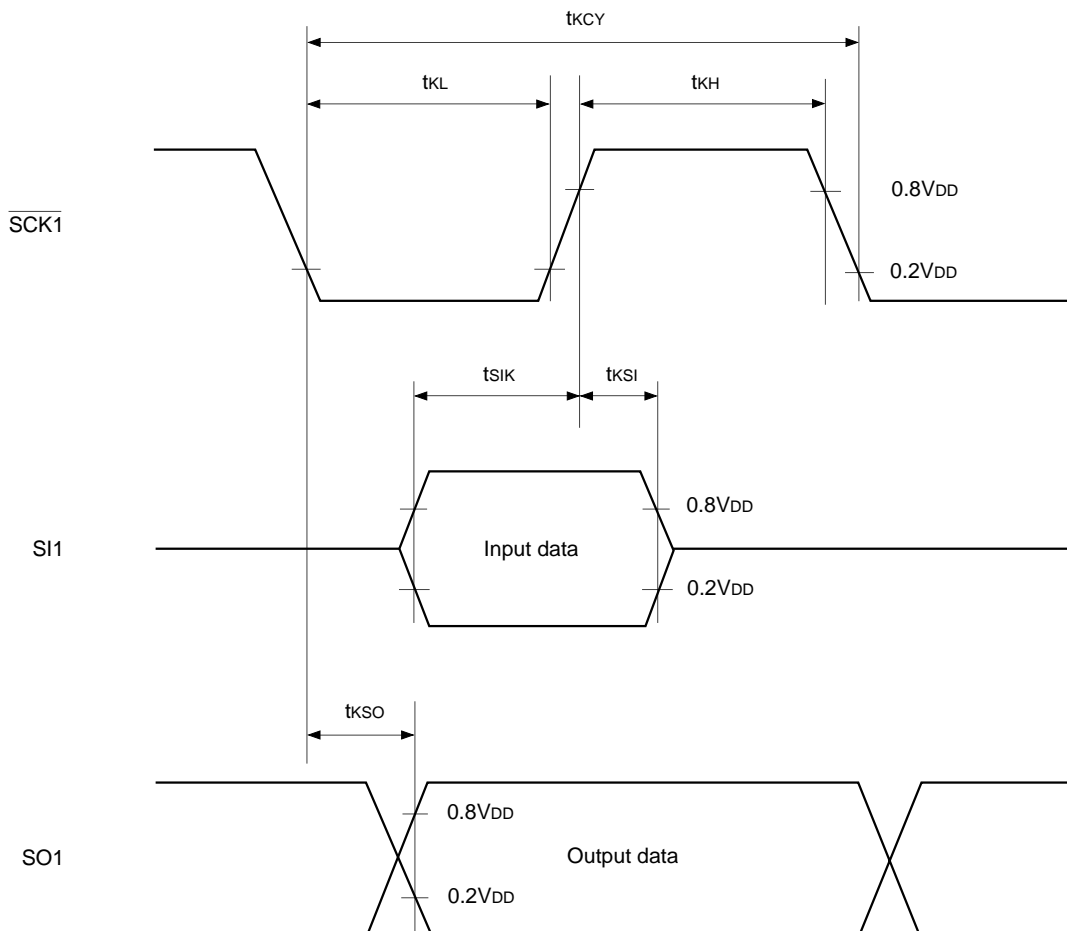
Serial transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

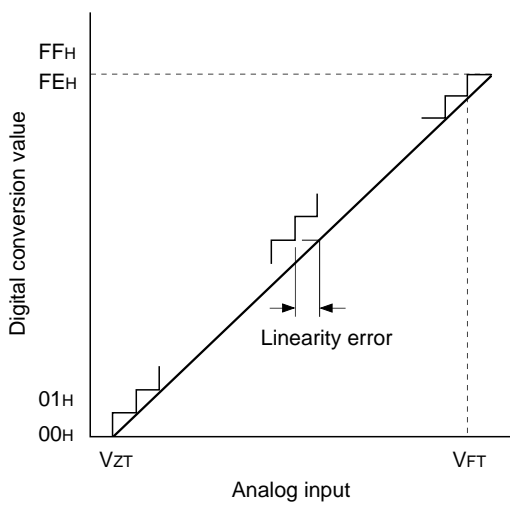
Fig. 5. Serial transfer timing (CH1)



(3) A/D converter characteristics (Ta=-10 to +75°C, VDD=AVDD=4.5 to 5.5V, AVREF=4.0 to AVDD, VSS=AVSS=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta=25°C VDD=AVDD=AVREF=5.0V VSS=AVSS=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t _{CONV}			160/f _{ADC}			µs
Sampling time	t _{SAMP}			12/f _{ADC}			µs
Reference input voltage	V _{REF}	AV _{REF}		AV _{DD} -0.5		AV _{DD}	V
Analog input voltage	V _{IAN}	AN0 to AN7		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode AV _{REF} =4.0 to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode				10

Fig. 6. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: 01FFH bit 0).
 When PS2 is selected, f_{ADC}=fc/2
 When PS1 is selected, f_{ADC}=fc

(4) Interruption, reset input

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

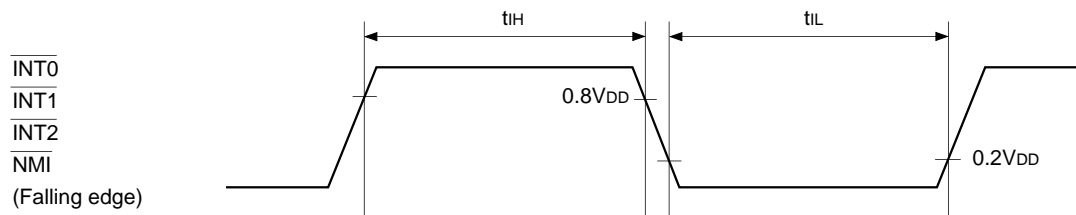
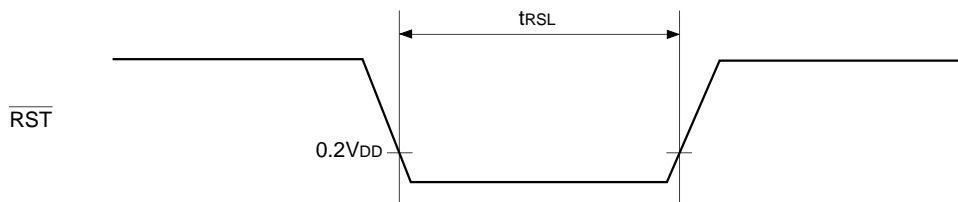


Fig. 8. Reset input timing



(5) Others

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

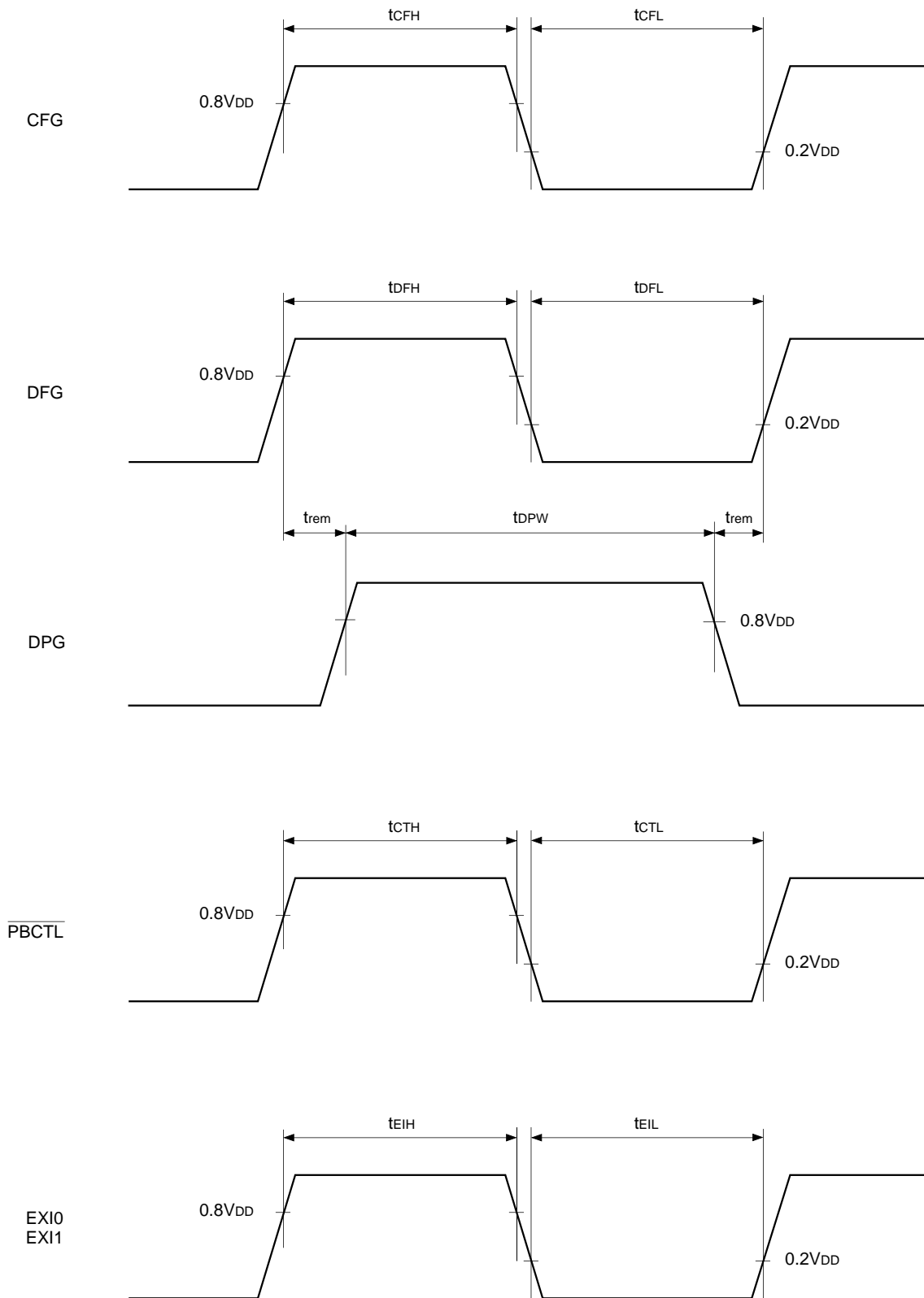
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 16 + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		$t_{FRC} \times 8 + 200$		ns
DPG minimum removal time	t_{rem}	DPG		$t_{FRC} \times 16 + 200$		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{\text{PBCTL}}$	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + t_{sys} + 200$		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + t_{sys} + 200$		ns

Note 1 t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2 bits="00"), $4000/f_c$ (Upper 2 bits="01"), $16000/f_c$ (Upper 2 bits="11")

Note 2 $t_{FRC} = 1000/f_c$ (ns)

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Product list

Option item	Mask product	CXP881P60Q-1-□□□*2
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	16K/20K/24K (CXP88216/88220/88224) 32K/40K (CXP88132/88140) 52K/60K (CXP88152/88160)	PROM 60K bytes
Reset pin pull-up resistor	Existent/non-existent	Existent
Input circuit format*1	CMOS schmitt /TTL schmitt	TTL schmitt
High voltage drive output port pull-down resistor	Existent/non-existent	Existent*3

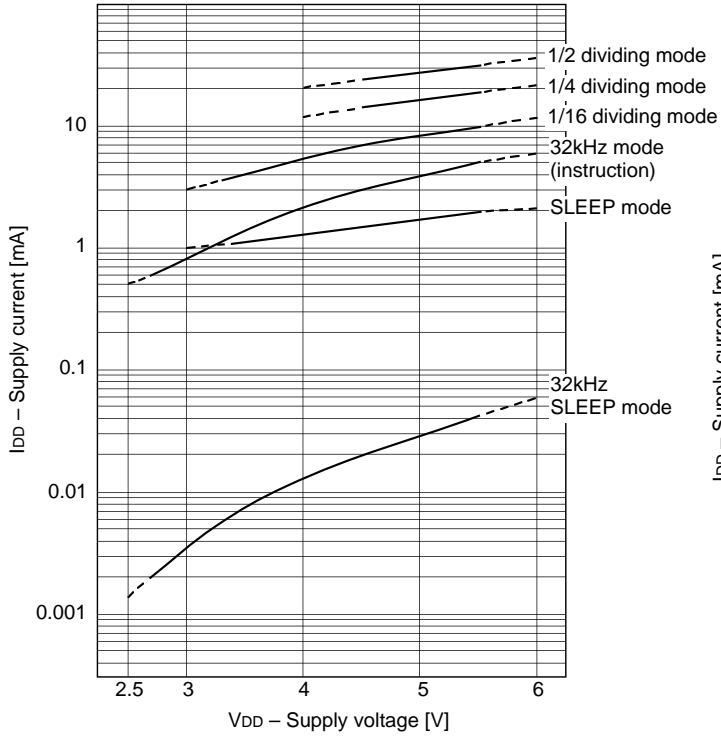
*1 In PG4/SYNC0/EC2 pin and PG5/SYNC1 pin only.

*2 OEM No.

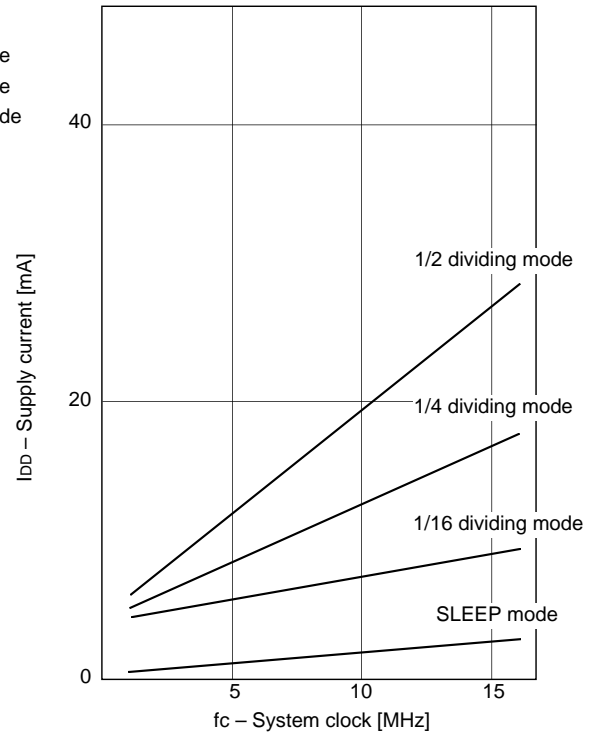
*3 No pull-down resistor for PD0/S0 to PD7/S7 pins.

Characteristics Curve

I_{DD} vs. V_{DD}
(f_c = 16MHz, T_a = 25°C, Typical)



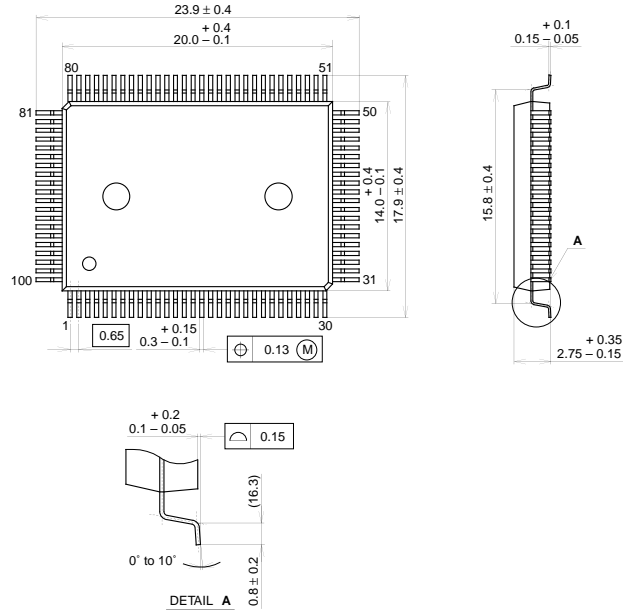
I_{DD} vs. f_c
(V_{DD} = 5.0V, T_a = 25°C, Typical)



Package Outline

Unit: mm

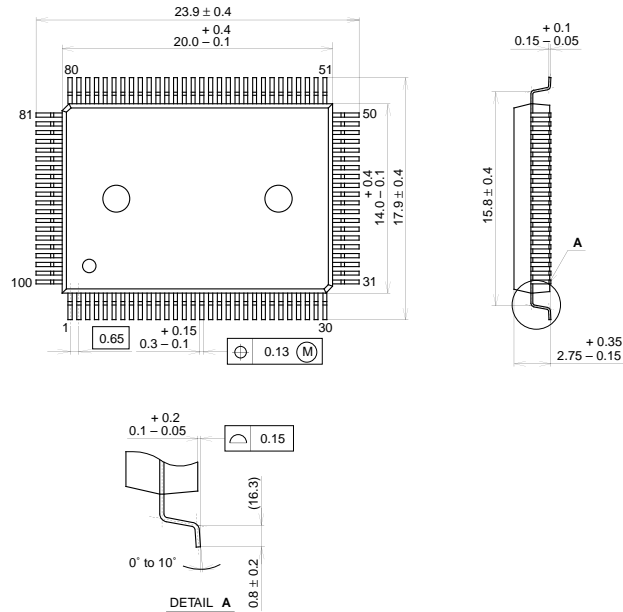
100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	QFP100-P-1420	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	QFP100-P-1420	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm