

Features

- High performance ULC family suitable for large-sized CPLDs and FPGAs
- Conversion to 1,000,000 gates
- Pin counts to over 976 pins
- Any pin-out matched due to limited number of dedicated pads
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, BGA, PGA/PPGA
- Low quiescent current: 0.3 nA/gate
- Available in commercial and industrial grades
- 0.35 μ m Drawn CMOS, 3 and 4 Metal Layers
- Library Optimised for Synthesis, Floor Plan & Automatic Test Pattern Generation (ATPG)
- High Speed Performances:
 - 150 ps Typical Gate Delay @3.3V
 - Typical 600 MHz Toggle Frequency @3.3V
 - Typical 360 MHz Toggle Frequency @2.5V
- High System Frequency Skew Control:
 - Clock Tree Synthesis Software
- Low Power Consumption:
 - 0.25 μ W/Gate/ MHz @3.3V
 - 0.18 μ W/Gate/ MHz @2.5V
- Power on Reset
- Standard 2, 4, 6, 8,10, 12 and 18mA I/Os
- CMOS/TTL/PCI Interface
- ESD (2 kV) and Latch-up Protected I/O
- High Noise & EMC Immunity:
 - I/O with Slew Rate Control
 - Internal Decoupling
 - Signal Filtering between Periphery & Core

Description

The UA1 series of ULCs is well suited for conversion of large sized CPLDs and FPGAs. Devices are implemented in high-performance CMOS technology with 0.35 μ m (drawn) channel lengths, and are capable of supporting flip-flop toggle rates of 200 MHz at 3.3V and 180 MHz at 2.5V, and input to output delays as fast as 150ps at 3.3V. The architecture of the UA1 series allows for efficient conversion of many PLD architecture and FPGA device types with higher IO count. A compact RAM cell, along with the large number of available gates allows the implementation of RAM in FPGA architectures that support this feature, as well as JTAG boundary-scan and scan-path testing.

Conversion to the UA1 series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100mA or more even when not being clocked. The UA1 series has a very low standby consumption of 0.3nA/gate typically commercial temperature, which would yield a standby current of 42 μ A on a 144,000 gates design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UA1 series provides several options for output buffers, including a variety of drive levels up to 18mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available if required. The UA1 series is designed to allow conversion of high performance 3.3V devices as well as 2.5V devices.



0.35 μ m ULC Series

UA1



Support of mixed supply conversions is also possible, allowing optimal trade-offs between speed and power consumption.

Array Organization

Part Number	Max Pad Count	Full Programmable Usable Pads	Routable Gates	Equivalent FPGA Gates
UA1044	44	36	3729	14916
UA1068	68	60	11760	47044
UA1084	84	76	19734	78936
UA1100	100	92	29760	119040
UA1120	120	112	42211	168844
UA1132	132	124	52222	208888
UA1144	144	136	63298	253192
UA1160	160	152	79866	319464
UA1184	184	176	107538	430152
UA1208	208	200	13124	525296
UA1228	228	220	160020	640080
UA1256	256	240	204552	818208
UA1304	304	288	292288	1169152
UA1352	352	336	369164	1476656
UA1388	388	372	451269	1805076
UA1432	432	416	565431	2261724
UA1484	484	468	658314	2633256
UA1540	540	516	826353	3305412
UA1600	600	576	1025460	4101840
UA1700	700	676	1407636	5630544
UA1800	800	776	1691906	6767624
UA1900	900	876	2151765	8607060
UA1976	976	952	2360609	9226436

Architecture

The basic element of the UA1 family is called a cell. One cell can typically implement between one to four FPGA gates. Cells are located contiguously through out the core of the device, with routing resources provided in three to four metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O buffer interfacing

I/O Flexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator could be located close to each buffer.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 2 to 18mA at 3.3V according to the chosen option. 36mA achievable, using 2 pads.

Slew Rate Controlled Output Buffer

In this mode, the p- and n-output transistors commands are delayed, so that they are never set "ON" simultaneously, resulting in a low switching current and low noise. These buffers are dedicated to very high load drive.

2.5V Compatibility

The UA1 series of ULC's is fully capable of supporting high-performance operation at 2.5V or 3.3V. The performance specifications of any given ULC design however, must be explicitly specified as 2.5V, 3.3V or both.

Power Supply and Noise Protection

The speed and density of the UA1 technology cause large switching current spikes, for example when:

- 16 high current output buffers switch simultaneously, or
- 10% of the 700 000 gates are switching within a window of 1ns.

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the setting time of the current and causes voltage drops on the power supply lines. These drops can affect the behavior of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the UA1 core matrix, several mechanisms have been implemented inside the UA1 arrays. Two types of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O buffers switching protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.

- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial V_{DD} and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the V_{DD} supply of the matrix to the external world via the output buffers.

Absolute Maximum Ratings

Max Supply Core Voltage (V_{DD})	3.6V
Max Supply Periphery Voltage (V_{DD5})	5.5V
InputVoltage (V_{IN}) V_{DD}	+ 0.5V
5V Tolerant/Compliant V_{DD5}	+ 0.5V
Storage Temperature	-65° to 150°C
Operating Ambient Temperature	-55° to 125°C

Recommended Operating Range

V_{DD}	2.5V \pm 5% or 3.3V
Operating Temperature	
Commercial	0° to 70°C
Industrial	-40° to 85°C

DC Characteristics

2.5V

Specified at $V_{DD} = +2.5V$

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	°C	
VDD	Supply Voltage	All	2.3	2.5	2.7	V	
IIH	High level input current	CMOS			10	μA	$V_{IN} = V_{DD}, V_{DD} = V_{DD}(\max)$
		PCI			10		
IIL	Low Level input current	CMOS	-10			μA	$V_{IN} = V_{SS}, V_{DD} = V_{DD}(\max)$
		PCI					
IOZ	High-Impedance State Output Current	All	-10		10	μA	$V_{IN} = V_{DD}$ or V_{SS} , $V_{DD} = V_{DD}(\max)$, No Pull-up
IOS	Output short-circuit current	PO11		9		mA	$V_{OUT} = V_{DD}, V_{DD} = V_{DD}(\max)$ $V_{OUT} = V_{SS}, V_{DD} = V_{DD}(\max)$
		PO11		6			
VIH	High-level Input Voltage	CMOS	$0.7V_{DD}$			V	
		PCI	$0.475V_{DD}$				
		CMOS Schmitt	$0.7V_{DD}$				
VIL	Low-Level Input Voltage	CMOS			$0.3V_{DD}$	V	
		PCI			$0.325V_{DD}$		
		CMOS Schmitt			$0.3V_{DD}$		
Vhys	Hysteresis	CMOS Schmitt		0.5		V	
VOH	High-Level output voltage	PO11	$0.7V_{DD}$			V	$I_{OH} = 1.4mA, V_{DD} = V_{DD}(\min)$ $I_{OH} = -500\mu A$
		PCI	$0.9V_{DD}$				
VOL	Low-Level output voltage	PO11			0.4	V	$I_{OL} = 1.4mA, V_{DD} = V_{DD}(\min)$ $I_{OL} = 1.5mA$
		PCI			$0.1V_{DD}$		

3.3V

Specified at $V_{DD} = +3.3V$

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	°C	
V_{DD}	Supply Voltage	All	3.0	3.3	3.6	V	
I _{IH}	High level input current	CMOS			10	μA	$V_{IN} = V_{DD}, V_{DD} = V_{DD(max)}$
		PCI			10		
I _{IL}	Low Level input current	CMOS	-10			μA	$V_{IN} = V_{SS}, V_{DD} = V_{DD(max)}$
		PCI					
I _{OZ}	High-Impedance State Output Current	All	-10		10	μA	$V_{IN} = V_{DD}$ or V_{SS} , $V_{DD} = V_{DD(max)}$, No Pull-up
I _{OS}	Output short-circuit current	PO11		14		mA	$V_{OUT} = V_{DD}, V_{DD} = V_{DD(max)}$ $V_{OUT} = V_{SS}, V_{DD} = V_{DD(max)}$
		PO11		-9			
V _{IH}	High-level Input Voltage	CMOS, LVTTTL	2.0			V	
		PCI	0.475V _{DD}				
		CMOS Schmitt	2.0				
V _{IL}	Low-Level Input Voltage	CMOS			0.8	V	
		PCI			0.325V _{DD}		
		CMOS/TTL-level Schmitt			1.1		
V _{hys}	Hysteresis	TTL-level Schmitt		0.6		V	
V _{OH}	High-Level output voltage	PO11	0.7V _{DD}			V	I _{OH} = 2mA, V _{DD} = V _{DD(min)} I _{OH} = -500μA
		PCI	0.9V _{DD}				
V _{OL}	Low-Level output voltage	PO11			0.4	V	I _{OL} = 2mA, V _{DD} = V _{DD(min)} I _{OL} = 1.5mA
		PCI			0.1V _{DD}		

5V

 Specified at $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-55		+125	°C	
V _{DD}	Supply Voltage	5V Tolerant	3.0	3.3	3.6	V	
V _{DD5}	Supply Voltage	5V Compliant	4.5	5.0	5.5	V	
I _{IH}	High level input current	CMOS			10	μA	V _{IN} = V _{DD} , V _{DD} = V _{DD} (max)
		PCI			10		
I _{IL}	Low Level input current	CMOS	-10			μA	V _{IN} = V _{SS} , V _{DD} = V _{DD} (max)
		PCI					
I _{OZ}	High-Impedance State Output Current	All	-10		10	μA	V _{IN} = V _{DD} or V _{SS} , V _{DD} = V _{DD} (max), No Pull-up
I _{OS}	Output short-circuit current	PO11V		8		mA	V _{OUT} = V _{DD} , V _{DD} = V _{DD} (max) V _{OUT} = V _{SS} , V _{DD} = V _{DD} (max)
		PO11V		-7			
V _{IH}	High-level Input Voltage	PICV, PICV5	2.0	5.0	5.5	V	
		PCI	0.475V _{DD}	5.0	5.5		
		CMOS/TTL-level Schmitt	2.0	1.7			
V _{IL}	Low-Level Input Voltage	PICV, PICV5		0.5V _{DD}	0.8	V	
		PCI			0.325V _{DD}		
		CMOS/TTL-level Schmitt		1.1	0.8		
V _{hys}	Hysteresis	TTL-level Schmitt		0.6		V	
V _{OH}	High-Level output voltage	PO11V	0.7V _{DD}			V	I _{OH} = -1.7mA I _{OH} = -1.7mA
		PO11V5	0.7V _{DD5}				
V _{OL}	Low-Level output voltage	PO11V			0.5	V	I _{OL} = 1.7mA
		PO11V5			0.5		

I/O Buffer

Symbol	Parameter	Typ	Unit	Conditions
C _{IN}	Capacitance, Input Buffer (Die)	2.4	pF	3.3V
C _{OUT}	Capacitance, Output Buffer (Die)	5.6	pF	3.3V
C _{I/O}	Capacitance, Bidirectional	6.6	pF	3.3V



Atmel Sales Offices

France

3, Avenue du Centre
78054 St.-Quentin-en-Yvelines
Cedex
France
Tel: 33130 60 70 00
Fax: 33130 60 71 11

Germany

Erfurter Strasse 31
85386 Eching
Germany
Tel: 49893 19 70 0
Fax: 49893 19 46 21

Kruppstrasse 6
45128 Essen
Germany
Tel: 492 012 47 30 0
Fax: 492 012 47 30 47

Theresienstrasse 2
74072 Heilbronn
Germany
Tel: 4971 3167 36 36
Fax: 4971 3167 31 63

Italy

Via Grosio, 10/8
20151 Milano
Italy
Tel: 390238037-1
Fax: 390238037-234

Spain

Principe de Vergara, 112
28002 Madrid
Spain
Tel: 3491564 51 81
Fax: 3491562 75 14

Sweden

Kavallerivaegen 24, Rissne
17402 Sundbyberg
Sweden
Tel: 468587 48 800
Fax: 468587 48 850

United Kingdom

Easthampstead Road
Bracknell, Berkshire RG12 1LX
United Kingdom
Tel: 441344707 300
Fax: 441344427 371

USA

2325 Orchard Parkway
San Jose
California 95131
USA-California
Tel: 1408441 0311
Fax: 1408436 4200

1465 Route 31, 5th Floor
Annandale
New Jersey 08801
USA-New Jersey
Tel: 1908848 5208
Fax: 1908848 5232

Hong Kong

77 Mody Rd., Tsimshatsui East,
Rm.1219
East Kowloon
Hong Kong
Tel: 85223789 789
Fax: 85223755 733

Korea

Ste.605,Singsong Bldg. Young-
deungpo-ku
150-010 Seoul
Korea
Tel: 8227851136
Fax: 8227851137

Singapore

25 Tampines Street 92
Singapore 528877
Rep. of Singapore
Tel: 65260 8223
Fax: 65787 9819

Taiwan

Wen Hwa 2 Road, Lin Kou
Hsiang
244 Taipei Hsien 244
Taiwan, R.O.C.
Tel: 88622609 5581
Fax: 88622600 2735

Japan

1-24-8 Shinkawa, Chuo-Ku
104-0033 Tokyo
Japan
Tel: 8133523 3551
Fax: 8133523 7581

Web site

<http://www.atmel-wm.com>

© Atmel Nantes SA, 2001.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.



Printed on recycled paper.