Very Low Power/Voltage CMOS SRAM
128K X 8 bit

BS62LV1024

■ FEATURES

- Wide Vcc operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
  - Vcc = 3.0V C-grade : 20mA (Max.) operating current
    I- grade : 25mA (Max.) operating current
    0.02uA (Typ.) CMOS standby current
  - Vcc = 5.0V C-grade : 35mA (Max.) operating current
    I- grade : 40mA (Max.) operating current
    0.4uA (Typ.) CMOS standby current
- High speed access time :
  - -70 70ns (Max.) at Vcc = 3.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with CE2, $\overline{CE1}$, and $\overline{OE}$ options

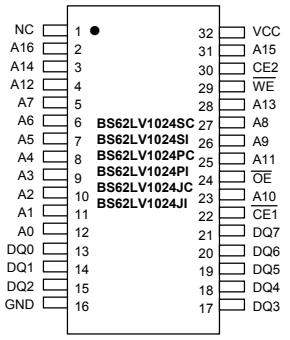
■ DESCRIPTION

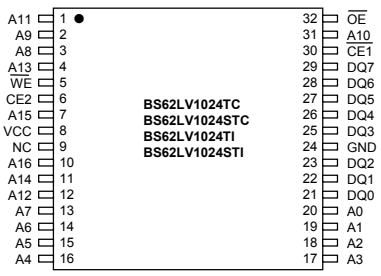
The BS62LV1024 is a high performance, very low power CMOS Static Random Access Memory organized as 131,072 words by 8 bits and operates from a wide range of 2.4V to 5.5V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.02uA and maximum access time of 70ns in 3V operation.
Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), an active HIGH chip enable (CE2), and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The BS62LV1024 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS62LV1024 is available in DICE form, JEDEC standard 32 pin 450mil Plastic SOP, 300mil Plastic SOJ, 600mil Plastic DIP, 8mmx13.4mm STSOP and 8mmx20mm TSOP.

■ PRODUCT FAMILY

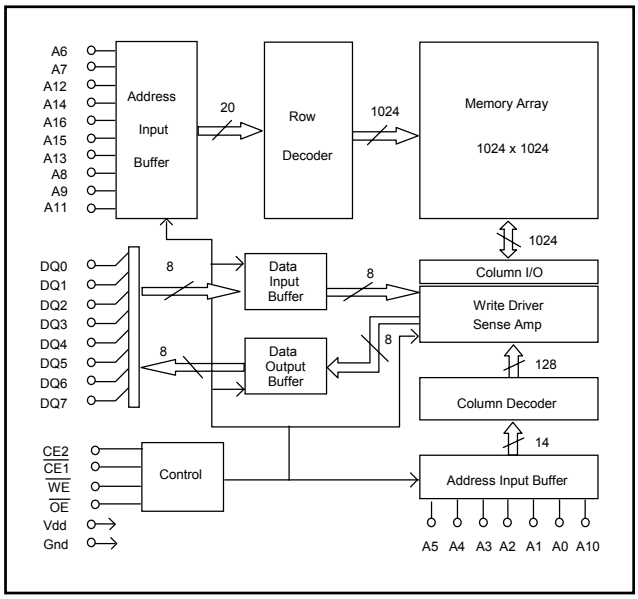
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				Standby (IccSB1, Max)		Operating (Icc, Max)		
			Vcc=3V	Vcc=5V	Vcc=3V	Vcc=5V	Vcc=3V	
BS62LV1024SC	+0°C to +70°C	2.4V ~ 5.5V	70	3.0uA	1.0uA	35mA	20mA	SOP-32
BS62LV1024TC								TSOP-32
BS62LV1024STC								STSOP-32
BS62LV1024PC								PDIP-32
BS62LV1024JC								SOJ-32
BS62LV1024DC								DICE
BS62LV1024SI	-40°C to +85°C	2.4V ~ 5.5V	70	5.0uA	1.5uA	40mA	25mA	SOP-32
BS62LV1024TI								TSOP-32
BS62LV1024STI								STSOP-32
BS62LV1024PI								PDIP-32
BS62LV1024JI								SOJ-32
BS62LV1024DI								DICE

■ PIN CONFIGURATIONS





■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A16 Address Input	These 17 address inputs select one of the 131,072 x 8-bit words in the RAM
$\overline{CE1}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected (Power Down)	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	X	L	X		
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	$0^{O}C$ to $+70^{O}C$	2.4V ~ 5.5V
Industrial	$-40^{O}C$ to $+85^{O}C$	2.4V ~ 5.5V

■ CAPACITANCE (1) (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=3.0V	-0.5	--	0.8	V
			Vcc=5.0V				
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=3.0V	2.0	--	Vcc+0.2	V
			Vcc=5.0V	2.2			
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc		--	--	1	uA
I_{OL}	Output Leakage Current	Vcc = Max, $\overline{CE1}$= V_{IH}, CE2= V_{IL}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc		--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 2mA	Vcc=3.0V	--	--	0.4	V
			Vcc=5.0V				
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -1mA	Vcc=3.0V	2.4	--	--	V
			Vcc=5.0V				
I_{CC}	Operating Power Supply Current	$\overline{CE1}$ = V_{IL}, or CE2 = V_{IH}, I_{DQ} = 0mA, F = Fmax(3)	Vcc=3.0V	--	--	20	mA
			Vcc=5.0V	--	--	35	
I_{CCSB}	Standby Current-TTL	$\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, I_{DQ} = 0mA, F = Fmax(3)	Vcc=3.0V	--	--	1	mA
			Vcc=5.0V	--	--	2	
I_{CCSB1}	Standby Current-CMOS	$\overline{CE1}$ ≧ Vcc-0.2V, CE2 ≦ 0.2V, V_{IN} ≧ Vcc-0.2V or V_{IN} ≦ 0.2V	Vcc=3.0V	--	0.02	1	uA
			Vcc=5.0V	--	0.4	3	

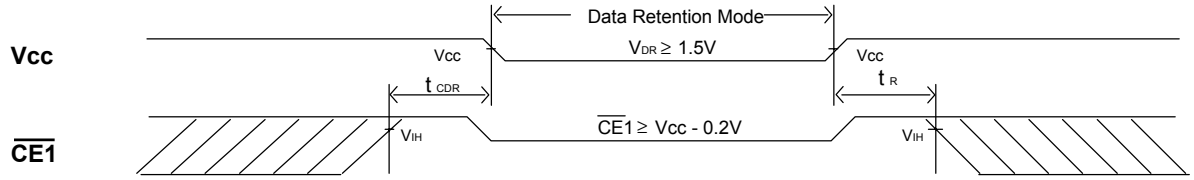
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ DATA RETENTION CHARACTERISTICS (TA = 0°C to + 70°C)

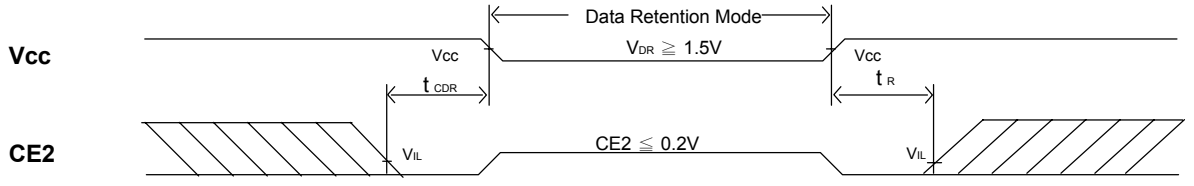
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE1}$ ≧ Vcc - 0.2V, CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE1}$ ≧ Vcc - 0.2V, CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.02	0.3	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

■ AC TEST LOADS AND WAVEFORMS

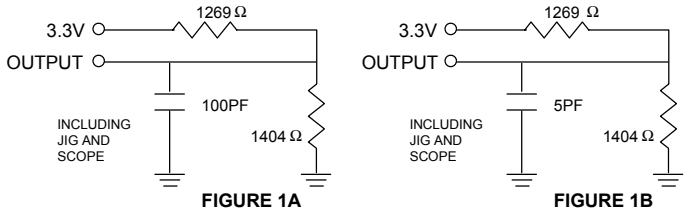


FIGURE 1A FIGURE 1B

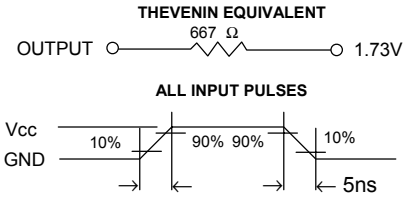


FIGURE 2

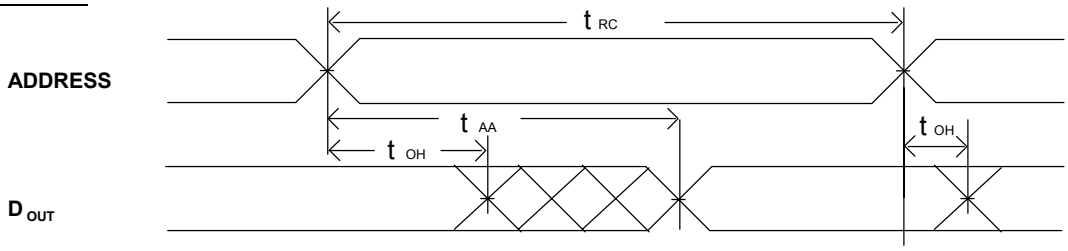
■ AC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C, Vcc=3.0V)

READ CYCLE

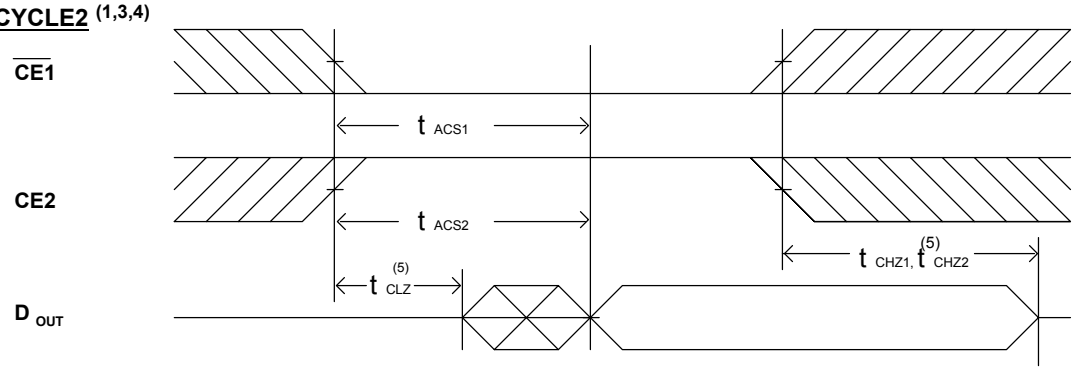
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS62LV1024-70 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	70	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time ($\overline{CE1}$)	--	--	70	ns
t_{E2HOV}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z ($\overline{CE1}$)	10	--	--	ns
t_{E2HOX}	t_{CLZ2}	Chip Select to Output Low Z (CE2)	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	--	--	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z ($\overline{CE1}$)	0	--	40	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z (CE2)	0		40	
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	35	ns
t_{AXOX}	t_{OH}	Output Disable to Address Change	10	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

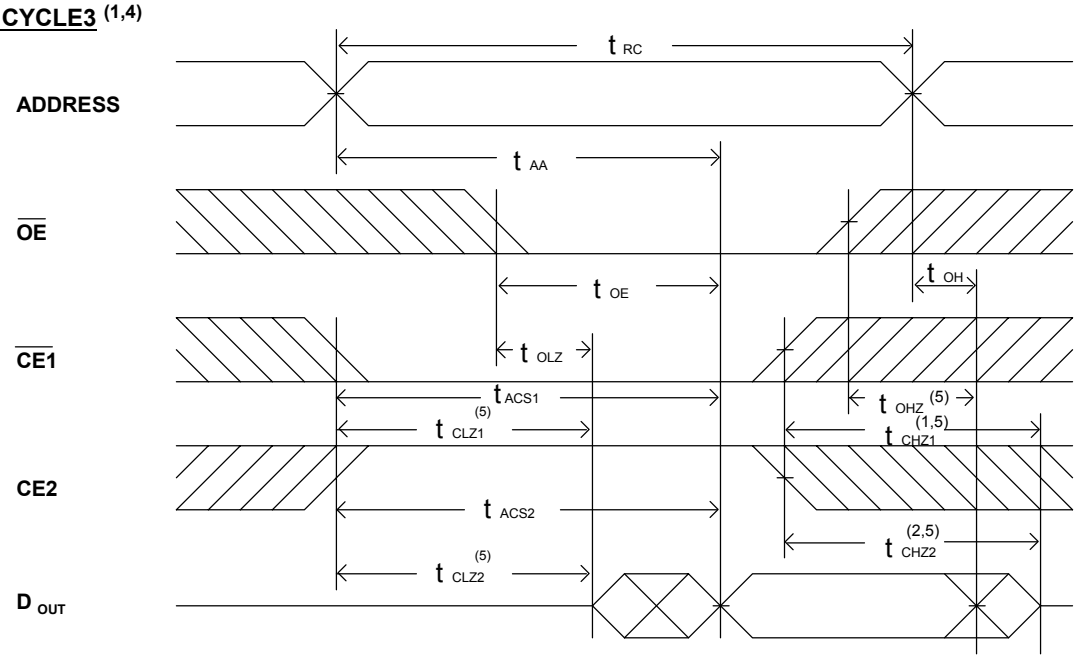
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. WE is high in read Cycle.
2. Device is continuously selected when $\overline{CE1}$ = V_{IL} and CE2= V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or CE2 transition high.
4. $\overline{OE}$ = V_{IL} .
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

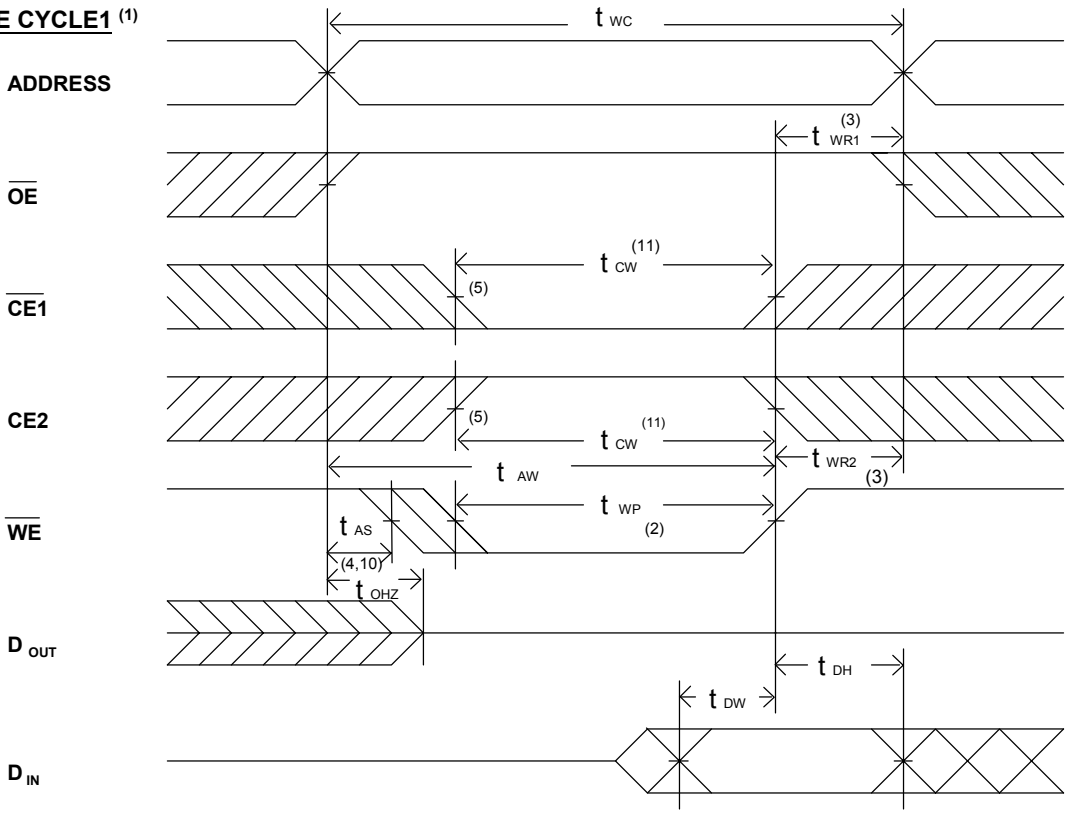
■ AC ELECTRICAL CHARACTERISTICS (TA = 0ºC to + 70ºC, Vcc=3.0V)

WRITE CYCLE

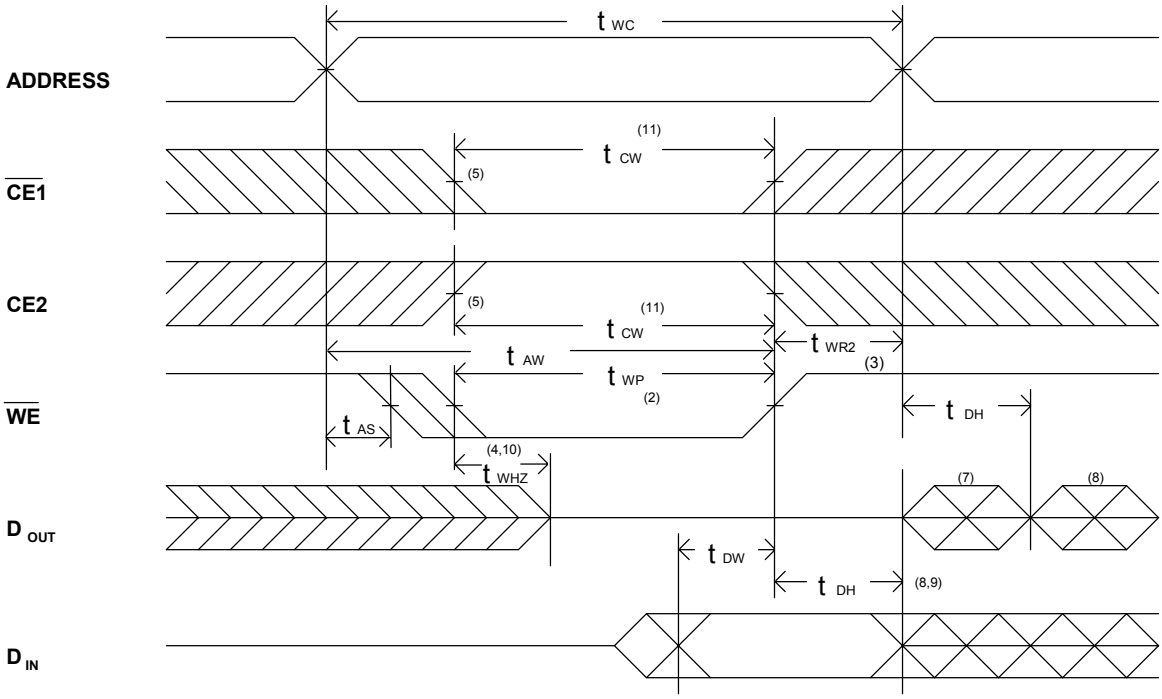
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS62LV1024-70 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	70	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	70	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	--	--	ns
t_{WHAX}	t_{WR1}	Write Recovery Time ($\overline{CE1}$, $\overline{WE}$)	0	--	--	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time (CE2)	0	--	--	ns
t_{WLOZ}	t_{WHZ}	Write to Output in High Z	0	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output in High Z	0	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



WRITE CYCLE2 (1,6)



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE1}$ is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm$500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

■ ORDERING INFORMATION

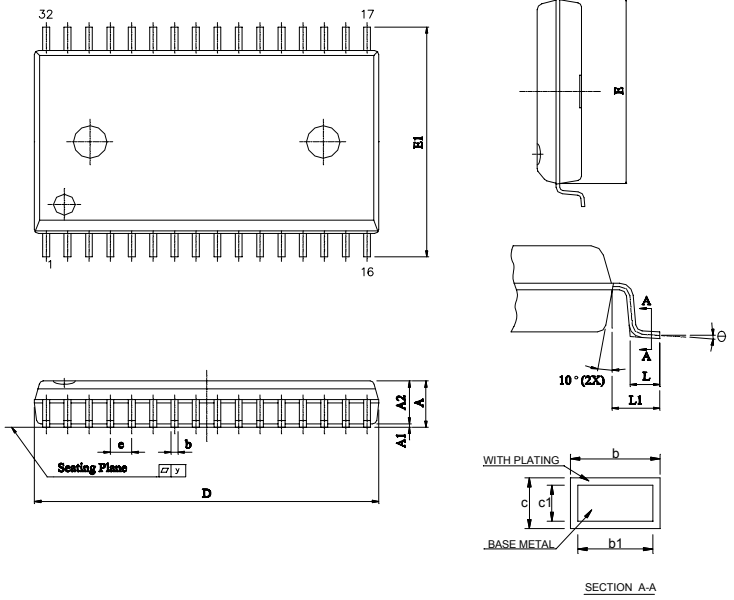
BS62LV1024 X X -- Y Y

SPEED
70: 70ns

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

PACKAGE
J: SOJ
S: SOP
P: PDIP
T: TSOP (8mm x 20mm)
ST: Small TSOP (8mm x 13.4mm)
D: DICE

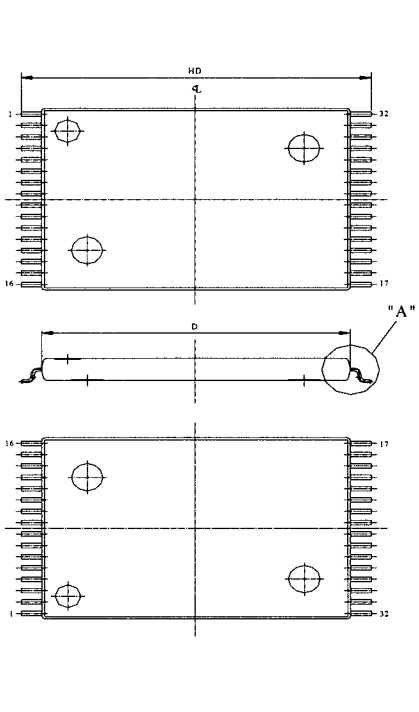
■ PACKAGE DIMENSIONS

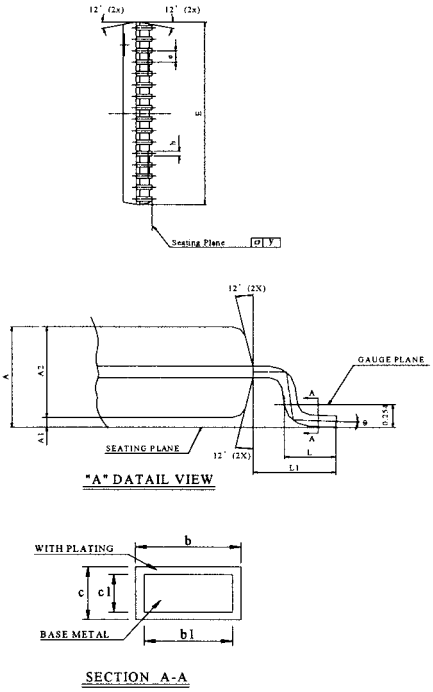


SYMBOL \ UNIT	INCH	MM
A	0.111±0.007	2.821±0.176
A1	0.009±0.005	0.229±0.127
A2	0.1055±0.0055	2.680±0.140
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.46
c	0.006 ~ 0.012	0.15 ~ 0.32
c1	0.006 ~ 0.011	0.15 ~ 0.28
D	0.805±0.005	20.447±0.127
E	0.445±0.005	11.303±0.127
E1	0.555±0.012	14.097±0.305
e	0.050±0.006	1.270±0.152
L	0.033±0.010	0.834±0.25
L1	0.055±0.008	1.397±0.203
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

SOP -32

■ PACKAGE DIMENSIONS (continued)





UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.528± 0.008	13.40± 0.20
L	0.0197 $^{+0.008}_{-0.004}$	0.50 $^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

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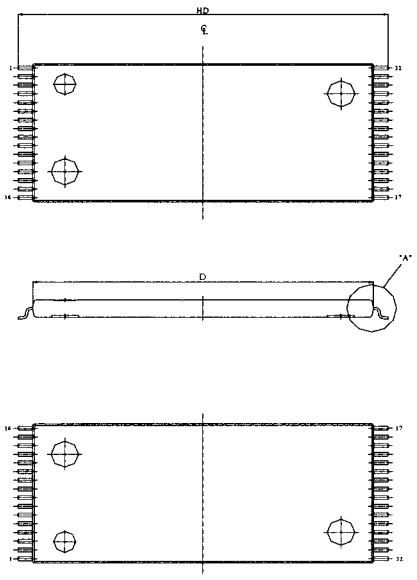

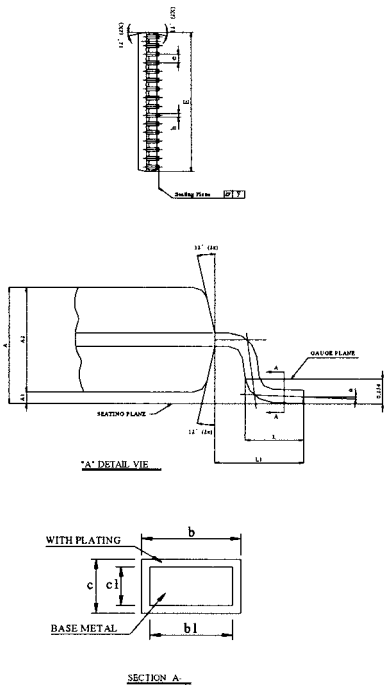

UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.724± 0.004	18.40± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.787± 0.008	20.00± 0.20
L	0.0197 $^{+0.008}_{-0.004}$	0.50 $^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

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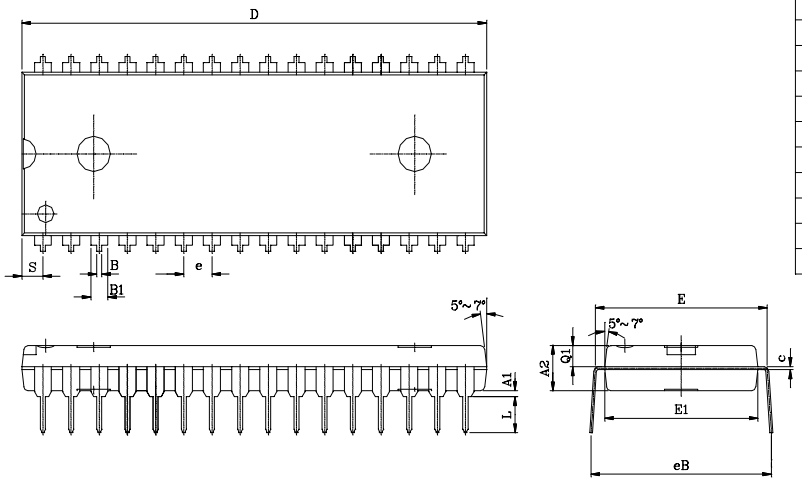
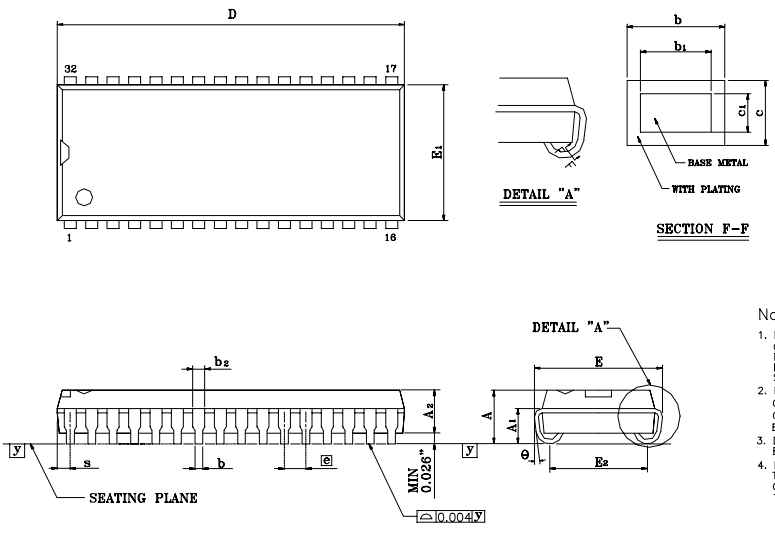
■ PACKAGE DIMENSIONS (continued)

UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.154±0.005	3.912±0.127
B	0.018±0.005	0.457±0.127
B1	0.050±0.005	1.270±0.127
c	0.010±0.004	0.254±0.102
D	1.650±0.005	41.910±0.127
E	0.600±0.010	15.240±0.254
E1	0.544±0.004	13.818±0.102
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508
L	0.130±0.010	3.302±0.254
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127



PDIP - 32

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.128	0.132	0.140	3.25	3.35	3.56
A_1	0.082	—	—	2.08	—	—
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b_2	0.026	0.028	0.032	0.66	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
E	0.330	0.335	0.340	8.39	8.51	8.63
E_1	0.295	0.300	0.305	7.49	7.62	7.75
E_2	0.260	0.267	0.274	6.61	6.78	6.96
e	—	0.050	—	—	1.27	—
s	—	—	0.048	—	—	1.22
y	—	—	0.004	—	—	0.10
θ	-5°	2°	6°	-5°	2°	6°



Note:

1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS, AND GATE BURRS. BUT MOLD MISMATCH IS INCLUDED, MOLD FLASH. TIE BAR BURRS. AND GATE BURRS SHALL NOT EXCEED .006" PER END. DIMENSION E_1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .010" PER SIDE.
2. DIMENSIONS D AND E_1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDEING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
3. DIMENSION S INCLUDES MOLD PROTRUSION. MISMATCH AND SUPPORTING BAR BURRS.
4. DIMENSION b_2 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE b_2 DIMENSION TO BE GREATER THAN .037" THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE b_2 DIMENSION TO BE SMALLER THAN .025"

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REVISION HISTORY

Revision	Description	Date	Note
2.2	**2001 Data Sheet release**	**Apr. 15, 2001**	