Revision History

Revision 1.0 (Oct. 29, 2002)

- Delete "Preliminary", as formal data sheet.

Revision 0.2 (Mar. 13 2001)

-Changed Input leakage current from $\pm2\mu A$ to $\pm5\mu A$
-Changed output leakage current from $\pm2\mu A$ to $\pm5\mu A$
-Added DC current
-Changed AC Characteristics

Parameter	Symbol	Rev. 0.1 -10		Rev. 0.2 -10	
		min	max	min	max
Chip Enable to end of write	t_{CW}	8		7	
Write pulse width, with $\overline{OE}$ HIGH	t_{WP1}	8		7	

-Typo

Revision 0.1 (Dec. 27 2001)

-Original

SRAM **128 K x 8 SRAM**

HIGH SPEED CMOS SRAM

FEATURES

- Fast access times: 8ns, 10ns
- Fast $\overline{OE}$ access times: 4ns, 5ns
- Single +3.3V power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Center power and ground pins for greater noise immunity
- Easy memory expansive with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- High-performance, low-power consumption, CMOS triple-poly, double-metal process

ORDERING INFORMATION

32-pin 300mil SOJ
32-pin 400mil TSOP (TypeII)

| PRODUCT NO.	Access Time (ns)	PACKING TYPE
M21L18128A-8J	8	SOJ
M21L18128A-8T		TSOP
M21L18128A-10J	10	SOJ
M21L18128A-10T		TSOP

GENERAL DESCRIPTION

The M21L18128A is a high speed, low power asynchronous SRAM containing 1,048,576 bits and organized as 131,072 by 8 bits, it is produced by high performance CMOS process.

This device offers center power and ground pins for improved performance and noise immunity. Static design

eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization.

PIN ASSIGNMENT

SOJ Top View

A0	1		32	A16
A1	2		31	A15
A2	3		30	A14
A3	4		29	A13
$\overline{CE}$	5		28	$\overline{OE}$
DQ1	6		27	DQ8
DQ2	7		26	DQ7
V	8		25	GND
GND	9		24	V
DQ3	10		23	DQ6
DQ4	11		22	DQ5
$\overline{WE}$	12		21	A12
A4	13		20	A11
A5	14		19	A10
A6	15		18	A9
A7	16		17	A8

TSOP (TypeII) Top View

A0	1		32	A16
A1	2		31	A15
A2	3		30	A14
A3	4		29	A13
$\overline{CE}$	5		28	$\overline{OE}$
DQ1	6		27	DQ8
DQ2	7		26	DQ7
V	8		25	GND
GND	9		24	V
DQ3	10		23	DQ6
DQ4	11		22	DQ5
$\overline{WE}$	12		21	A12
A4	13		20	A11
A5	14		19	A10
A6	15		18	A9
A7	16		17	A8
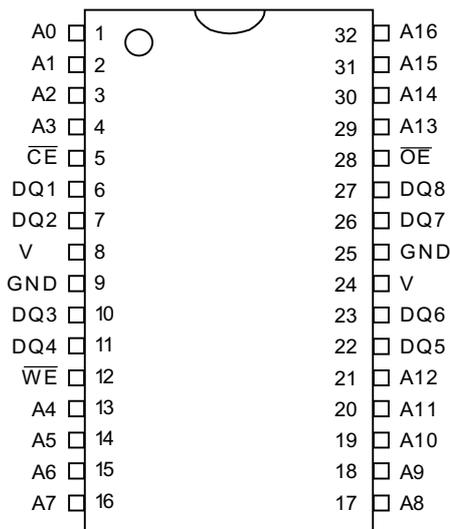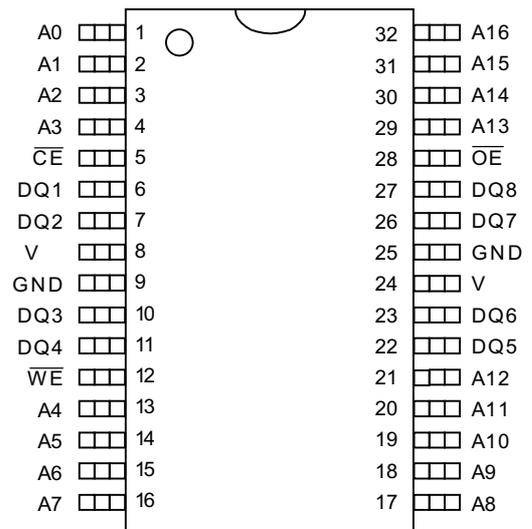
Block Diagram
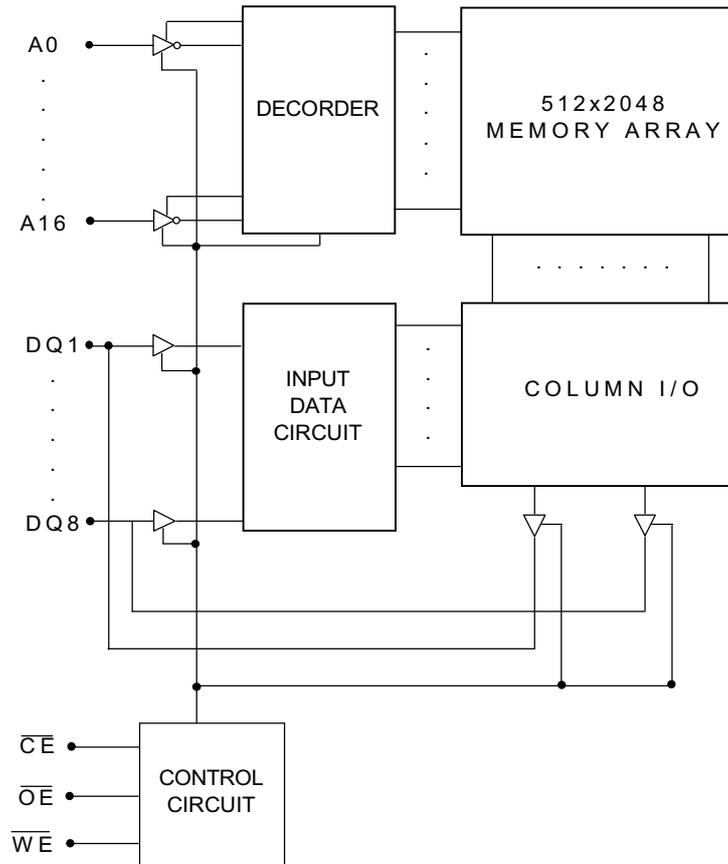
Pin Descriptions

Pin No.	Symbol	Description
1 - 4, 13 - 16, 17-21, 29 - 32	A0 - A16	Address Inputs
5	$\overline{CE}$	Chip Enable Input
6 - 7, 10 - 11, 22 - 23, 26 - 27	DQ1 – DQ8	Data Inputs/Outputs
12	$\overline{WE}$	Write Enable Input
28	$\overline{OE}$	Output Enable Input
8, 24	VCC	Power
9, 25	GND	Ground

ABSOLUTE MAXIMUM RATINGS *

Voltage on V_{CC} Supply Relative to Vss … ……-0.5V to +4.6V

Operating Temperature, Topr   (Commercial)….. 0 °C to +70 °C

Storage Temperature (plastic) ……………….-65 °C to +150 °C

Power Dissipation …..…………………………………1.0W

*Stresses greater than those listed under Absolute Maximum. Ratings may permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0(*1)	3.6	V	1
Supply Voltage		V_{CC}	3.15(*2)	3.6	V	1
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1,2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1,2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-5	5	μ A	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-5	5	μ A	
Output High Voltage	I_{OH} = -4.0 mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}		0.4	V	1

*1 : For all speed grades except M21L18128A -8
*2 : For M21L18128A -8 only

DESCRIPTION	CONDITIONS	SYMBOL	MAX		UNITS	NOTES
			-8	-10		
Power Supply Current : Operating	Device selected; $\overline{CE} \leq V_{IL}$; V_{CC}=MAX; f=f$_{MAX}$; outputs open	I_{CC}	170	160	mA	3
TTL Standby	$\overline{CE} \geq V_{IH}$; V_{CC}=MAX; f=f$_{MAX}$	I_{SB1}	35	30	mA	
CMOS Standby	$\overline{CE} \geq V_{CC}$-0.2; V_{CC} = MAX; all other inputs$\leq$ GND +0.2 or $\geq V_{CC}$ -0.2; all inputs static ; f=0	I_{SB2}	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A= 25°C ; f=1 MHz	C_I	6	pF	4
Input/Output Capacitance(DQ)	V_{CC}=3.3V	$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS (Note 5)

DESCRIPTION	SYMBOL	-8		-10		Unit	Notes
		MIN	MAX	MIN	MAX		
Read Cycle							
Read Cycle Time	t_{RC}	8		10		ns	
Address access time	t_{AA}		8		10	ns	
Chip Enable access time	t_{ACE}		8		10	ns	
Output hold from address change	t_{OH}	3		3		ns	
Chip Enable to output in Low-Z	t_{CLZ}	3		3		ns	4,7
Chip disable to output in High-Z	t_{CHZ}		4		5	ns	4,6,7
Output Enable access time	t_{OE}		4		5	ns	
Output Enable to output in Low-Z	t_{OLZ}	0		0		ns	
Output Disable to output in High-Z	t_{OHZ}		4		5	ns	4,6
Chip Enable to Power Up time	t_{PU}	0		0			
Chip Enable to Power Down time	t_{PD}		8		10		
Write Cycle							
Write cycle time	t_{WC}	8		10		ns	
Chip Enable to end of write	t_{CW}	6		7		ns	
Address valid to end of write, with $\overline{OE}$ HIGH	t_{AW}	8		8		ns	
Address setup time	t_{AS}	0		0		ns	
Address hold from end of write	t_{WR}	0		0		ns	
Write pulse width	t_{WP2}	8		10		ns	
Write pulse width, with $\overline{OE}$ HIGH	t_{WP1}	6		7		ns	
Data setup time	t_{DW}	5		5		ns	
Data hold time	t_{DH}	0		0		ns	
Write disable to output in Low-Z	t_{OW}	3		3		ns	4,7
Write to output in High-Z	t_{WHZ}		4		5	ns	4,6,7

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	DQ1-DQ8	POWER
READ	L	H	L	Q	ACTIVE
WRITE	L	L	X	D	ACTIVE
OUTPUT DISABLE	L	H	H	HIGH-Z	ACTIVE
STANDBY	H	X	X	HIGH-Z	STANBY

AC TEST CONDITIONS

Input plus levels	0V to 3.0V
Input rise and fail times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2
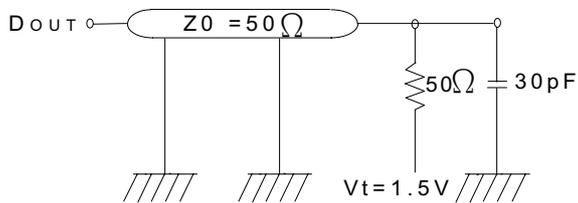
Fig.1 OUTPUT LOAD EQUIVALENT
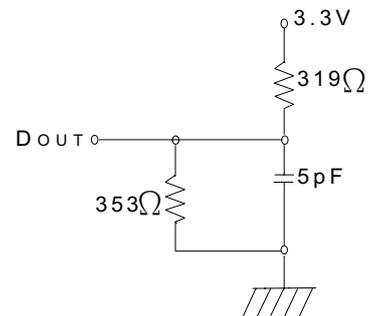
Fig.2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to GND (VSS).

2. Overshoot : $V_{IH} \leq$ +6.0V for t $\leq t_{RC}$ /2.

   Undershoot : $V_{IL} \leq$ -2.0V for t $\leq t_{RC}$ /2.

3. I_{CC} is given without output current. ICC increases with greater output loading and faster cycle times.

4. This parameter is sampled.

5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.

6. Output loading is specified with CL=5pF as in Fig.2. Transition is measured ± 500mV from steady static voltage.

7. At any give temperature and voltage conditions, t_{CHZ} is less than t_{CLZ} and t_{WHZ} is less than t_{OW}

8. $\overline{WE}$ is High for Read cycle.

9. Device is continuously selected. Chip enable and output enables are held in their active state.

10. Address valid prior to, or coincident with, latest occurring chip enable.

11. t_{RC}=Read Cycle Time.

12. Chip Enable and Write Enable can initiate and terminate a Write cycle.

13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

Timing Waveforms

Read Cycle 1[8, 9]
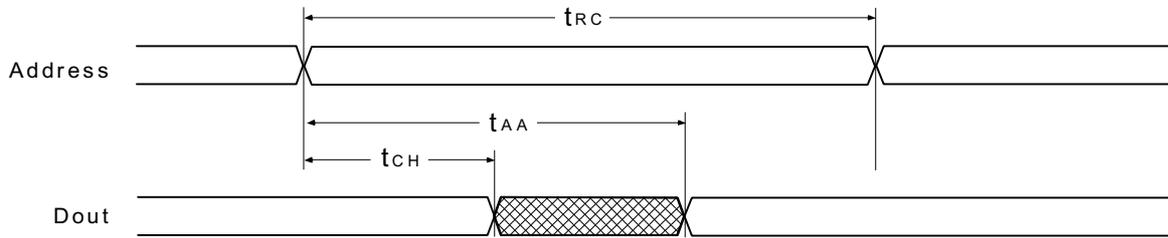
Read Cycle 2[7, 8, 9, 10]
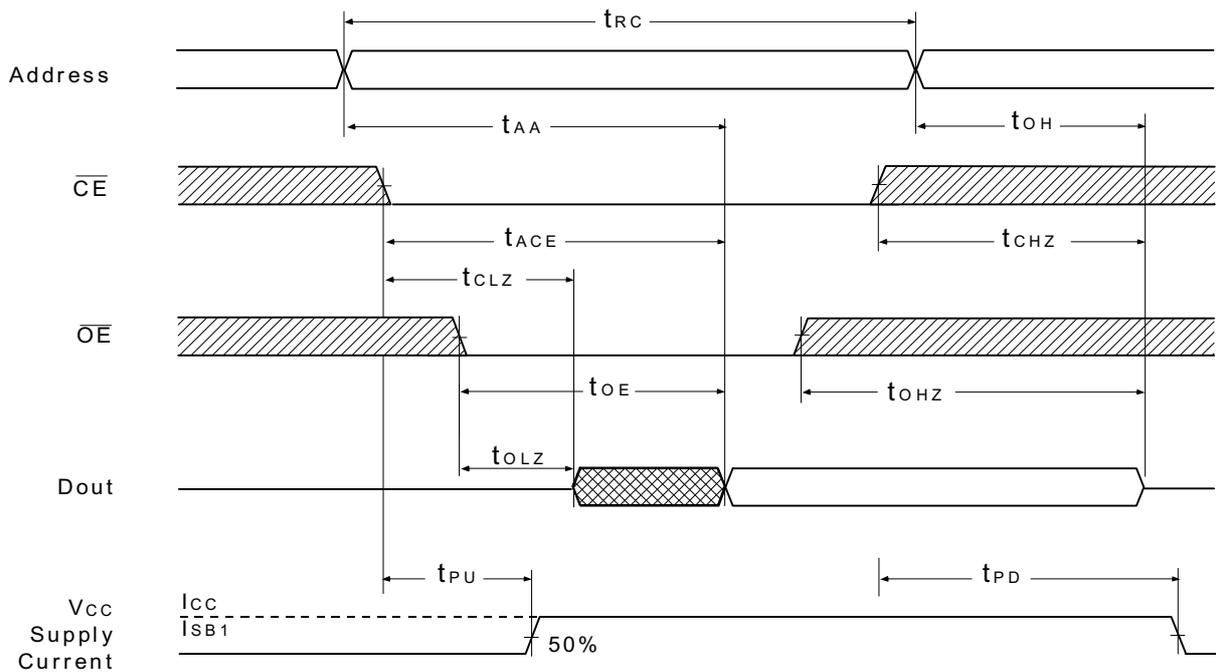
▨ : DON'T CARE

▩ : UNDEFINED

Timing Waveforms   (continued)

Write Cycle 1[7, 12, 13]

(Write Enable Controlled with Output Enable $\overline{OE}$ active LOW)

DON'T CARE
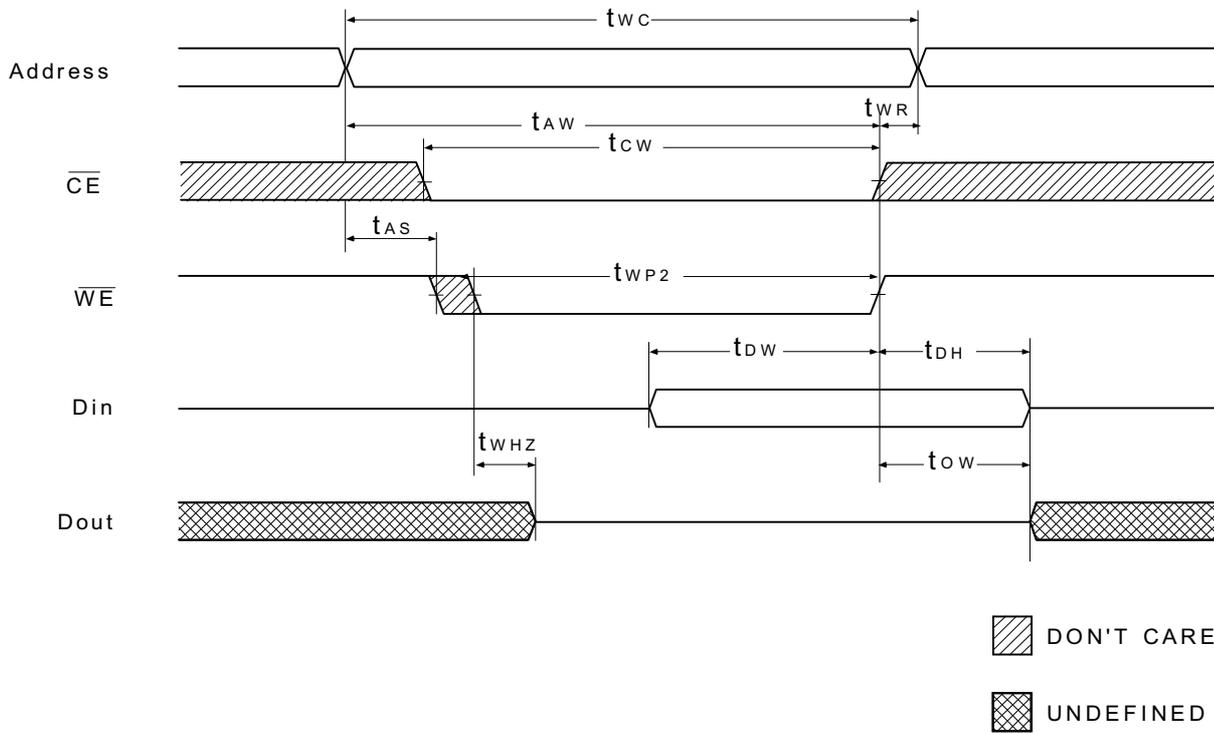
UNDEFINED

Timing Waveforms   (continued)

Write Cycle 2[12, 13]

(Write Enable Controlled with Output Enable $\overline{OE}$ active HIGH)
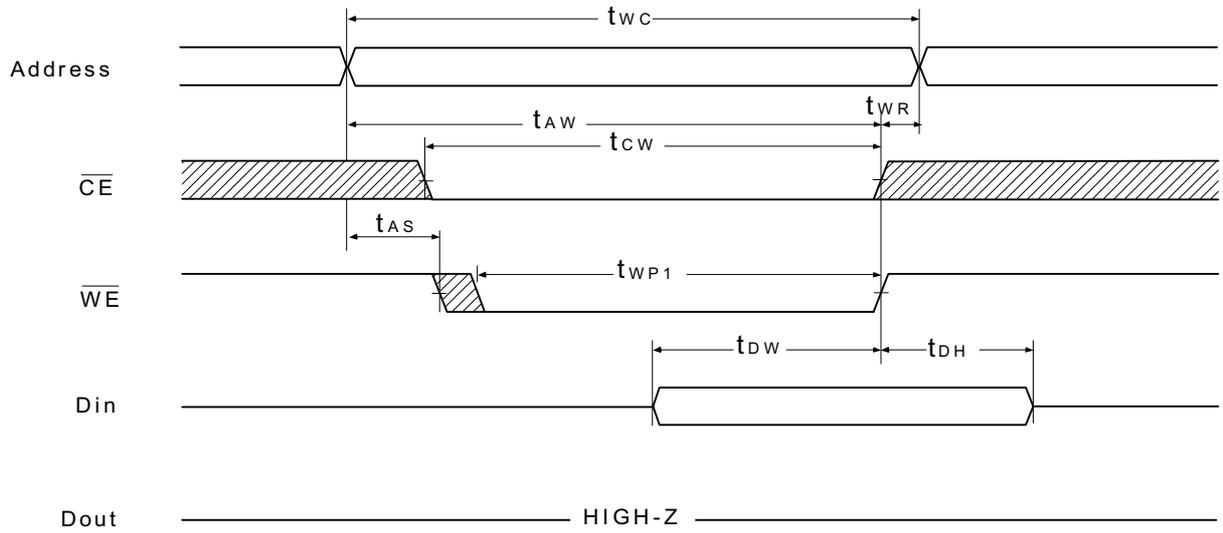
▨	DON'T CARE
▨	UNDEFINED

Timing Waveforms   (continued)

Write Cycle 3[12, 13]
(Chip Enable Controlled)
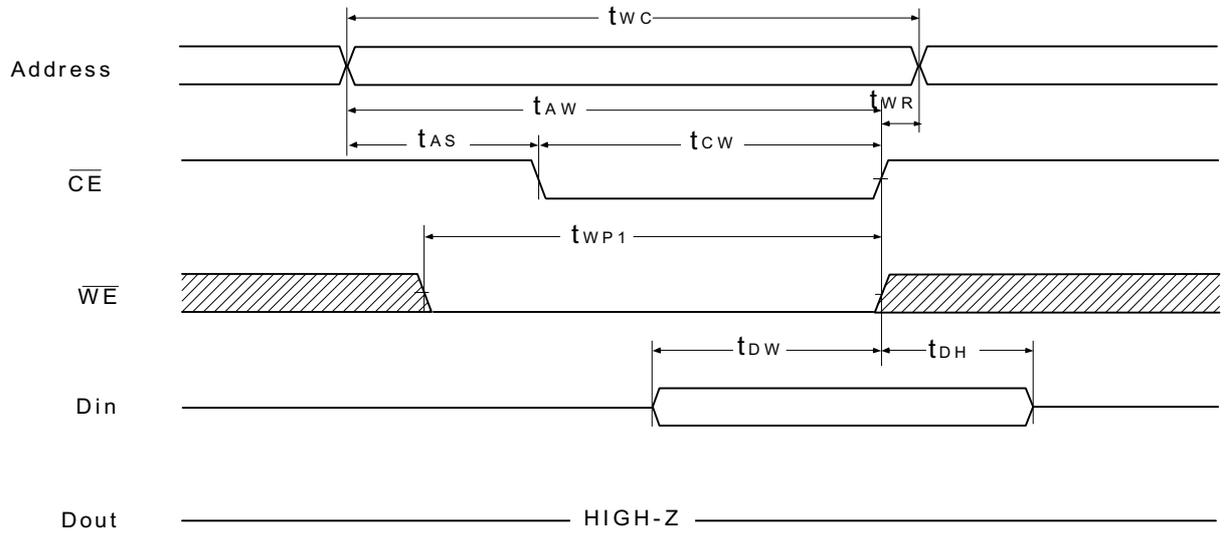
PACKING   DIMENSIONS

32-LEAD   SOJ CMOS SRAM (300mil)
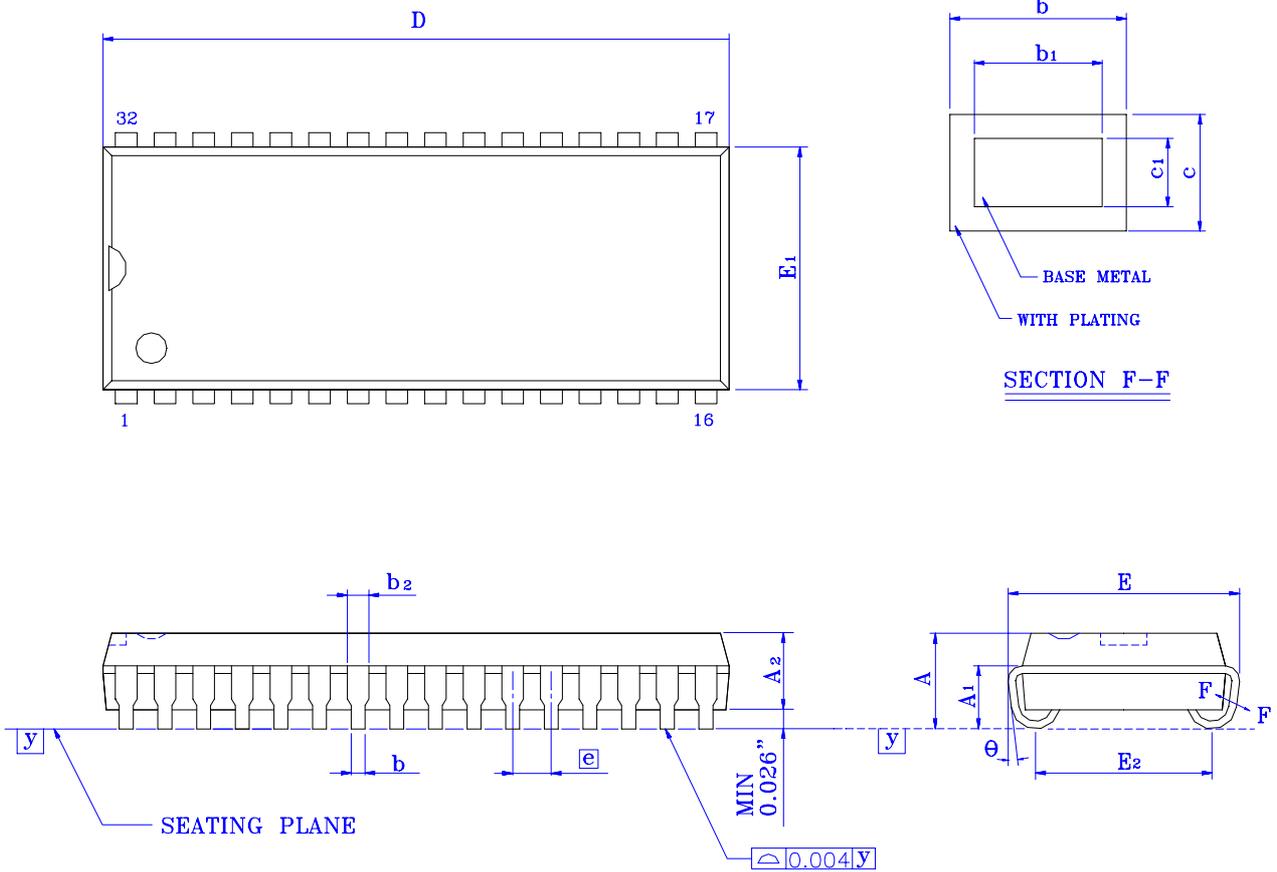
Symbol	Dimension in Inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	0.128	0.132	0.140	3.25	3.35	3.56
A$_1$	0.082	---------------	---------------	2.08	---------------	---------------
A$_2$	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b$_2$	0.026	0.028	0.032	0.66	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
E	0.330	0.335	0.340	8.39	8.51	8.63
E$_1$	0.295	0.300	0.305	7.49	7.62	7.75
E$_2$	0.260	0.267	0.274	6.61	6.78	6.96
e	---------------	0.050	---------------	---------------	1.27	---------------
y	---------------	---------------	0.004	---------------	---------------	0.10
θ	-5°	2°	6°	-5°	2°	6°

PACKING DIMENSIONS

32-LEAD TSOP(II) (400mil)
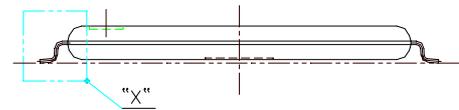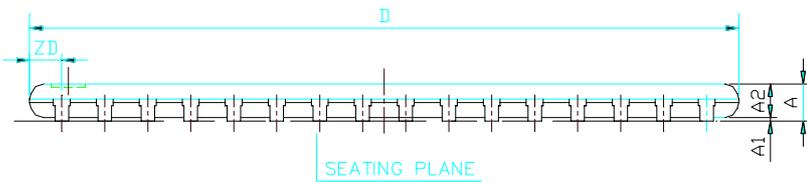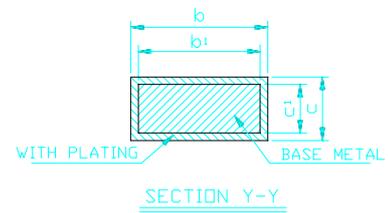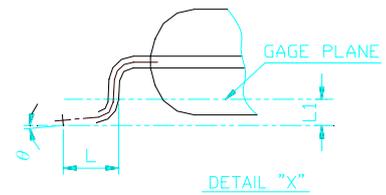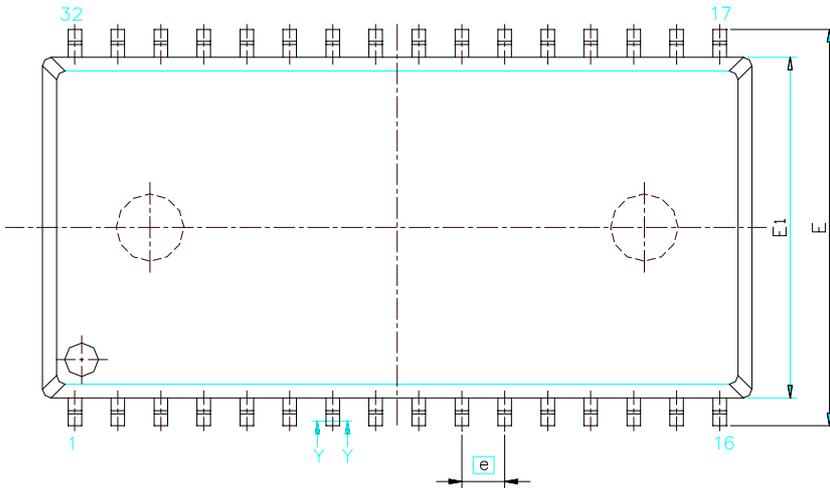
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	-	0.52	0.012	-	0.020
b1	0.30	0.40	0.45	0.012	0.016	0.018
c	0.12	-	0.21	0.005	-	0.008
c1	0.12	0.15	0.16	0.005		0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
ZD	0.95 REF			0.037 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 REF		
e	1.27 BASIC			0.050 BSC		
θ	0	-	5	0	-	5

Important Notice