

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

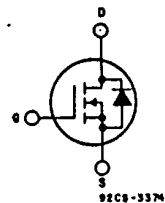
File Number 1514

N-Channel Logic Level Power Field-Effect Transistors (L² FET)

12 A, 80 V and 100 V
 $r_{DS(on)}$: 0.5 Ω

Features:

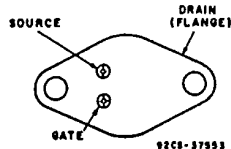
- Design optimized for 5 volt gate drive
- Can be driven directly from Q-MOS, N-MOS, TTL Circuits
- Compatible with automotive drive requirements
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device



N-CHANNEL ENHANCEMENT MODE

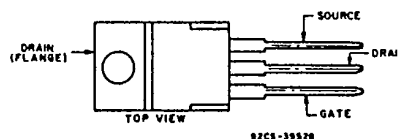
TERMINAL DESIGNATIONS

RFM8N18L
 RFM8N20L



JEDEC TO-204AA

RFP8N18L
 RFP8N20L



JEDEC TO-220AB

The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9534 and TA9535.

MAXIMUM RATINGS, Absolute-Maximum Values ($T_C=25^\circ\text{C}$):

	RFM8N18L	RFM8N20L		RFP8N18L	RFP8N20L	
DRAIN-SOURCE VOLTAGE	180	200		180	200	V
DRAIN-GATE VOLTAGE ($R_{GS}=1\text{ M}\Omega$)	180	200		180	200	V
GATE-SOURCE VOLTAGE			± 10			V
DRAIN CURRENT, RMS Continuous			8			A
Pulsed			20			A
POWER DISSIPATION @ $T_C=25^\circ\text{C}$	75	75		60	60	W
Derate above $T_C=25^\circ\text{C}$	0.6	0.6		0.48	0.48	W/ $^\circ\text{C}$
OPERATING AND STORAGE TEMPERATURE			-55 to +150			$^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C)=25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DS}	$I_D=1\text{ mA}$ $V_{GS}=0$	180	—	200	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ $I_D=1\text{ mA}$	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=145\text{ V}$ $V_{GS}=160\text{ V}$	—	1	—	—	μA
		$T_C=125^\circ\text{C}$ $V_{DS}=145\text{ V}$ $V_{GS}=160\text{ V}$	—	50	—	—	
			—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 10\text{ V}$ $V_{DS}=0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}^*$	$I_D=4\text{ A}$ $V_{GS}=5\text{ V}$	—	2.0	—	2.0	V
		$I_D=8\text{ A}$ $V_{GS}=5\text{ V}$	—	4.6	—	4.6	
Static Drain-Source On Resistance	$r_{DS(on)}^*$	$I_D=4\text{ A}$ $V_{GS}=5\text{ V}$	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}^*	$V_{DS}=10\text{ V}$ $I_D=4\text{ A}$	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	$V_{DS}=25\text{ V}$ $V_{GS}=0\text{ V}$	—	900	—	900	pF
Output Capacitance	C_{oss}	$f=1\text{ MHz}$	—	250	—	250	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	$V_{DD}=50\text{ V}$ $I_D=4\text{ A}$	15(typ)	45	15(typ)	45	ns
Rise Time	t_r	$R_{\theta JA}=\infty$	45(typ)	150	45(typ)	150	
Turn-Off Delay Time	$t_d(off)$	$R_{\theta JA}=6.25\text{ }^\circ\text{C/W}$ $V_{GS}=5\text{ V}$	100(typ)	135	100(typ)	135	
Fall Time	t_f		60(typ)	105	60(typ)	105	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	$^\circ\text{C/W}$
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	

*Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V _{SD}	I _{SD} =4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t _{rr}	I _F =4 A d _I /d _t =100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width $\leq 300\text{ } \mu\text{s}$, duty cycle $\leq 2\%$.

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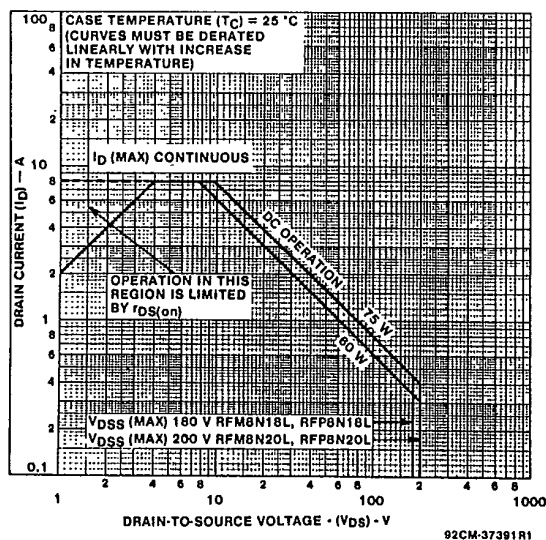


Fig. 1 — Maximum safe operating areas for all types.

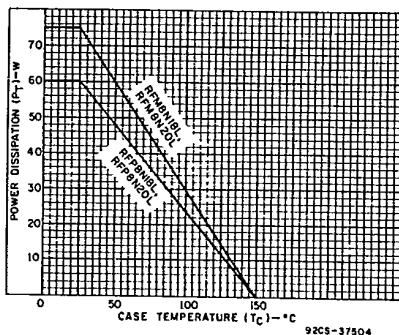


Fig. 2 — Power vs. temperature derating curve for all types.

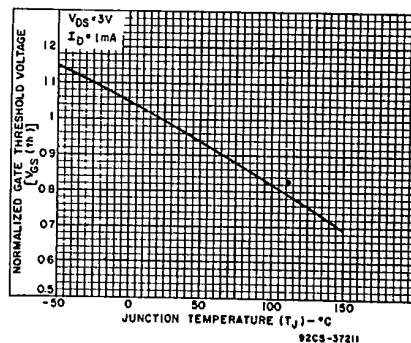


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

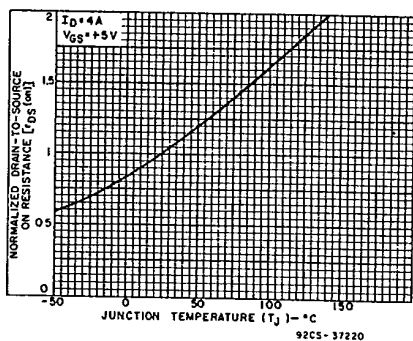


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

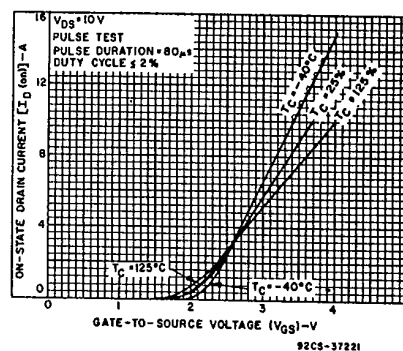


Fig. 5 — Typical transfer characteristics for all types.

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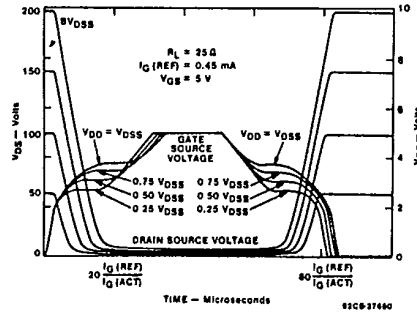


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

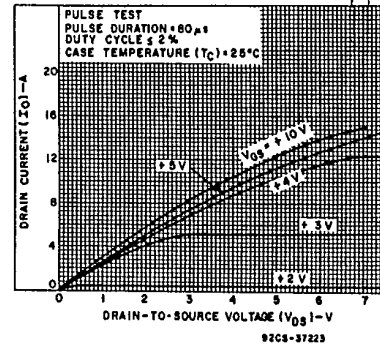


Fig. 7 - Typical saturation characteristics for all types.

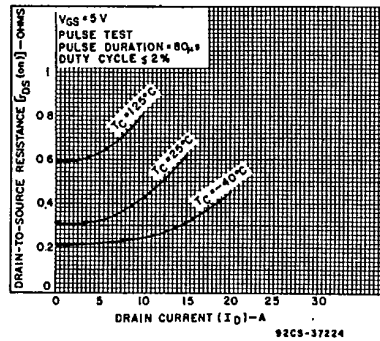


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

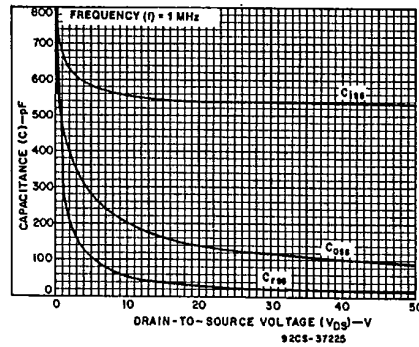


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

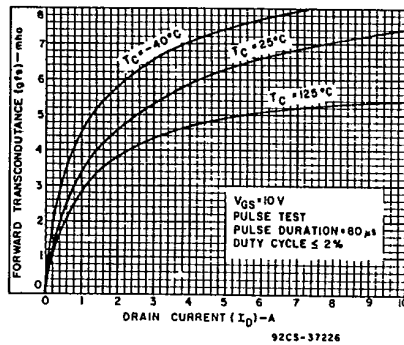


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

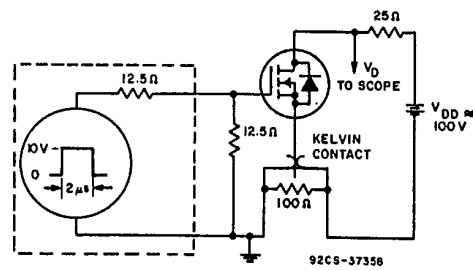


Fig. 11 - Switching Time Test Circuit.