

Key Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- automatic cable equalization
- multi-standard operation from 143Mb/s to 1.485Gb/s
- supports DVB-ASI at 270Mb/s
- manual bypass (useful for low data rates with slow rise/fall times)
- performance optimized for 270Mb/s and 1.485Gb/s
- typical maximum equalized length of Belden 1694A cable: 140m at 1.485Gb/s, 350m at 270Mb/s
- 50Ω differential output (with internal 50Ω pull-ups)
- Pb-free and RoHS Compliant

Key Specifications

- cable length indicator for SMPTE 259M inputs
- output mute based on max cable length adjust or manual override
- single 3.3V power supply operation
- operating temperature range: 0°C to +70°C

Applications

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces

Description

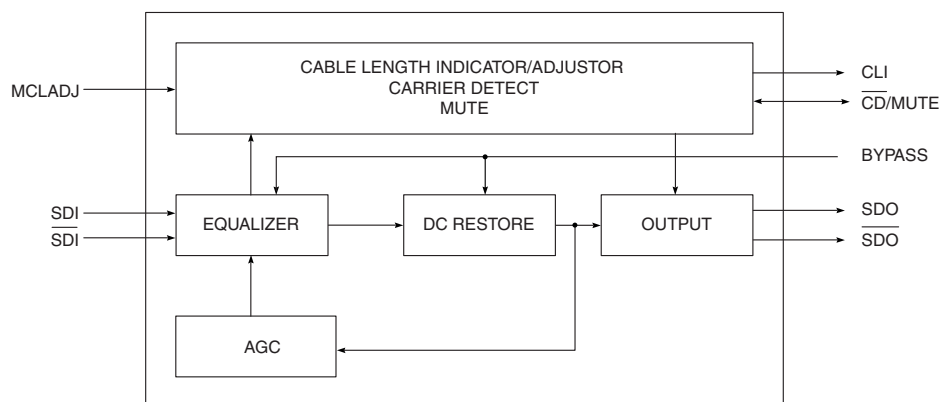
The GS1524 is a second-generation high-speed bipolar integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable at data rates from 143Mb/s up to 1.485Gb/s. The GS1524 is designed to support SMPTE 292M, SMPTE 344M and SMPTE 259M, and is optimized for performance at 270Mb/s and 1.485Gb/s.

The GS1524 features DC restoration to compensate for the DC content of SMPTE pathological test patterns. The GS1524 also incorporates a Cable Length Indicator (CLI) that provides an indication of the amount of cable being equalized for data rates up to 360Mb/s.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1524 output when an approximate selected cable length is reached for SMPTE 259M signals. This feature allows the GS1524 to distinguish between low amplitude SD-SDI signals and noise at the input of the device. The $\overline{\text{CD}}/\text{MUTE}$ pin provides an indication of the GS1524 mute status in addition to functioning as a mute control input. The SD outputs of the GS1524 may be forced to a mute state by applying a voltage to the $\overline{\text{CD}}/\text{MUTE}$ pin.

Power consumption is typically 265mW using a 3.3V power supply.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

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1. Electrical Characteristics

1.1 Absolute Maximum Ratings

| Parameter | Value |
|---------------------------------------|----------------------------------|
| Supply Voltage | -0.5V to +3.6V _{DC} |
| Input ESD Voltage | 500V |
| Storage Temperature Range | -50°C < T _s < 125°C |
| Input Voltage Range (any input) | -0.3 to (V _{CC} + 0.3)V |
| Operating Temperature Range | 0°C to 70°C |
| Power Dissipation | 300mW |
| Lead Temperature (soldering, 10 sec.) | 260°C |

1.2 DC Electrical Characteristics

Table 1-1: DC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

| Parameter | Conditions | Symbol | Min | Typ | Max | Units | Notes | Test Levels |
|----------------------------|----------------------|--------------------------|-------|--|-------|-------|-------|-------------|
| Supply Voltage | – | V _{CC} | 3.135 | 3.3 | 3.465 | V | ± 5% | 1 |
| Power Consumption | T _A =25°C | P _D | – | 265 | – | mW | – | 5 |
| Supply Current | T _A =25°C | I _S | – | 80 | – | mA | – | 1 |
| Output Common Mode Voltage | T _A =25°C | V _{CMOUT} | – | V _{CC} - ΔV _{SDO} /2 | – | V | – | 7 |
| Input Common Mode Voltage | T _A =25°C | V _{CMIN} | – | 1.75 | – | V | – | 10 |
| CLI DC Voltage (0m) | T _A =25°C | – | – | 2.5 | – | V | – | 1 |
| CLI DC Voltage (no signal) | T _A =25°C | – | – | 1.9 | – | V | – | 7 |
| Floating MCLADJ DC Voltage | T _A =25°C | – | – | 1.3 | – | V | – | 7 |
| MCLADJ Range | T _A =25°C | – | – | 0.69 | – | V | – | 7 |
| CD/Mute Output Voltage | Carrier not present | V _{CD/Mute(OH)} | 2.6 | – | – | V | – | 1 |
| | Carrier present | V _{CD/Mute(OL)} | – | – | 1.2 | – | – | 1 |

Table 1-1: DC Electrical Characteristics

$V_{DD} = 3.3V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, unless otherwise shown

| Parameter | Conditions | Symbol | Min | Typ | Max | Units | Notes | Test Levels |
|---|-----------------|--------------------------|-----|-----|-----|-------|-------|-------------|
| \overline{CD} /Mute Input Voltage Required to Force Outputs to Mute | Min to Mute | $V_{\overline{CD}/Mute}$ | 3.0 | – | – | V | – | 7 |
| \overline{CD} /Mute Input Voltage Required to Force Active | Max to Activate | $V_{\overline{CD}/Mute}$ | – | – | 2.0 | V | – | 7 |

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.
10. Wafer Probe

1.3 AC Electrical Characteristics

Table 1-2: AC Electrical Characteristics

$V_{DD} = 3.3V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, unless otherwise shown

| Parameter | Conditions | Symbol | Min | Typ | Max | Units | Notes | Test Levels |
|--------------------------------|--|------------------|-----|-----|------|-------------------|------------------------|-------------|
| Serial input data rate | – | – | 143 | – | 1485 | Mb/s | – | 6 |
| Input Voltage Swing | $T_A = 25^{\circ}C$, differential | ΔV_{SDI} | 720 | 800 | 950 | mV _{p-p} | 0m cable length | 1 |
| Output Voltage Swing | 50 Ω load, $T_A = 25^{\circ}C$, differential | ΔV_{SDO} | – | 750 | – | mV _{p-p} | – | 1 |
| Maximum equalized cable length | 270Mb/s, Belden 1694A, 0.2UI output jitter | – | – | 350 | – | m | Equalizer Pathological | 7 |
| | 270Mb/s, Belden 8281 0.2UI output jitter | – | – | 280 | – | m | Equalizer Pathological | 1 |
| | 1.485Gb/s, Belden 1694A 0.25UI output jitter | – | – | 140 | – | m | Equalizer Pathological | 7 |
| | 1.485Gb/s, Belden 8281 0.25UI output jitter | – | – | 100 | – | m | Equalizer Pathological | 1 |
| Output Rise/Fall time | 20% - 80% | – | – | 80 | 220 | ps | – | 1 |
| Mismatch in rise/fall time | | – | – | – | 30 | ps | – | 1 |

Table 1-2: AC Electrical Characteristics

$V_{DD} = 3.3V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, unless otherwise shown

| Parameter | Conditions | Symbol | Min | Typ | Max | Units | Notes | Test Levels |
|-----------------------|--------------|--------|-----|------|-----|------------|-------|-------------|
| Duty cycle distortion | – | – | – | – | 30 | ps | – | 1 |
| Overshoot | – | – | – | – | 10 | % | – | 1 |
| Input Return Loss | – | – | 15 | – | – | dB | 1 | 7 |
| Input Resistance | single ended | – | – | 1.64 | – | k Ω | – | 6 |
| Input Capacitance | single ended | – | – | 1 | – | pF | – | 6 |
| Output Resistance | single ended | – | – | 50 | – | Ω | – | 6 |

TEST LEVELS:

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES:

1. 1. Tested on CB1524 board from 5MHz to 2GHz.

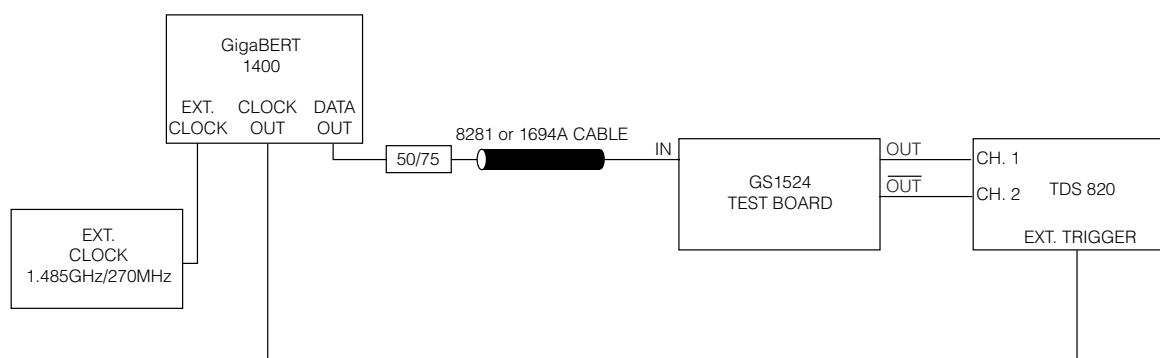


Figure 1-1: Test Circuit

2. Pin Out

2.1 Pin Connections

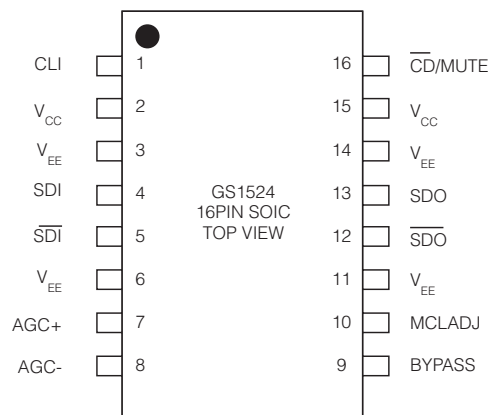


Figure 2-1: 16 PIN SOIC

2.2 Pin Descriptions

Table 2-1: Pin Descriptions

| Pin Number | Name | Type | Description |
|------------|------------|---------------|--|
| 1 | CLI | ANALOG OUTPUT | CABLE LENGTH INDICATOR. An analog voltage proportional to the cable length connected to the Serial digital input. Note: CLI is recommended for data rates up to 360Mb/s only. |
| 4,5 | SDI, SDI | INPUT | Serial digital differential input. |
| 7,8 | AGC+, AGC- | PASSIVE INPUT | External AGC capacitor. Should be set to 1μF |
| 9 | BYPASS | LOGIC INPUT | Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode. |
| 10 | MCLADJ | ANALOG INPUT | MAXIMUM CABLE LENGTH ADJUST. Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. Note: MCLADJ is recommended for data rates up to 360Mb/s |
| 12, 13 | SDO, SDO | PECL OUTPUT | Equalized serial digital differential output. |

Table 2-1: Pin Descriptions

| | | | |
|--------------|------------------------------------|---------------|---|
| 16 | $\overline{\text{CD}}/\text{MUTE}$ | BIDIRECTIONAL | <p>MUTE INDICATOR-CONTROL/ CARRIER DETECT.</p> <p>OUTPUT: the output voltage drops to below 1.2V when the carrier is present and the data outputs are active.</p> <p>INPUT: if the $\overline{\text{CD}}/\text{MUTE}$ pin is tied to ground, the data output will never mute and the MCLADJ setting is overwritten. If the $\overline{\text{CD}}/\text{MUTE}$ pin is tied to VCC, the data outputs will always mute and the MCLADJ setting is overwritten.</p> <p>Note: $\overline{\text{CD}}/\text{MUTE}$ is not functional in BYPASS mode.</p> |
| 3, 6, 11, 14 | V_{EE} | POWER | Most negative power supply connection. Connect to ground. |
| 2, 15 | V_{CC} | POWER | Most positive power supply connection. Connect to +3.3V. |

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

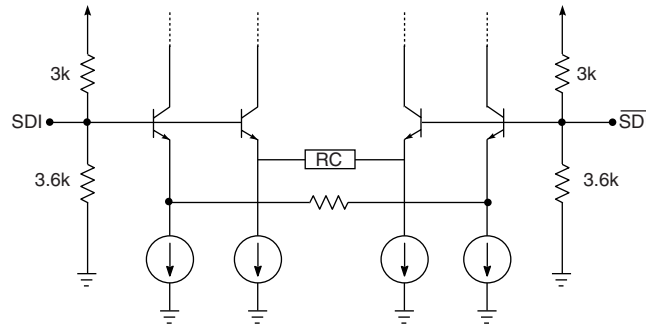


Figure 3-1: Input Equivalent Circuit

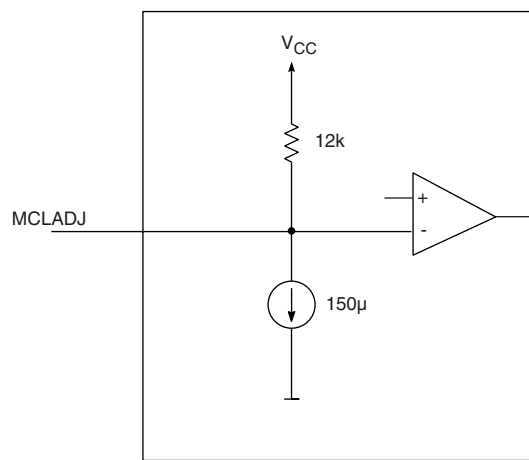


Figure 3-2: MCLADJ Equivalent Circuit

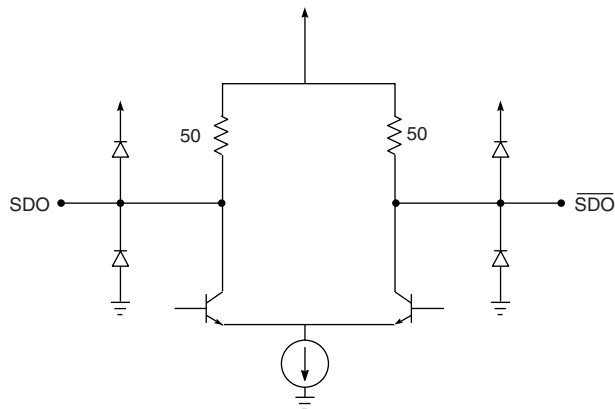


Figure 3-3: Output Circuit

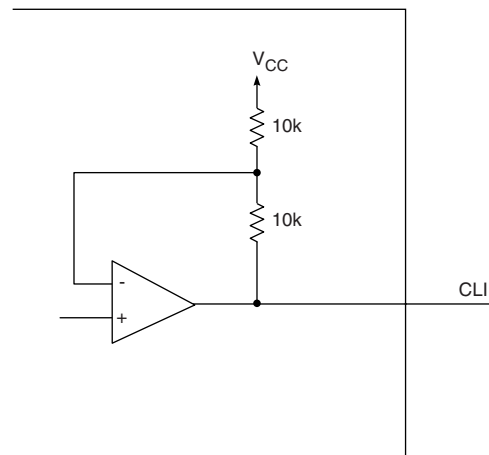


Figure 3-4: CLI Output Circuit

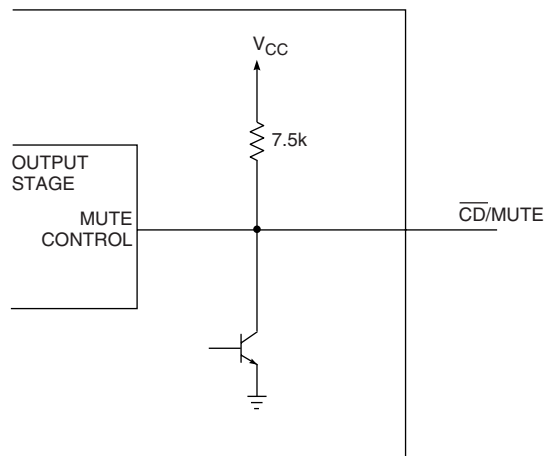


Figure 3-5: $\overline{\text{CD}}$ /Mute Circuit

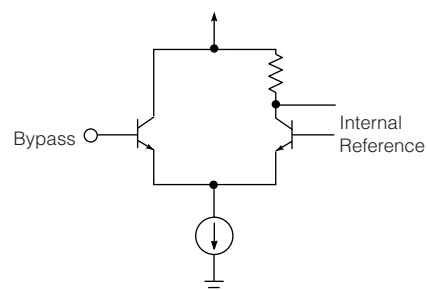


Figure 3-6: Bypass Circuit

4. Typical Performance Curves

(unless otherwise shown, $V_{CC} = 3.3V$, $T_A = 25^\circ C$)

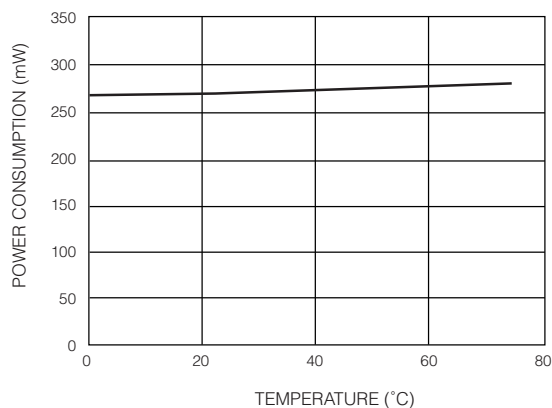


Figure 4-1: Power Consumption

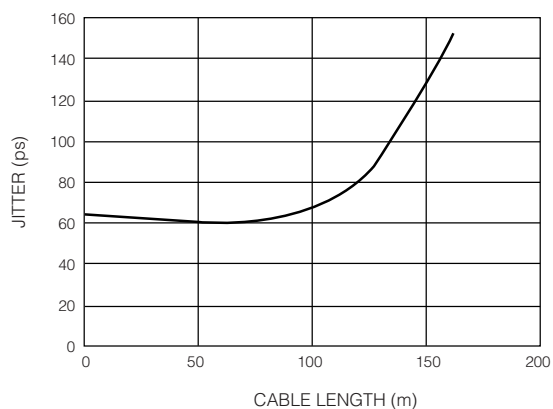


Figure 4-2: Typical Peak to Peak Jitter, PRN 2²³-1, Belden 1694A, 1.485 Gb/s

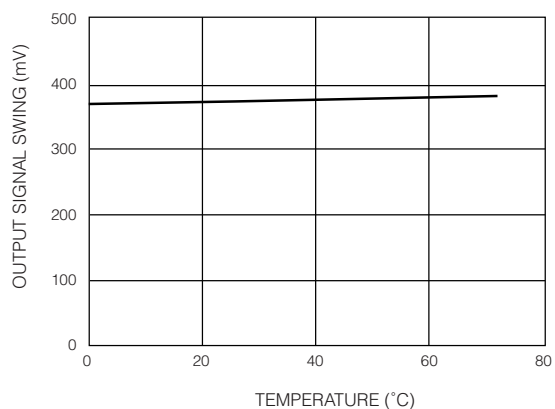


Figure 4-3: Output Signal Swing, p-p, Single Ended

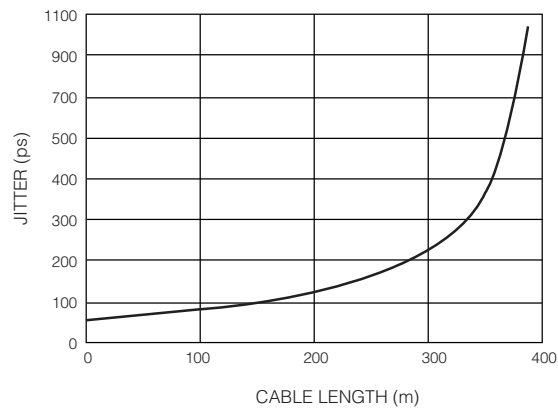


Figure 4-4: Typical Peak to Peak Jitter, PRN 223-1, Belden 1694A, 270Mb/s

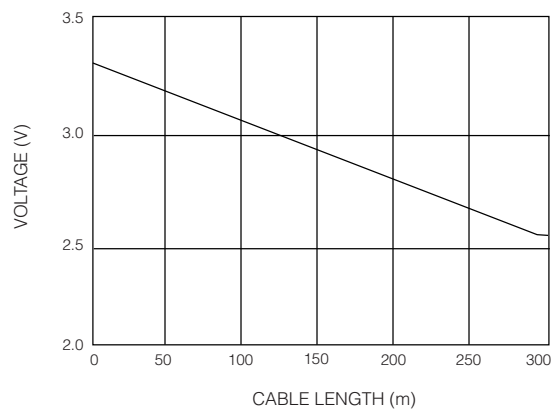


Figure 4-5: MCLADJ Input Voltage vs 1694A Cable Length, 270Mb/s

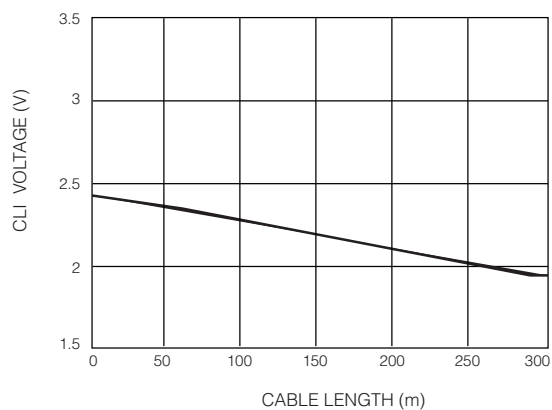


Figure 4-6: CLI Voltage vs. Belden 8281 Cable Length, 270Mb/s

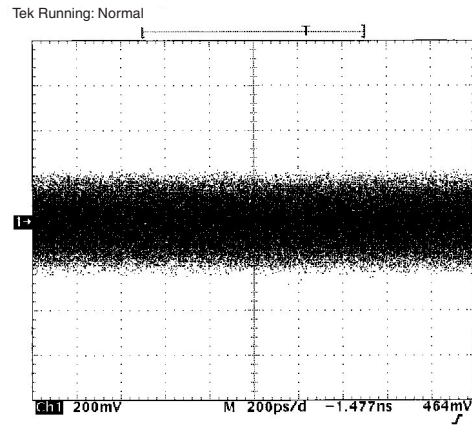


Figure 4-7: Input 100m (Belden 8281), 1.485Gb/s

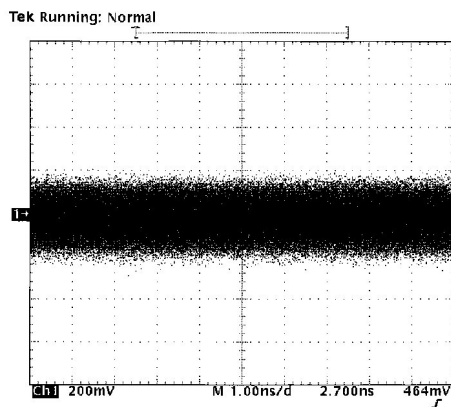


Figure 4-8: Input 280m (Belden 8281), 270Mb/s

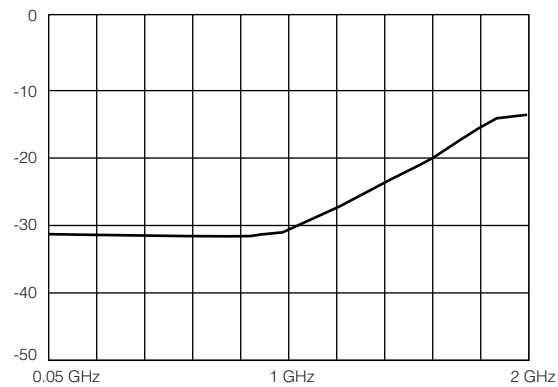


Figure 4-9: Input Return Loss using CB1524 Board

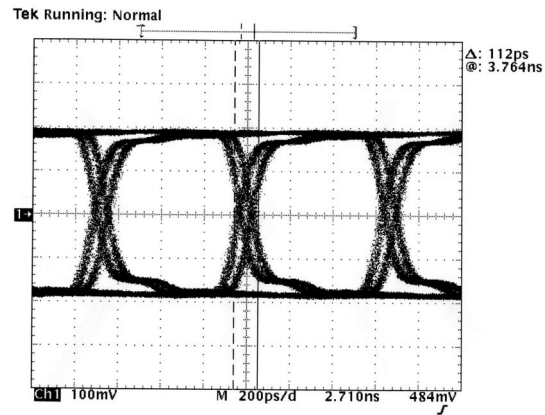


Figure 4-10: Fig. 17 Output 100m (Belden 8281), 1.485Gb/s

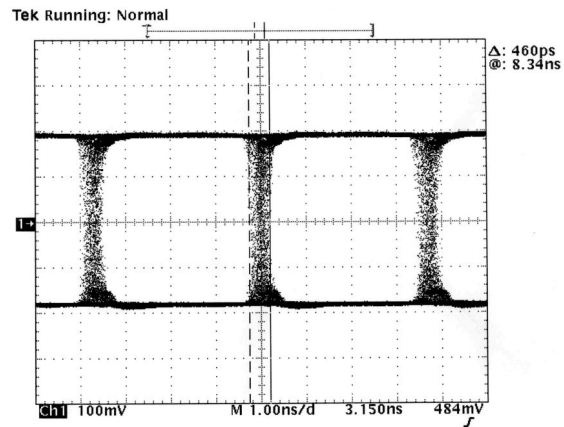


Figure 4-11: Output 280m (Belden 8281), 270Mb/s

5. Detailed Description

The GS1524 is a high speed bipolar IC designed to equalize both HD and SD serial digital signals. The device can typically equalize greater than 140 meters of Belden 1694A cable at 1.485Gb/s and 350m at 270Mb/s. Powered from a single +3.3V or -3.3V power supply, the device consumes approximately 265mW of power.

The serial data signal may be connected to the input pins ($\overline{\text{SDI}}$ / $\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the $\overline{\text{SDI}}$ and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV_{pp} differential, or 375mV_{pp} single ended when terminated with 50Ω as shown in [Figure 5-1](#).

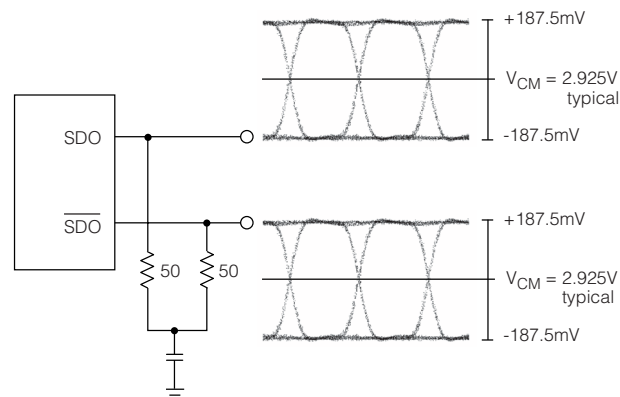


Figure 5-1: Typical Output Voltage Levels

6. Cable Length Indication/Carrier Detect/Mute

For SMPTE 259M inputs the GS1524 incorporates an analog cable length indicator (CLI) output and a programmable threshold output mute (MCLADJ). In addition, a multi-function $\overline{\text{CD}}$ /MUTE pin allows control of the GS1524 MUTE functionality for both SD and HD inputs.

The voltage output of CLI pin is an approximation of the amount of cable present at the GS1524 input for data rates up to 360Mb/s. The CLI voltage versus cable length (signal strength) is shown in [Figure 4-6](#). With 0m of cable, 800mV input signal levels and at 270Mb/s, the CLI output voltage is approximately 2.5V. As the cable length increases, the CLI voltage decreases providing an approximate correlation between the CLI voltage and cable length.

In applications where there are multiple input channels using the GS1524, it is advantageous to have a programmable mute output to avoid signal crosstalk.

The output of the GS1524 can be muted when the input signal decreases below a selectable input level. The voltage applied to the MCLADJ pin vs input cable length is shown in [Figure 4-5](#). For consistent accurate results this may need to be calibrated for each device. The MCLADJ pin may be left unconnected for applications where output muting is not required. This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

Note: MCLADJ and CLI are only recommended for data rates up to 360Mb/s.

The $\overline{\text{CD}}$ /Mute pin is a multi-function bidirectional pin that provides the following functions:

Applying a HIGH INPUT to the $\overline{\text{CD}}$ /Mute pin forces the GS1524 outputs to a muted condition. See the [Table 1-1: DC Electrical Characteristics](#) for voltage levels. In this condition the outputs will be latched to the last logic level present at the output to avoid signal crosstalk.

Applying a LOW INPUT to the $\overline{\text{CD}}$ /Mute pin will force the GS1524 outputs to remain active regardless of the length of input cable and the voltage applied to the MCLADJ pin. See the [Table 1-1: DC Electrical Characteristics](#) for voltage levels.

When used as an OUTPUT, the $\overline{\text{CD}}$ /Mute pin will provide an indication of the output mute status. The $\overline{\text{CD}}$ /Mute voltage will fall to below 1.2V when the carrier is present and the data outputs are active.

Note: The $\overline{\text{CD}}$ /Mute pin is not functional in BYPASS mode.

7. Application Information

7.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

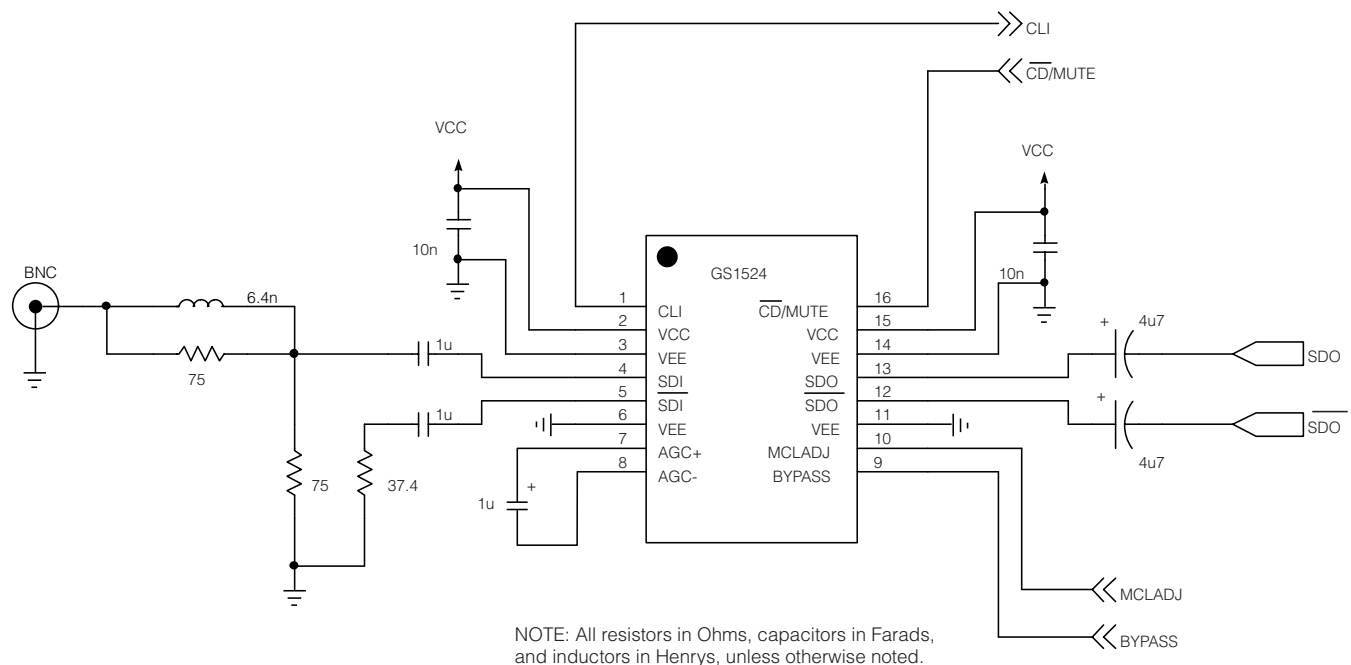
PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.

The PCB ground plane is removed under the GS1524 input components to minimize parasitic capacitance.

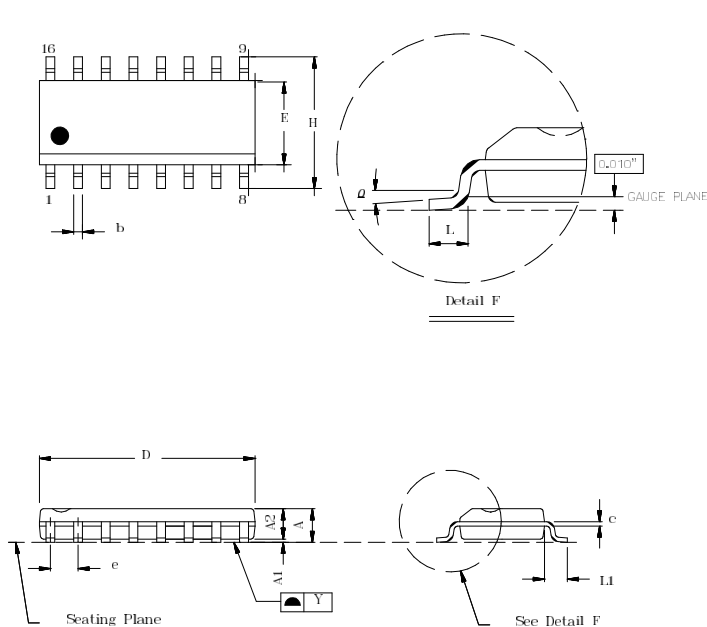
The PCB ground plane is removed under the GS1524 output components to minimize parasitic capacitance.

High speed traces are curved to minimize impedance changes.

7.2 Typical Application Circuit



8. Package dimensions



* CONTROLLING DIMENSION: MM

| Symbol | MILLIMETER | | | INCH | | |
|--------|------------|------|-------|-------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.35 | 1.63 | 1.75 | 0.053 | 0.064 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| A2 | 1.30 | 1.40 | 1.50 | 0.051 | 0.055 | 0.059 |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| c | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D | 9.80 | 9.91 | 10.01 | 0.386 | 0.390 | 0.394 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| e | | 1.27 | | | 0.50 | |
| H | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| L | 0.40 | 0.64 | 1.27 | 0.016 | 0.025 | 0.050 |
| L1 | | 1.07 | | | 0.042 | |
| Y | | | 0.10 | | | 0.004 |
| Ø | 0° | | 8° | 0° | | 8° |

Figure 8-1: 16 PIN SOIC

8.1 Ordering Information

| Part Number | Package | Temperature | Pb-Free and RoHS Compliant |
|--------------|------------------|-------------|----------------------------|
| GS1524-CKD | 16 pin SOIC | 0°C to 70°C | No |
| GS1524-CTD | 16 pin SOIC Tape | 0°C to 70°C | No |
| GS1524-CKDE3 | 16 pin SOIC | 0°C to 70°C | Yes |
| GS1524-CTDE3 | 16 pin SOIC Tape | 0°C to 70°C | Yes |

9. Revision History

| Version | ECR | Date | Changes and / or Modifications |
|---------|--------|------------|---|
| 6 | 136565 | April 2005 | Updated 'Green' references to RoHS Compliant. |
| 7 | 137165 | June 2005 | Rephrased RoHS compliance statement. |

CAUTION

ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

**DOCUMENT IDENTIFICATION****DATA SHEET**

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

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