

Description

The GMM7738280CTG is an 8M x 72 bits Dynamic RAM MODULE which is assembled 9 pieces of 8M x 8bit DRAMs in 32 pin TSOP II package and two 16bit driver ICs in 48pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors.

The GMM7738280CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM7738280CTG provides common data inputs and Extended Data Outputs.

Features

- * 168 pins Dual In-Line Package
- GMM7738280CTG : Gold plating
- * Extended Data Output (EDO) Mode Capability
- * Single Power Supply
- * Fast Access Time & Cycle Time

(Unit: ns)

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
GMM7738280CTG -5	50	18	84	20
GMM7738280CTG -6	60	20	104	25

- * Low Power

Active : 4770/4446mW (MAX)

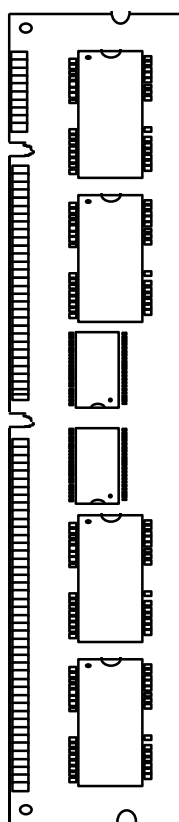
Standby : 89mW (CMOS level : MAX)

- * RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability

- * All inputs and outputs TTL Compatible

- * 4096 Refresh Cycles/64ms

GMM7738280CTG (Double Side)

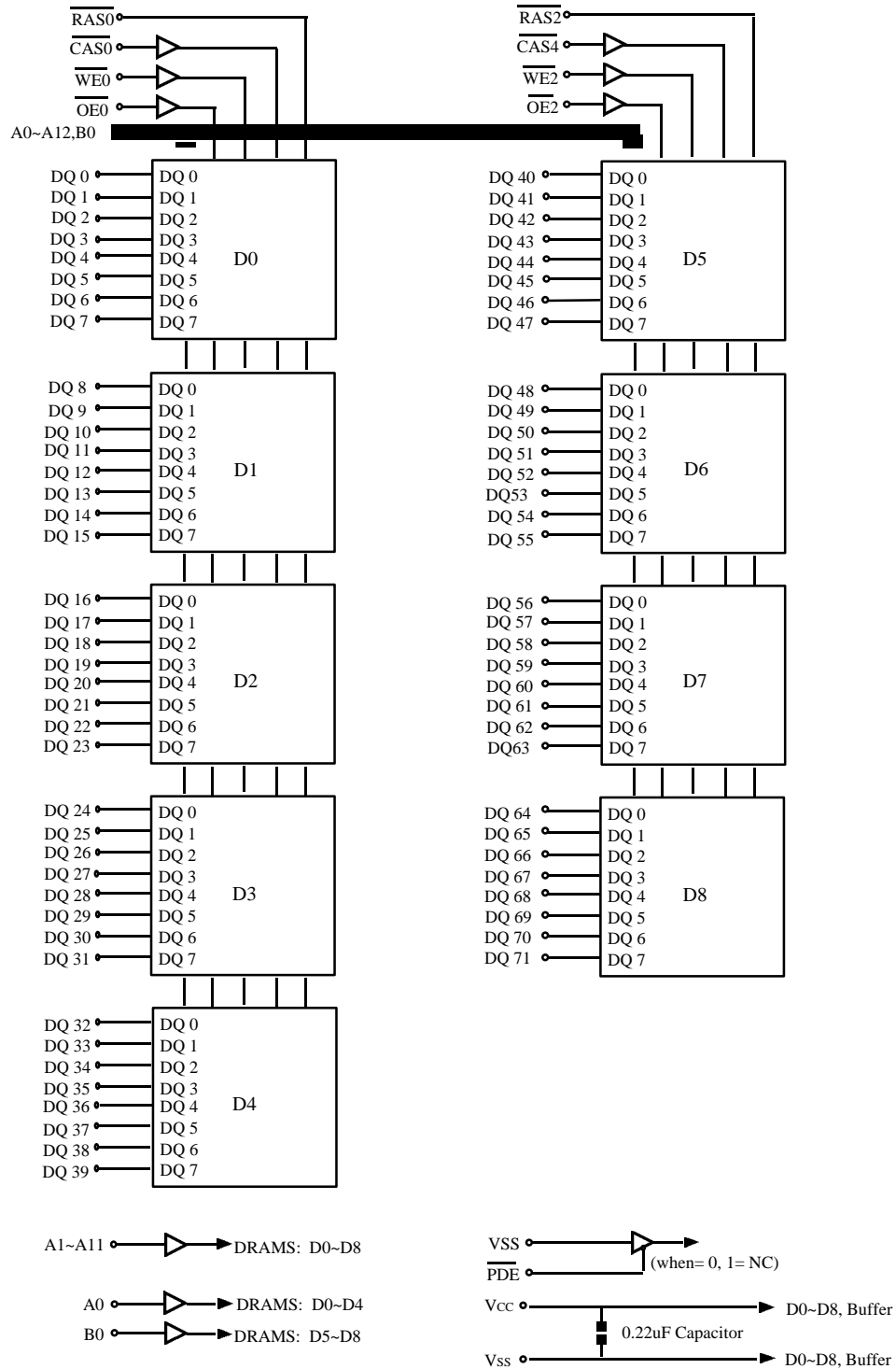


Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	29	RSVD	57	DQ ₂₂	85	V _{SS}	113	RSVD	141	DQ ₅₈
2	DQ ₀	30	/RAS ₀	58	DQ ₂₃	86	DQ ₃₆	114	/RAS ₁ *	142	DQ ₅₉
3	DQ ₁	31	/OE ₀	59	V _{CC}	87	DQ ₃₇	115	RFU	143	V _{CC}
4	DQ ₂	32	V _{SS}	60	DQ ₂₄	88	DQ ₃₈	116	V _{SS}	144	DQ ₆₀
5	DQ ₃	33	A ₀	61	RFU	89	DQ ₃₉	117	A ₁	145	RFU
6	V _{CC}	34	A ₂	62	RFU	90	V _{CC}	118	A ₃	146	RFU
7	DQ ₄	35	A ₄	63	RFU	91	DQ ₄₀	119	A ₅	147	RFU
8	DQ ₅	36	A ₆	64	RFU	92	DQ ₄₁	120	A ₇	148	RFU
9	DQ ₆	37	A ₈	65	DQ ₂₅	93	DQ ₄₂	121	A ₉	149	DQ ₆₁
10	DQ ₇	38	A ₁₀	66	DQ ₂₆	94	DQ ₄₃	122	A ₁₁	150	DQ ₆₂
11	DQ ₈	39	RSVD	67	DQ ₂₇	95	DQ ₄₄	123	A ₁₃ *	151	DQ ₆₃
12	V _{SS}	40	V _{CC}	68	V _{SS}	96	V _{SS}	124	V _{CC}	152	V _{SS}
13	DQ ₉	41	RFU	69	DQ ₂₈	97	DQ ₄₅	125	RFU	153	DQ ₆₄
14	DQ ₁₀	42	RFU	70	DQ ₂₉	98	DQ ₄₆	126	B ₀	154	DQ ₆₅
15	DQ ₁₁	43	V _{SS}	71	DQ ₃₀	99	DQ ₄₇	127	V _{SS}	155	DQ ₆₆
16	DQ ₁₂	44	/OE ₂	72	DQ ₃₁	100	DQ ₄₈	128	RFU	156	DQ ₆₇
17	DQ ₁₃	45	/RAS ₂	73	V _{CC}	101	DQ ₄₉	129	/RAS ₃ *	157	V _{CC}
18	V _{CC}	46	/CAS ₄	74	DQ ₃₂	102	V _{CC}	130	/CAS ₅ *	158	DQ ₆₈
19	DQ ₁₄	47	RSVD	75	DQ ₃₃	103	DQ ₅₀	131	RSVD	159	DQ ₆₉
20	DQ ₁₅	48	/WE ₂	76	DQ ₃₄	104	DQ ₅₁	132	/PDE	160	DQ ₇₀
21	DQ ₁₆	49	V _{CC}	77	DQ ₃₅	105	DQ ₅₂	133	V _{CC}	161	DQ ₇₁
22	DQ ₁₇	50	RSVD	78	V _{SS}	106	DQ ₅₃	134	RSVD	162	V _{SS}
23	V _{SS}	51	RSVD	79	PD ₁	107	V _{SS}	135	RSVD	163	PD ₂
24	RSVD	52	DQ ₁₈	80	PD ₃	108	RSVD	136	DQ ₅₄	164	PD ₄
25	RSVD	53	DQ ₁₉	81	PD ₅	109	RSVD	137	DQ ₅₅	165	PD ₆
26	V _{CC}	54	V _{SS}	82	PD ₇	110	V _{CC}	138	V _{SS}	166	PD ₈
27	/WE ₀	55	DQ ₂₀	83	ID ₀	111	RFU	139	DQ ₅₆	167	ID ₁
28	/CAS ₀	56	DQ ₂₁	84	V _{CC}	112	/CAS ₁ *	140	DQ ₅₇	168	V _{CC}

Note : Pins Marked * are not used in this module.

Block Diagram



Pin Description

Pin	Function	Pin	Function
A0-A11, B0	Address Inputs	$\overline{\text{PDE}}$	Presence Detect Enable
DQ0-DQ71	Data Input/Output	V _{CC}	Power (+3.3V)
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe	V _{SS}	Ground
$\overline{\text{CAS0}}, \overline{\text{CAS4}}$	Column Address Strobe	NC	No Connection
$\overline{\text{WE0}}, \overline{\text{WE2}}$	Read/Write Enable	$\overline{\text{OE0}}, \overline{\text{OE2}}$	Output Enable
PD 1 - 8	Presence Detect	RSVD	Reserved Use
ID 0-1	ID bit	RFU	Reserved for Future Use

Presence Detect Pins (Optional)

Pin	50ns	60ns
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

* 0 : V_{SS}
1 : NC or V_{CC}

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	C
T _{STG}	Storage Temperature (Plastic)	-55 ~ 125	C
V _{IN} /V _{OUT}	Voltage on any Pin Relative to V _{SS}	-0.5 ~ 4.6	V
V _{CC}	Voltage on V _{CC} Pin Relative to V _{SS}	-0.5 ~ 4.6	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	12	W

*Note: 1. Stress greater than above Absolute Maximum Ratings may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A = 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V _{IH}	Input High Voltage	2.0	-	V _{CC} +0.3	V	1
V _{IL}	Input Low Voltage	-0.3	-	0.8	V	1

*Note: 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics: ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter		GMM7738280CTG		Unit	Note
			Min	Max		
V_{OH}	Output Level Output ``H`` Level Voltage ($I_{OUT} = -2\text{ }\mu\text{A}$)		2.4	V_{CC}	V	
V_{OL}	Output Level Output ``L`` Level Voltage ($I_{OUT} = 2\text{ }\mu\text{A}$)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = t_{RC \text{ min}}$)	50ns	-	1325	μA	1,2
		60ns	-	1235		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (\overline{RAS} , $\overline{CAS} = V_{IH}$, $D_{OUT} = \text{High-Z}$)		-	38	μA	
I_{CC3}	\overline{RAS} -Only Refresh Current Average Power Supply Current \overline{RAS} -Only Refresh Mode (\overline{RAS} Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC \text{ min}}$)	50ns	-	1325	μA	2
		60ns	-	1235		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current Extended Data Out Mode ($\overline{RAS} = V_{IL}$, \overline{CAS} , Address Cycling: $t_{RC} = t_{RC \text{ min}}$)	50ns	-	1010	μA	1,3
		60ns	-	920		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (\overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2V$, $D_{OUT} = \text{High-Z}$)		-	24.5	μA	
I_{CC6}	\overline{CAS} -before- \overline{RAS} Refresh Current ($t_{RC} = t_{RC \text{ min}}$)	50ns	-	1325	μA	
		60ns	-	1235		
I_{CC7}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$		-	65	μA	1
$I_{I(L)}$	Input Leakage Current, Any Input ($0V \leq V_{IN} \leq V_{CC}$)		-5	5	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq V_{CC}$)		-5	5	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(\text{max})}$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$, $f = 1MHz$)

Symbol	Parameter	Min	Max	Unit	Note
C _{I1}	Input Capacitance (A0~A12,B0)	-	20	pF	1
C _{I2}	Input Capacitance ($\overline{WE}0, \overline{WE}2, \overline{OE}0, \overline{OE}2$)	-	20	pF	1, 2
C _{I3}	Input Capacitance ($\overline{RAS}0, \overline{RAS}2$)	-	45	pF	1, 2
C _{I4}	Input Capacitance ($\overline{CAS}0, \overline{CAS}4$)	-	20	pF	1, 2
C _{I/O}	I/O Capacitance (DQ0~DQ71)	-	20	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable DOUT.

AC Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim 70^\circ C$, Notes 1, 2, 19)

Test Conditions

Input rise and fall times : 2ns

Output timing reference levels : $V_{OL}/V_{OH} = 0.8/2.0V$

Input level : $V_{IL}/V_{IH} = 0.0/3.0V$

Output load : 1 TTL gate+C_L (100pF)

Input timing reference levels : $V_{IL}/V_{IH} = 0.8/2.0V$

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	84	-	104	-	§ Å	
t _{RP}	\overline{RAS} Precharge Time	30	-	40	-	§ Å	
t _{CP}	\overline{CAS} Precharge Time	8	-	10	-	§ Å	
t _{RAS}	\overline{RAS} Pulse Width	50	10000	60	10000	§ Å	
t _{CAS}	\overline{CAS} Pulse Width	8	10000	10	10000	§ Å	
t _{ASR}	Row Address Set-up Time	5	-	5	-	§ Å	
t _{RAH}	Row Address Hold Time	8	-	10	-	§ Å	
t _{ASC}	Column Address Set-up Time	0	-	0	-	§ Å	
t _{CAH}	Column Address Hold Time	8	-	10	-	§ Å	
t _{RCD}	\overline{RAS} to \overline{CAS} Delay Time	12	32	14	40	§ Å	3
t _{RAD}	\overline{RAS} to Column Address Delay Time	10	20	12	25	§ Å	4
t _{RSH}	\overline{RAS} Hold Time	18	-	20	-	§ Å	
t _{CSH}	\overline{CAS} Hold Time	35	-	40	-	§ Å	
t _{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	10	-	10	-	§ Å	
t _{ODD}	\overline{OE} to D _{IN} Delay Time	18	-	20	-	§ Å	5
t _{DZO}	\overline{OE} Delay Time from D _{IN}	0	-	0	-	§ Å	6
t _{DZC}	\overline{CAS} Set-up Time from D _{IN}	0	-	0	-	§ Å	6
t _t	Transition Time (Rise and Fall)	2	50	2	50	§ Å	7
t _{REF}	Refresh Period (4096 Cycles)	-	64	-	64	ms	

Read Cycles

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from \overline{RAS}	-	50	-	60	ns	8,9
t_{CAC}	Access Time from \overline{CAS}	-	18	-	20	ns	9,10,17
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,11,17
t_{OAC}	Access Time from \overline{OE}	-	18	-	20	ns	9
t_{RCS}	Read Command Set-up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to \overline{CAS}	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time to \overline{RAS}	0	-	0	-	ns	12
t_{RAL}	Column Address to \overline{RAS} Lead Time	30	-	35	-	ns	
t_{CAL}	Column Address to \overline{CAS} Lead Time	15	-	18	-	ns	
t_{OFF}	Output Buffer Turn-off Delay Time from \overline{CAS}	-	18	-	20	ns	13,21
t_{OEZ}	Output Buffer Turn-off Delay Time from \overline{OE}	-	18	-	20	ns	13
t_{CDD}	\overline{CAS} to D_{IN} Delay Time	18	-	20	-	ns	5
t_{RDD}	\overline{RAS} to D_{IN} Delay Time	13	-	15	-	ns	
t_{WDD}	\overline{WE} to D_{IN} Delay Time	13	-	15	-	ns	
t_{OFR}	Output Buffer Turn-off Delay Time from \overline{RAS}	-	13	-	15	ns	13,21
t_{WEZ}	Output Buffer Turn-off Delay Time from \overline{WE}	-	13	-	15	ns	13
t_{OH}	Output Data Hold Time	3	-	3	-	ns	21
t_{OHR}	Output Data Hold Time from \overline{RAS}	3	-	3	-	ns	21
t_{RCHR}	Read Command Hold Time from \overline{RAS}	50	-	60	-	ns	
t_{OHO}	Output Data Hold Time from \overline{OE}	3	-	3	-	ns	
t_{CLZ}	\overline{CAS} to Output in Low - Z	2	-	2	-	ns	

Write Cycles

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{WCS}	Write Command Set-up Time	0	-	0	-	§ Å	14
t _{WCH}	Write Command Hold Time	8	-	10	-	§ Å	21
t _{WP}	Write Command Pulse Width	8	-	10	-	§ Å	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	18	-	20	-	§ Å	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	8	-	10	-	§ Å	
t _{DS}	Data-in Set-up Time	0	-	0	-	§ Å	15
t _{DH}	Data-in Hold Time	13	-	15	-	§ Å	15

Read-Modify-Write Cycles

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	116	-	140	-	§ Å	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	72	-	84	-	§ Å	14
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	34	-	§ Å	14
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	42	-	49	-	§ Å	14
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	§ Å	

Refresh Cycles

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	§ Å	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	8	-	10	-	§ Å	
t _{WRP}	$\overline{\text{WE}}$ setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5		5		§ Å	
t _{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	8	-	10	-	§ Å	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	§ Å	

Extended Data Out Mode Cycles

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{HPC}	EDO Page Mode Cycle Time	20	-	25	-	§ Å	20
t _{WPE}	Write pulse width during $\overline{\text{CAS}}$ Precharge	8	-	10	-	§ Å	
t _{RASP}	EDO Mode $\overline{\text{RAS}}$ Pulse Width	-	100000	-	100000	§ Å	16
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	28	-	35	§ Å	9,17
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	33	-	40	-	§ Å	
t _{COL}	$\overline{\text{CAS}}$ Hold Time Referred $\overline{\text{OE}}$	8	-	10	-	§ Å	
t _{COP}	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ set-up Time	5	-	5	-	§ Å	
t _{RCHP}	Read Command Hold Time from $\overline{\text{CAS}}$ Precharge	28	-	35	-	§ Å	
t _{DOH}	Output Data Hold Time from $\overline{\text{CAS}}$ Low	5	-	5	-	§ Å	9,22
t _{OEP}	$\overline{\text{OE}}$ Precharge Time	8	-	10	-	§ Å	

EDO Page Mode Read-Modify-Write cycle

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	§ Å	
t _{CPW}	$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	45	-	54	-	§ Å	14

Present Detect Read cycle

Symbol	Parameter	GMM7738280CTG-5		GMM7738280CTG-6		Unit	Notes
		Min	Max	Min	Max		
t _{PD}	$\overline{\text{PDE}}$ to Valid PD bit		10		10	ns	
t _{PDOFF}	$\overline{\text{PDE}}$ to PD bit in active	2	7	2	7	§ Å	

Notes:

1. AC measurements assume $t_r = 2\text{S} \cdot \text{A}$
2. AC initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before-RAS refresh)
3. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
4. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. $t_{\text{OFF}}(\text{max})$, $t_{\text{OEZ}}(\text{max})$, $t_{\text{OFR}}(\text{max})$ and $t_{\text{WEZ}}(\text{max})$ define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle: if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in extended data out mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH min}}/V_{\text{IL max}}$ level.

20. $t_{HPC}(\min)$ can be achieved during a series of EDO mode early write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode, \overline{RAS} cycle { EDO mode mix cycle (1),(2) } minimum value of \overline{CAS} cycle $t_{HPC}(t_{CAS} + t_{CP} + 2t_T)$ becomes greater than the specified $t_{HPC}(\min)$ value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of \overline{RAS} and \overline{CAS} . Hold time and turn off time are specified by the timing specifications of later rising edge of \overline{RAS} and \overline{CAS} between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
22. t_{DOH} defines the time at which the output level go cross. $V_{OL}=0.8V$, $V_{OH}=2.0V$ of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 μs period on the condition a and b below.
 - a. Enter self refresh mode within 15.6 μs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
 - b. Start burst refresh or distributed refresh at equal interval to all refresh addressed within 15.6 μs after exiting from self refresh mode.
24. In case of entering from \overline{RAS} -only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. For L_version, it is available to apply each 128 μs and 31.2 μs instead of 64 μs and 15.6 μs at note 23.
26. At $t_{RASS} \leq 400 \mu s$, self refresh mode is activated, and not activated at $t_{RASS} > 400 \mu s$. It is undefined within the range of 10 $\mu s \leq t_{RASS} \leq 400 \mu s$. for $t_{RASS} > 40 \mu s$, it is necessary to satisfy t_{RPS} .
27. XXX: H or L (H : $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$)
 //Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms

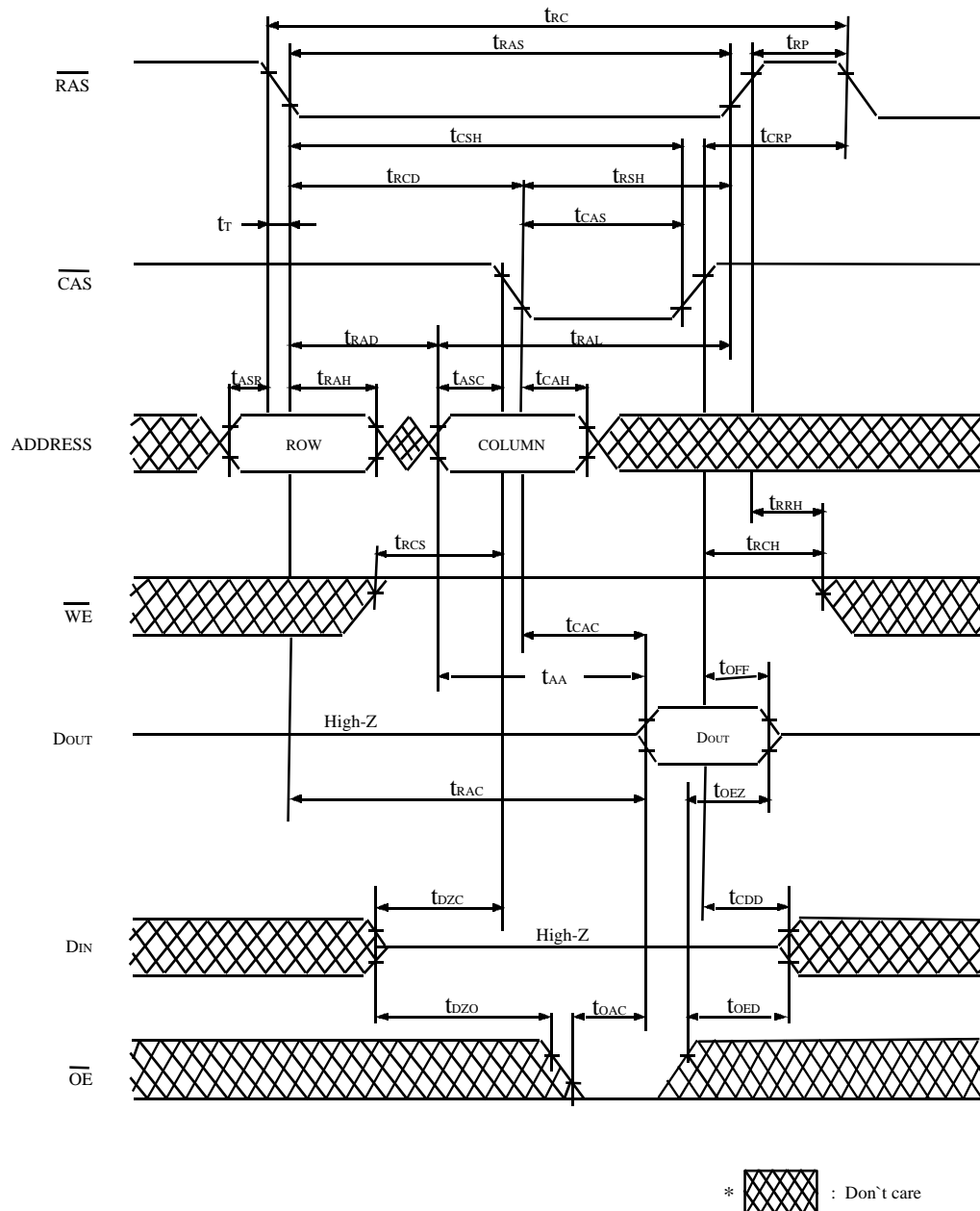


FIGURE 1. READ CYCLE

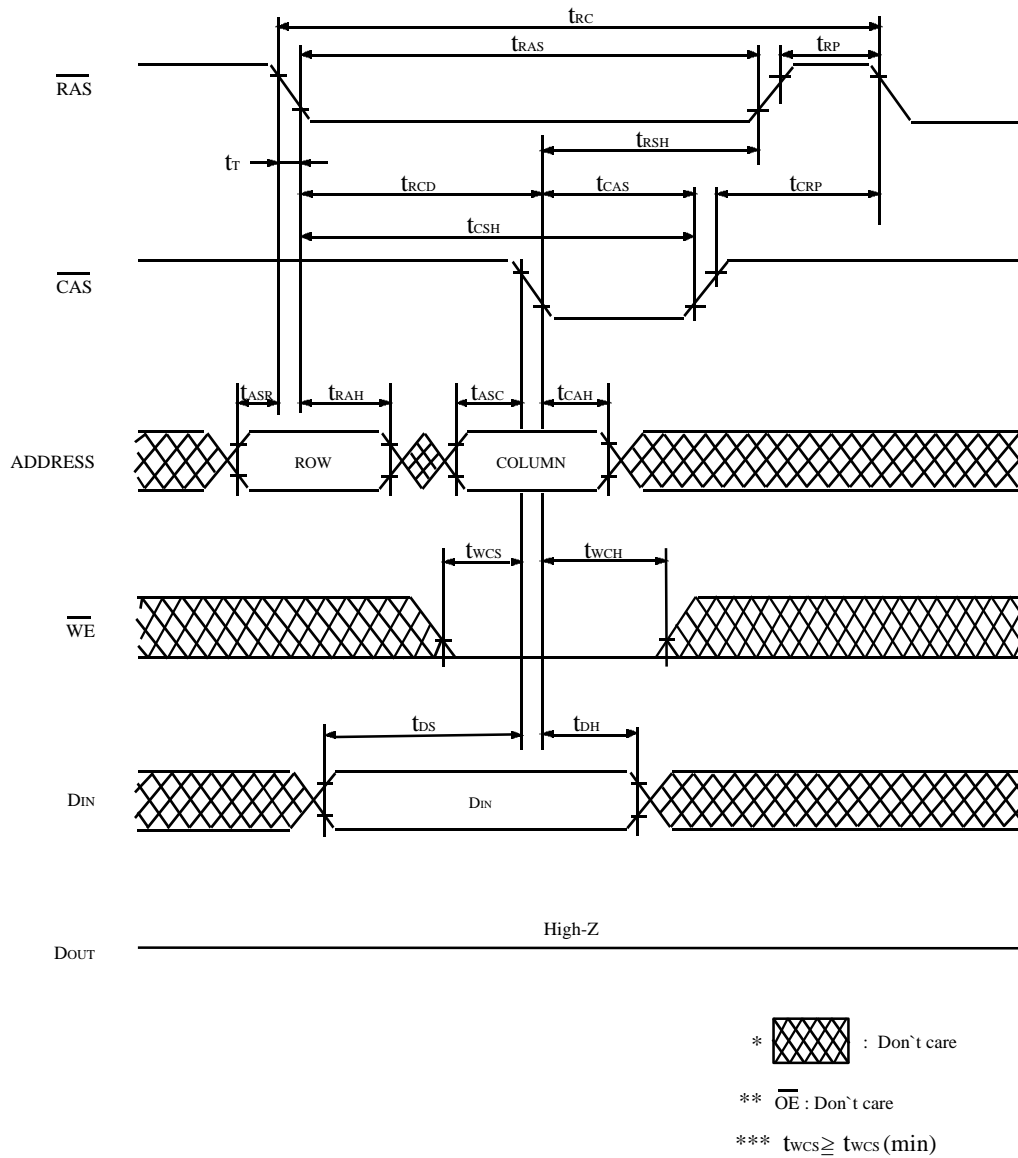


FIGURE 2. EARLY WRITE CYCLE

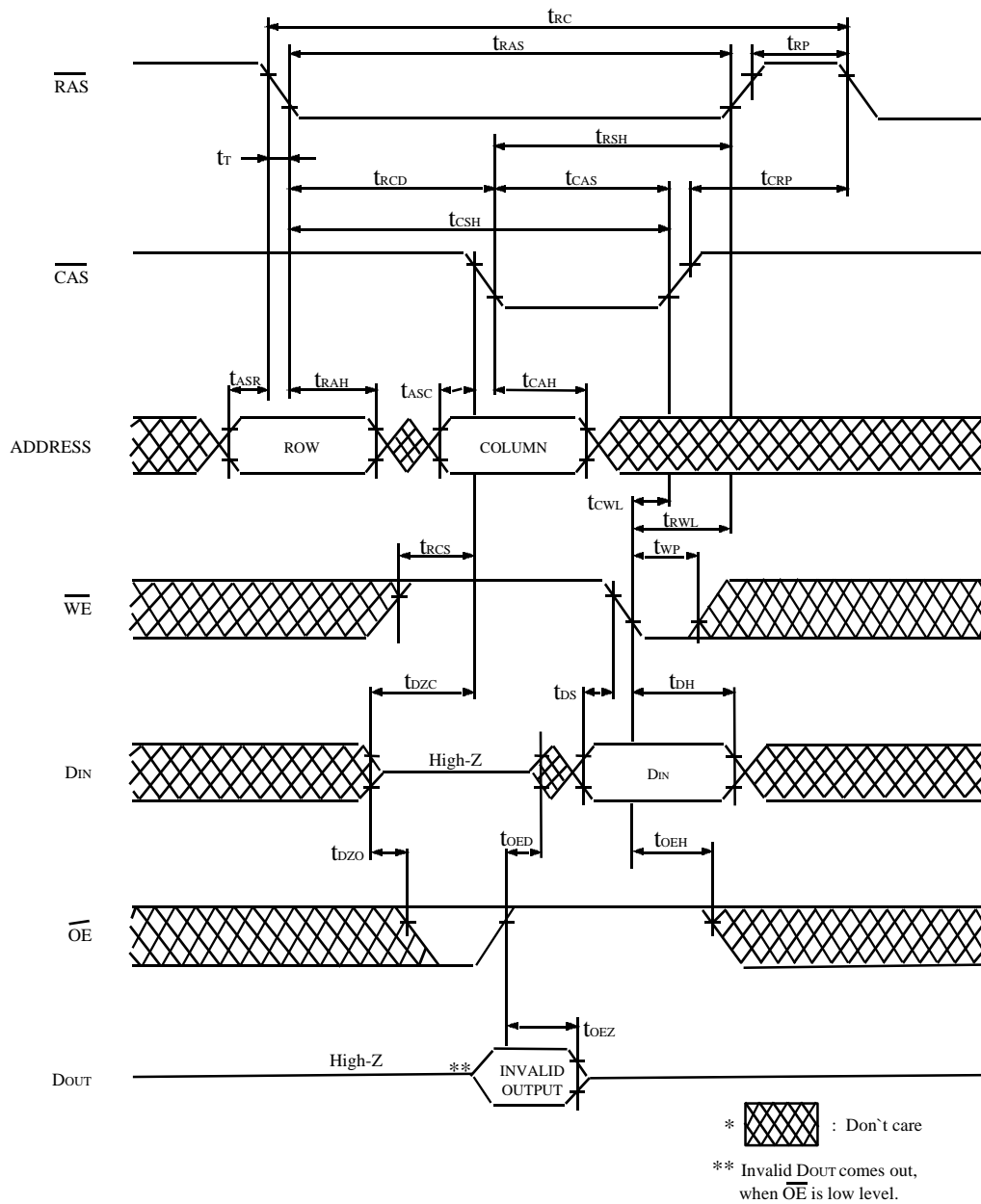


FIGURE 3. DELAYED WRITE CYCLE

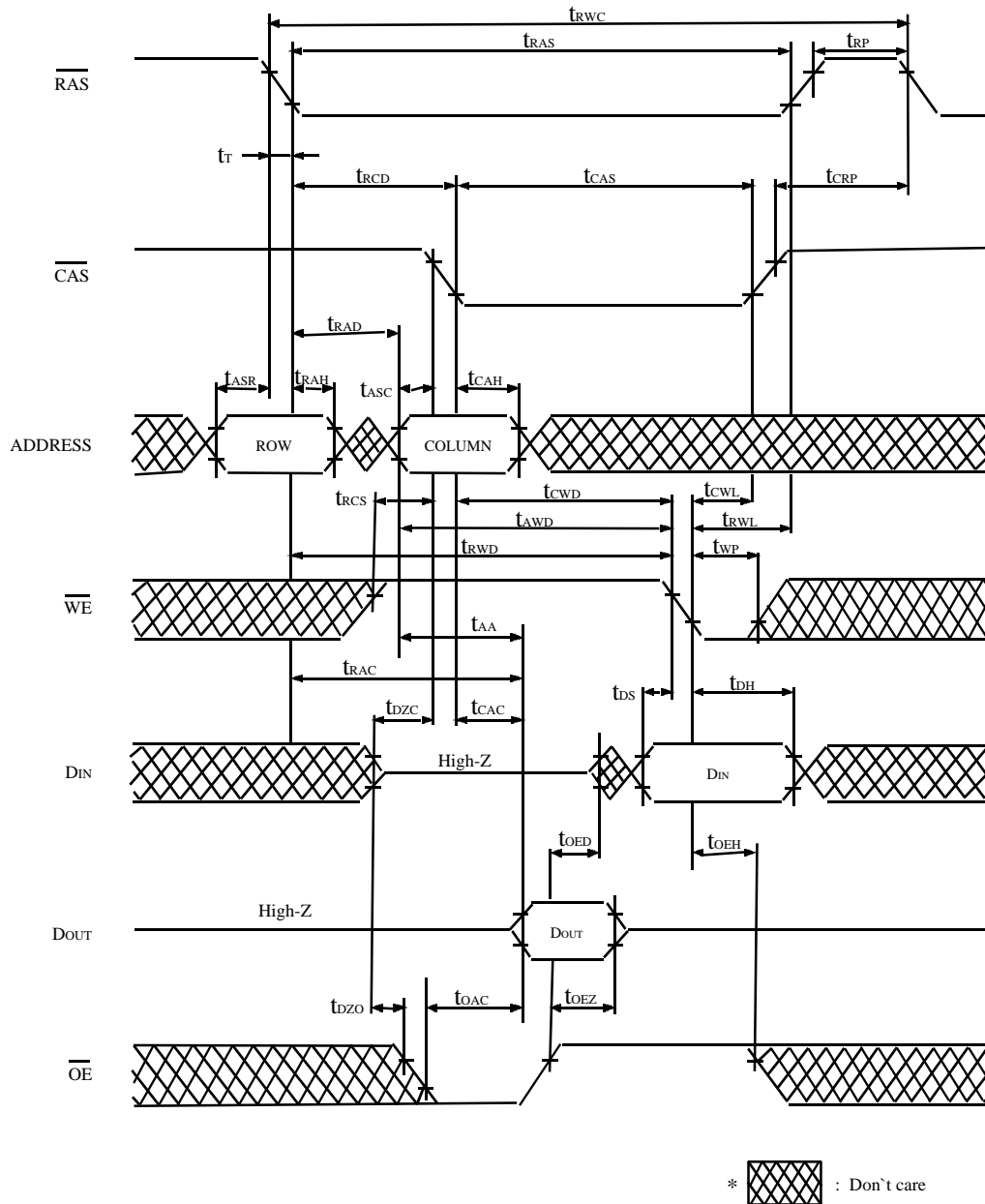


FIGURE 4. READ MODIFY WRITE CYCLE

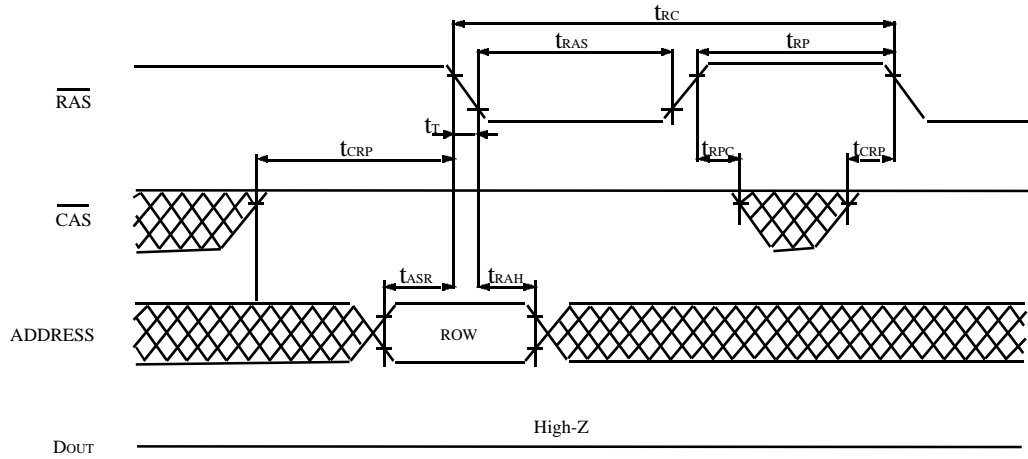


FIGURE 5. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

* $\overline{\text{OE}}, \overline{\text{WE}}$: Don't care
 ** Refresh address :
 A0~A12 (AX0 ~ AX12)

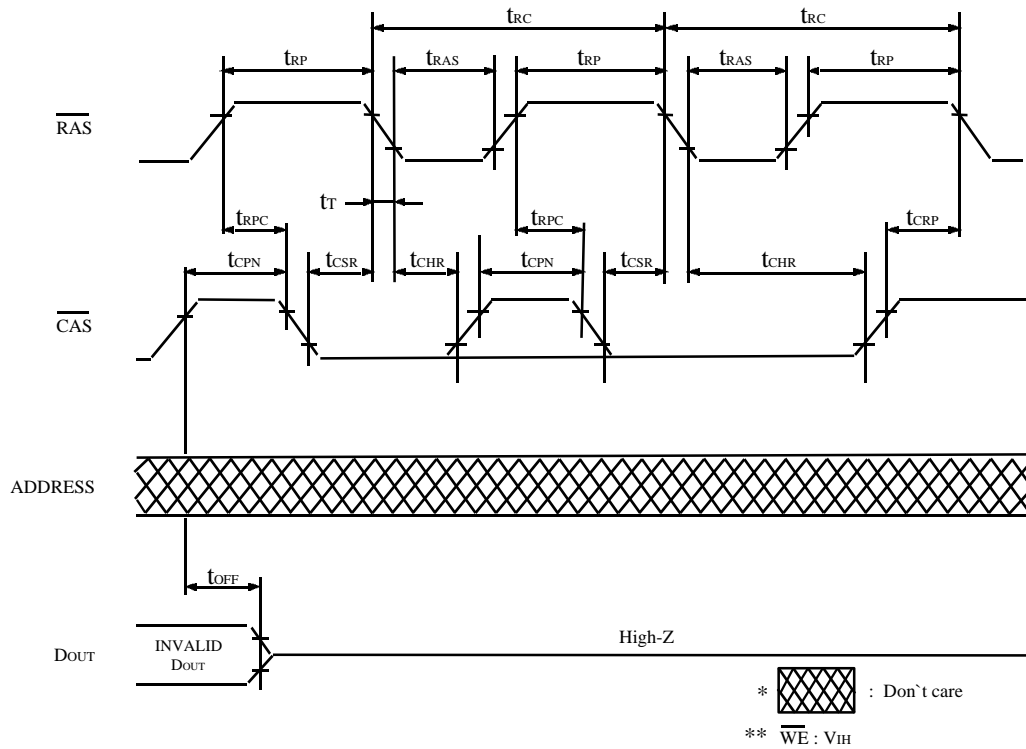



FIGURE 6. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

*  : Don't care
 ** $\overline{\text{WE}}$: V_{IH}

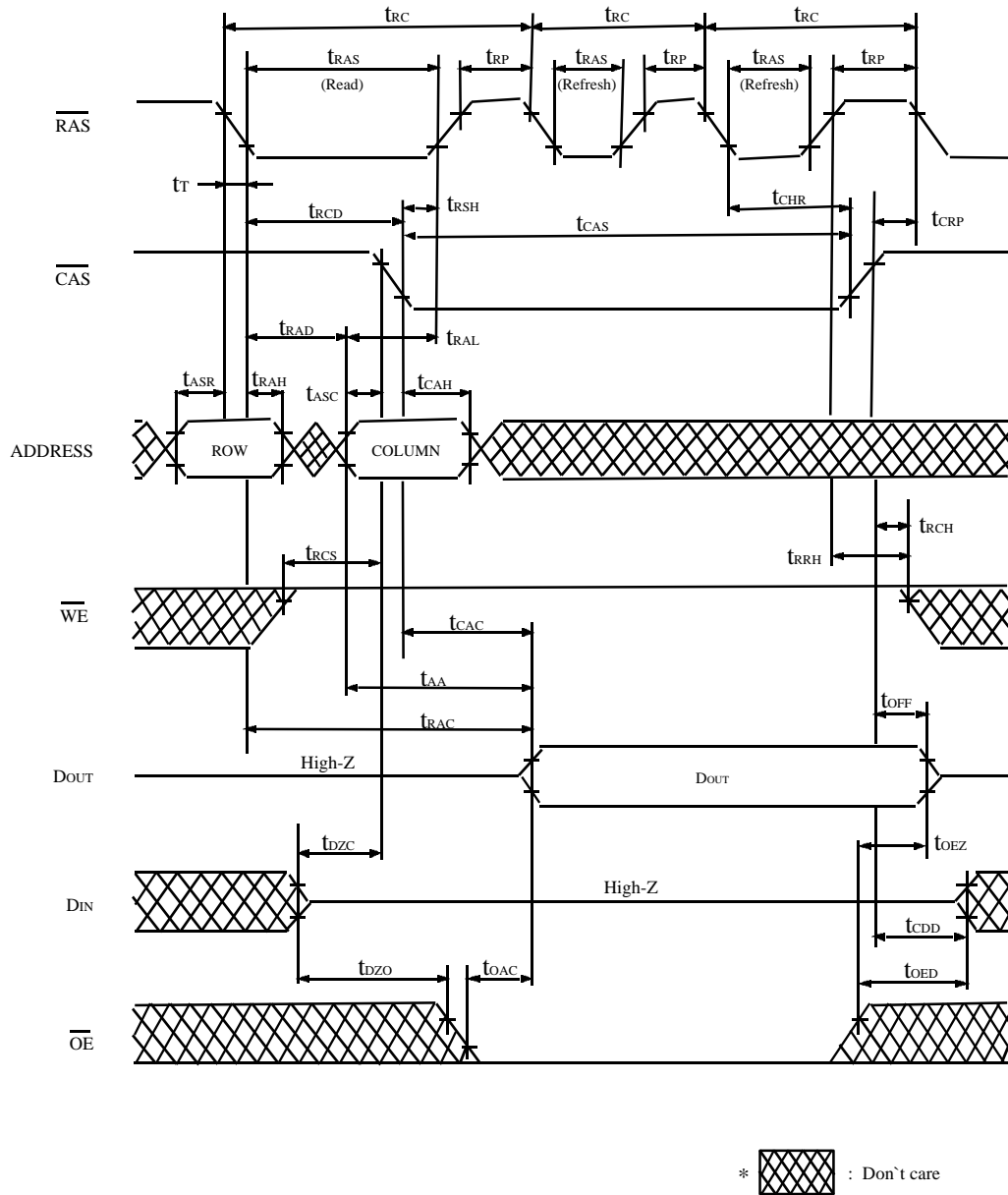


FIGURE 7. HIDDEN REFRESH CYCLE

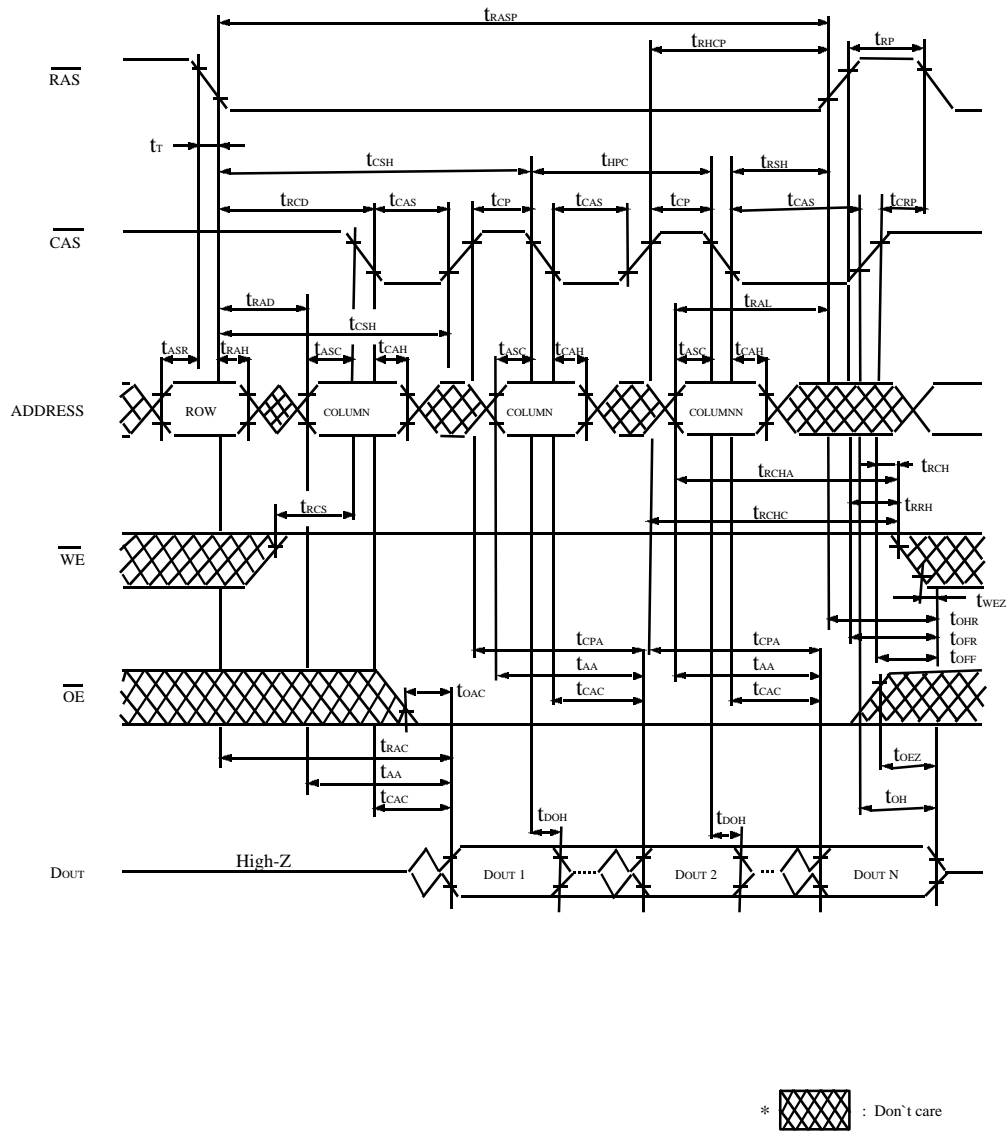


FIGURE 8. EXTENDED DATA OUT MODE READ CYCLE



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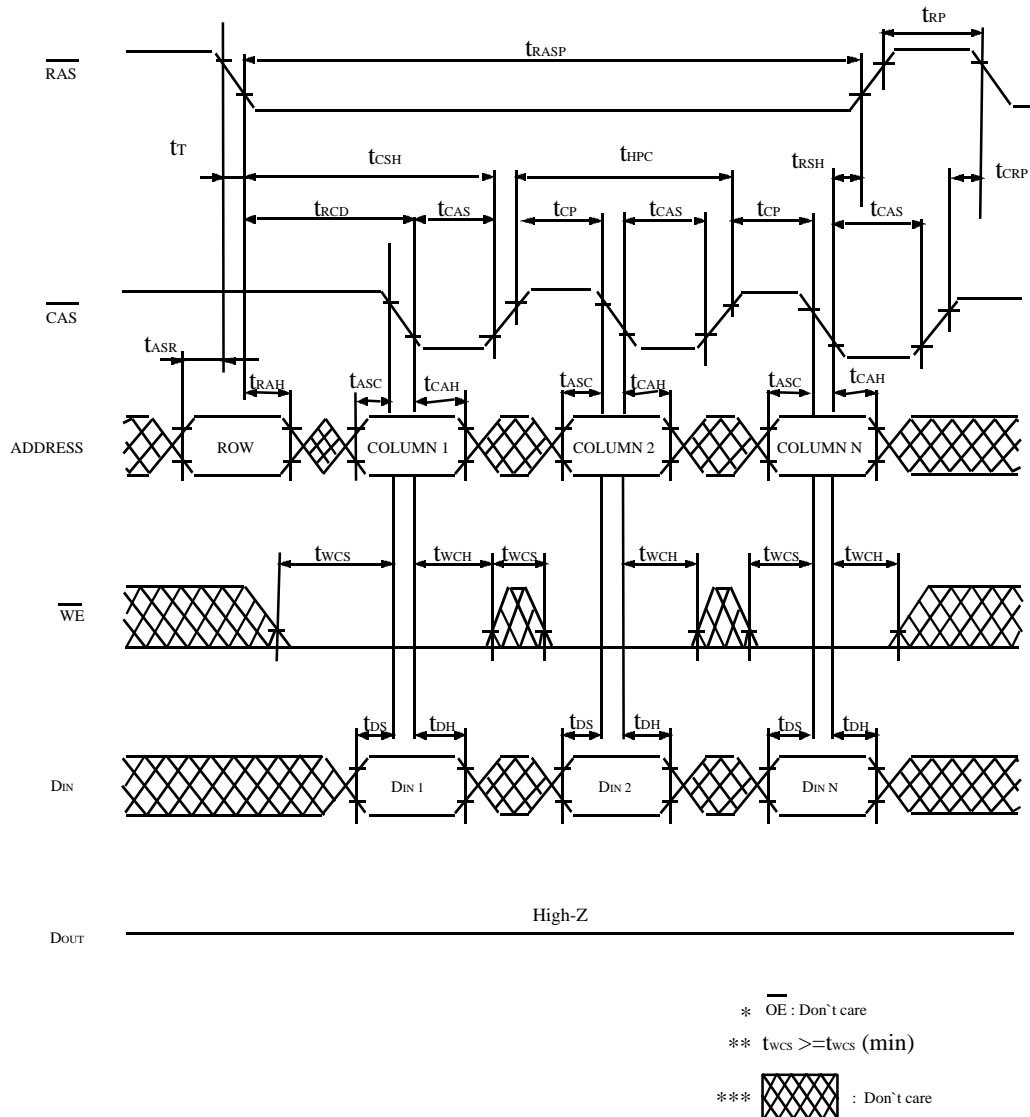


FIGURE 10. EXTENDED DATA OUT MODE EARLY WRITE CYCLE









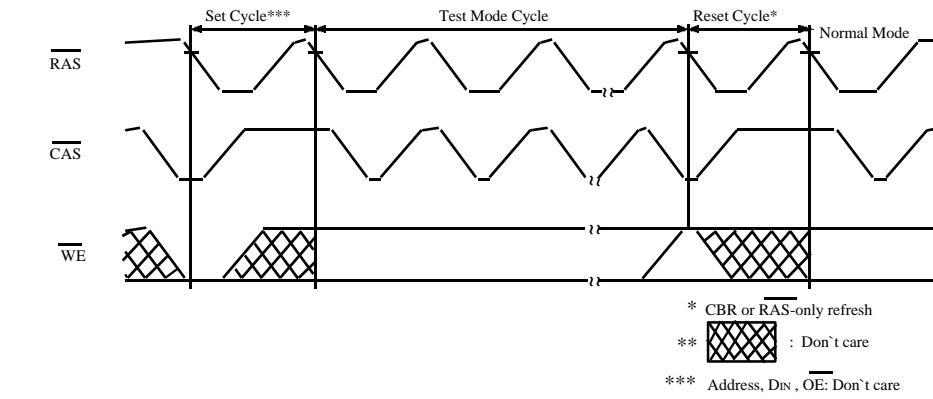


FIGURE 15. TEST MODE CYCLE

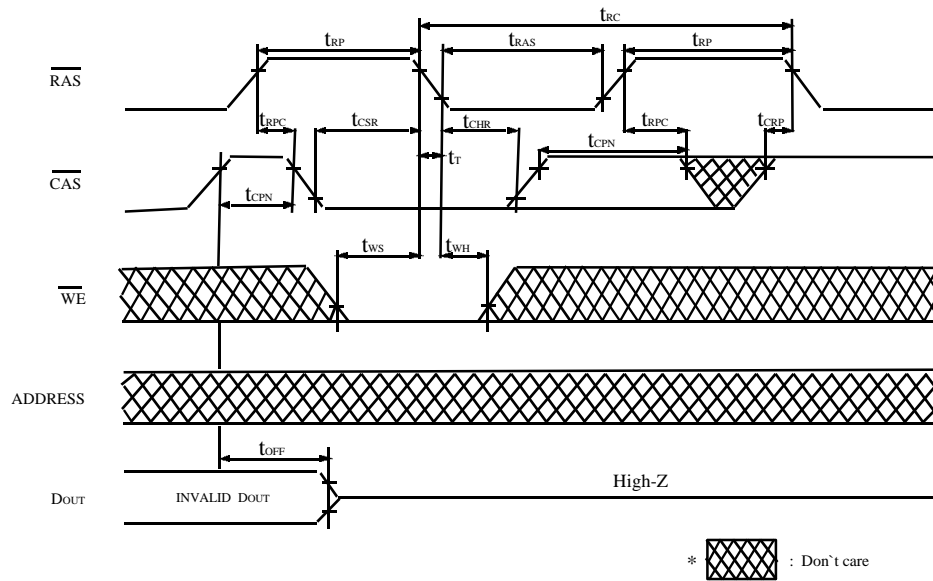


FIGURE 16. TEST MODE SET CYCLE



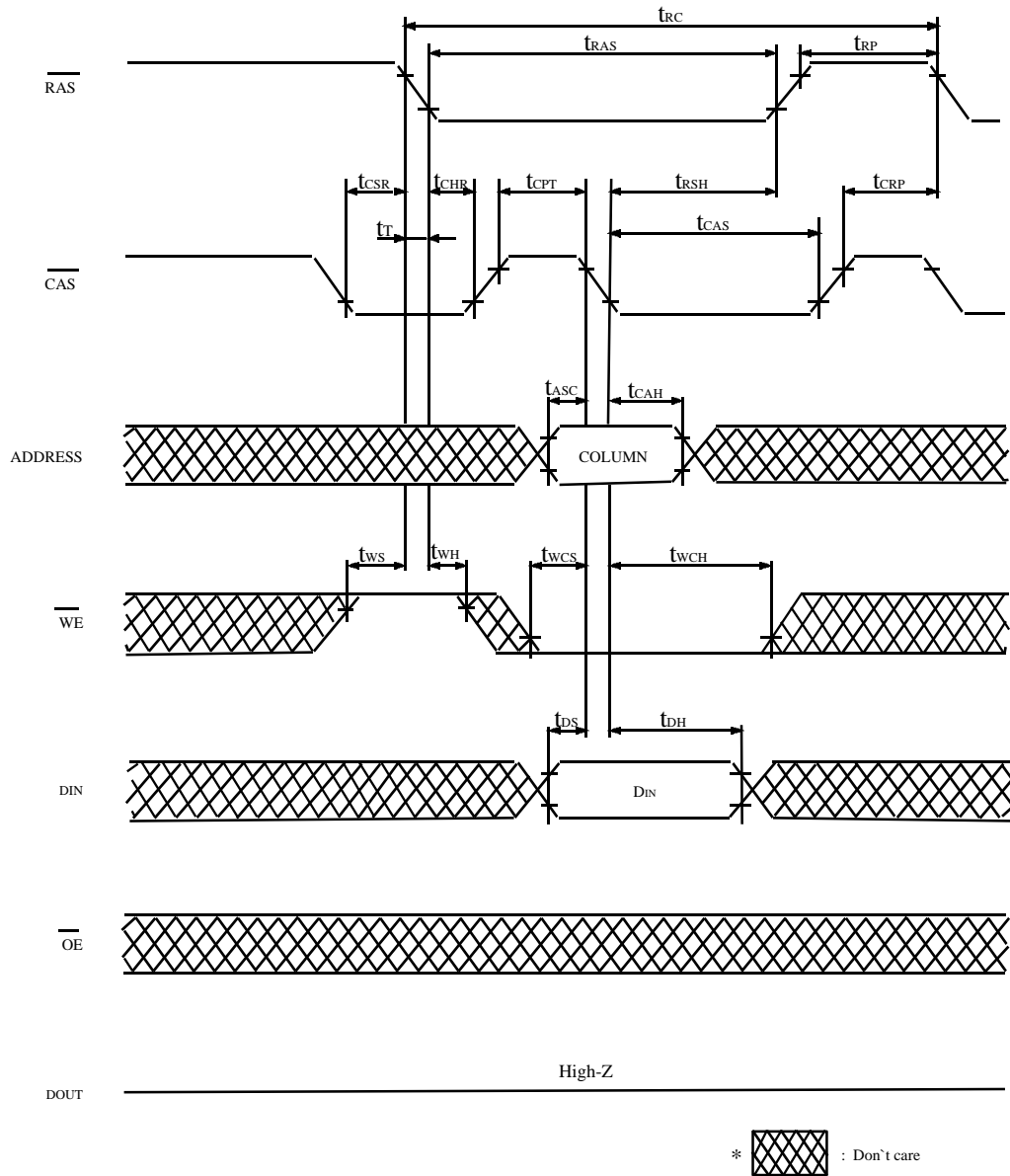


FIGURE 17. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER CHECK CYCLE (WRITE)

Unit: mil (mm)
* (1 mil = 1/1000 inches)

