4-BIT SINGLE CHIP MICROCOMPUTERS

GMS34XXXT SERIES

USER`S MANUAL

- GMS34004T
- GMS34112T
- GMS34140T

Revision 1.1

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Editor's E-Mail : rhja@hynix.com

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CHAPTER 1. Introduction

OUTLINE OF CHARACTERISTICS

The GMS340 series are remote control transmitter which uses CMOS technology, and the EPROM version of GMS34XXX series.
This enables transmission code outputs of different configurations, multiple custom code output, and double push key output for easy fabrication.
The GMS340 series are suitable for remote control of TV, VCR, FANS, Air-conditioners, Audio Equipments, Toys, Games etc.

Characteristics

- Program memory : 512bytes for GMS34004T
  1,024 bytes for GMS34112T/140T
- Data memory : 32 ¡¿ 4 bits
- 43 types of instruction set
- 3 levels of subroutine nesting
- 1 bit output port for a large current (REMOUT signal)
- Operating frequency :300KHz~500KHz at KHz version
  2.4MHz~4MHz at MHz version
  300KHz~4.2MHz at WIDE version
- Instruction cycle : f_{OSC}/6 at KHz and WIDE version
  f_{OSC}/48 at MHz version
- CMOS process (3.0V or 5.0V power supply)
- Stop mode (Through internal instruction)
- Released stop mode by key input
- Built in capacitor for ceramic oscillation circuit at KHz version
- Built in a watch dog timer (WDT)
- Low operating voltage : 2.2~4.5V (at KHz and MHz version)
  Normal operating voltage: 4.0~5.0V (at WIDE version)

Series	GMS34004T	GMS34112T	GMS34140T
Program memory	512	1,024	¡Ç
Data memory	32 ¡¿ 4	¡Ç	¡Ç
I/O ports	-	4	¡Ç
Input ports	4	¡Ç	¡Ç
Output ports	6 D0 ~ D5	¡Ç ¡Ç	10 D0 ~ D9
Package	16DIP	20DIP/SOP/SSOP	24DIP/SOP
KHz version	GMS34004TK	GMS34112TK	GMS34140TK
MHz version	GMS34004TM	GMS34112TM	GMS34140TM
WIDE version	GMS34004TW	GMS34112TW	GMS34140TW

Table 1-1 GMS34XXXT series members

Block Diagram

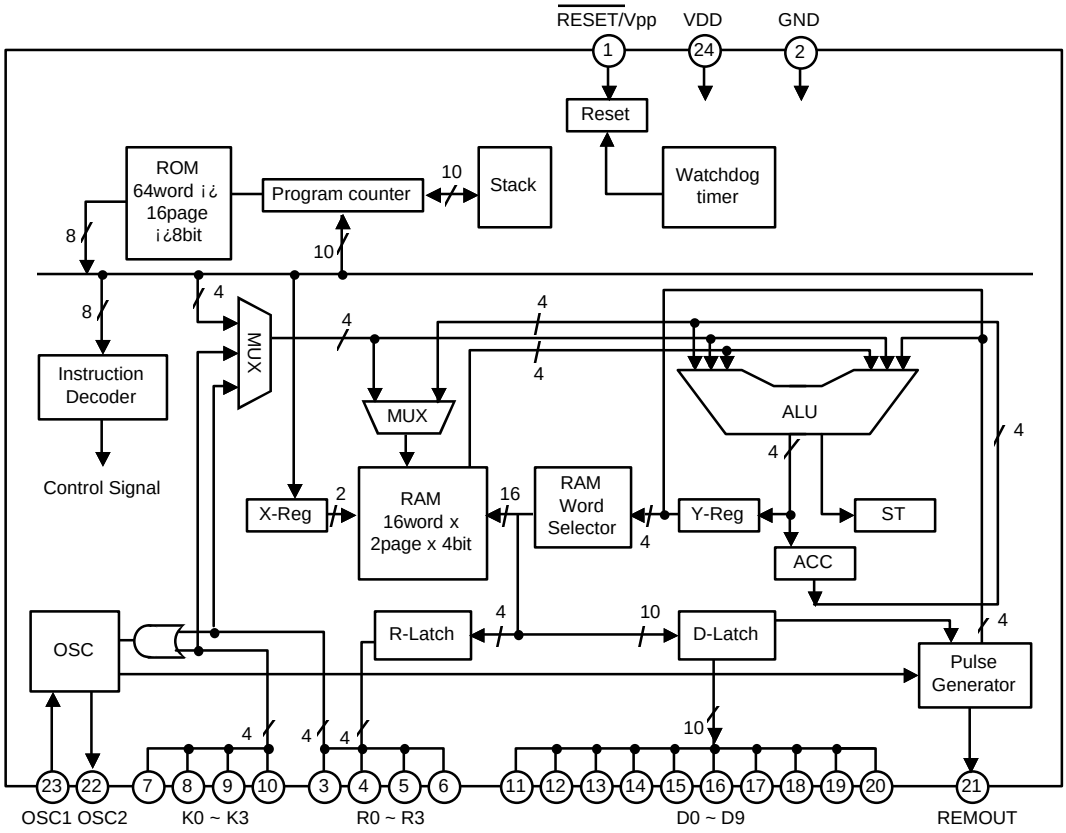


Fig 1-1 Block Diagram (In case of GMS34140T)

Pin Assignment and terminals

Pin Assignment

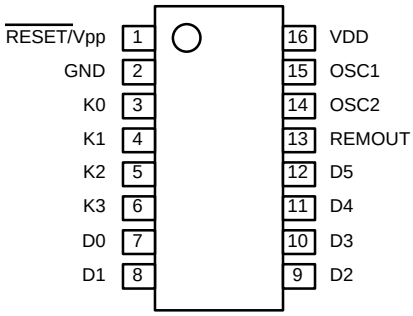


Fig 1-2 GMS34004T Pin Assignment (16PDIP)

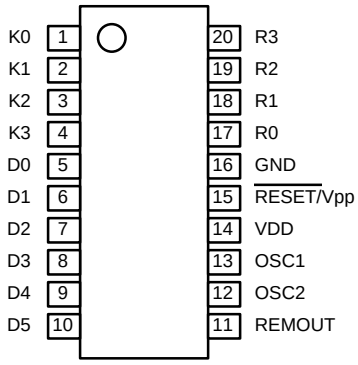


Fig 1-3 GMS34112T Pin Assignment (20DIP/SOP)

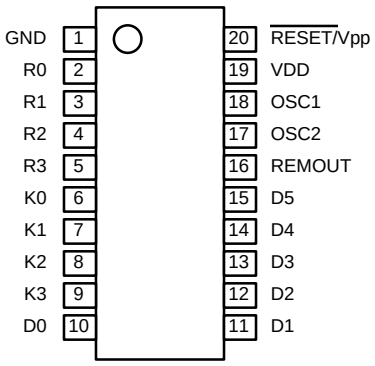


Fig 1-4 GMS34112T Pin Assignment (20SSOP only)

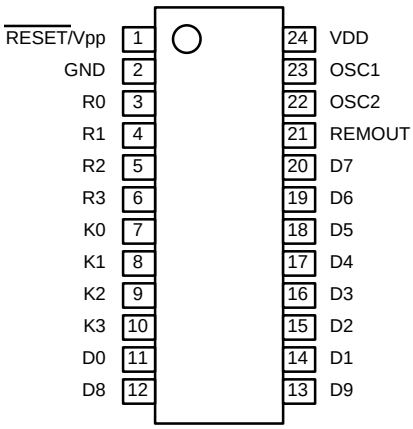


Fig 1-5 GMS34140T Pin Assignment (24DIP/SOP)

Pin Dimension

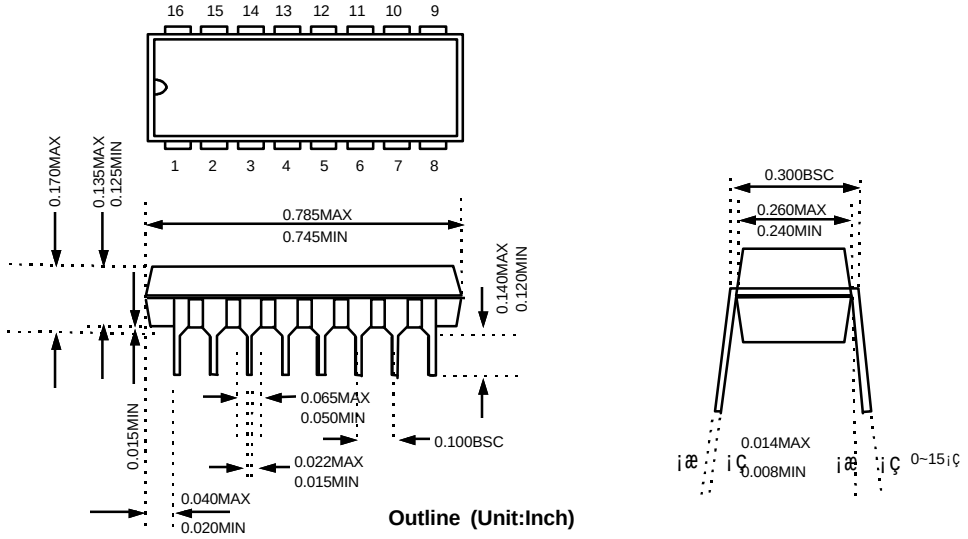


Fig 1-6 16PDIP Pin Dimension

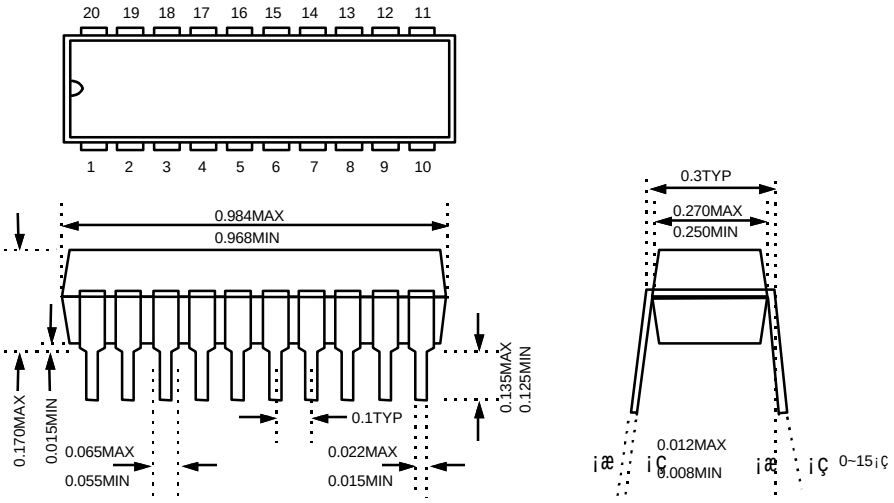
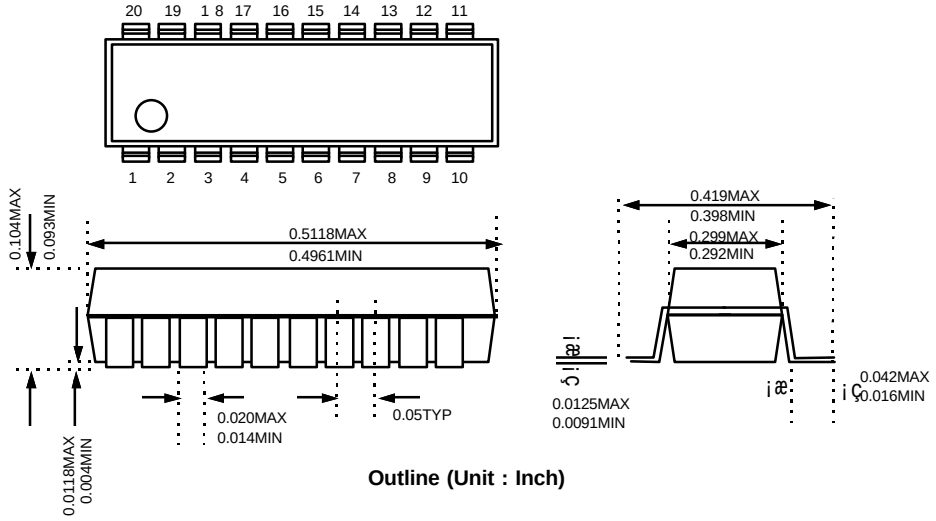
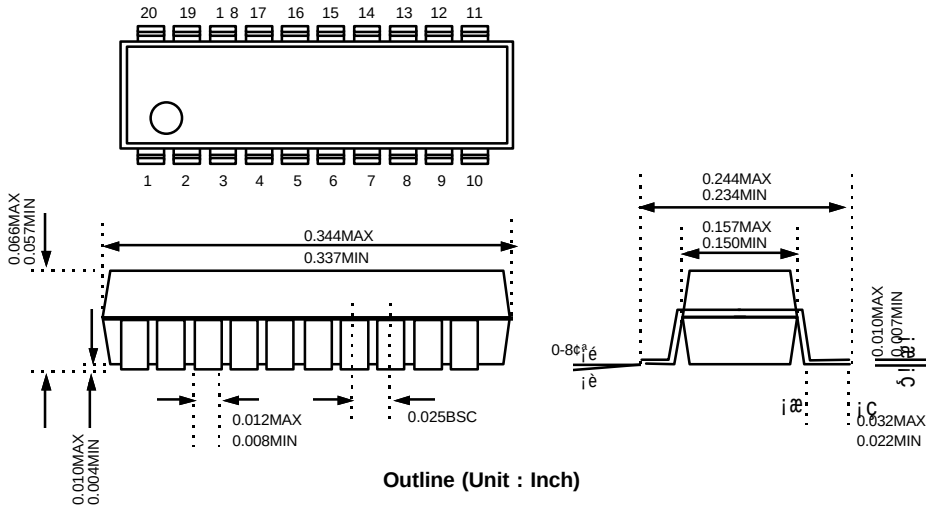


Fig 1-7 20PDIP Pin Dimension



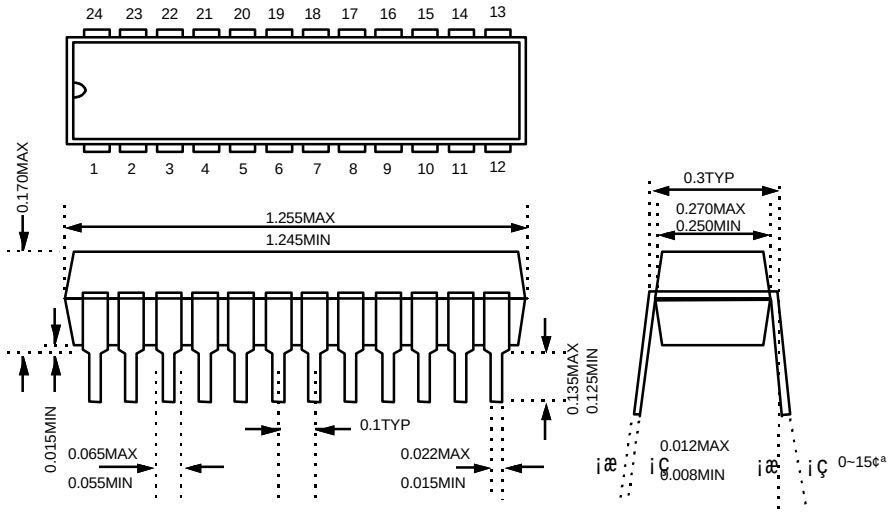
Outline (Unit : Inch)

Fig 1-8 20SOP Pin Dimension



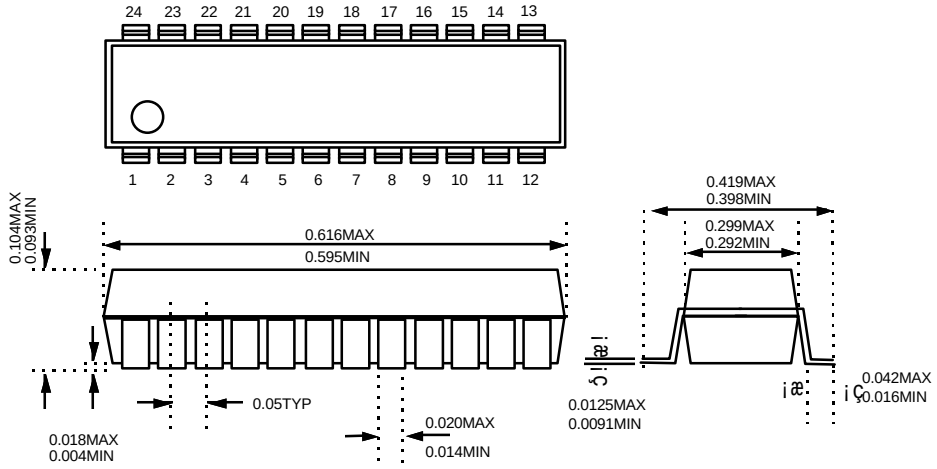
Outline (Unit : Inch)

Fig 1-9 20SSOP Pin Dimension



Outline (Unit : Inch)

Fig 1-10 24Skinny DIP Pin Dimension



Outline (Unit : Inch)

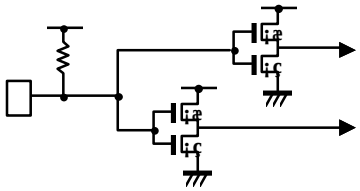
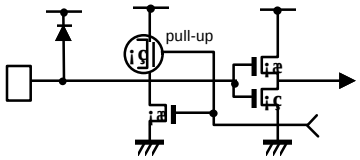
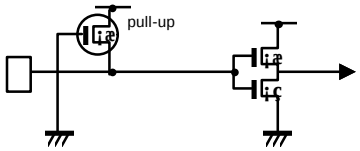
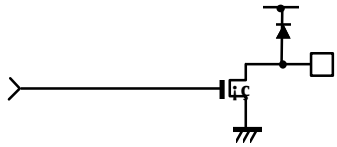
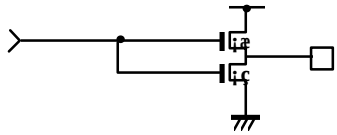
Fig 1-11 24SOP Pin Dimension

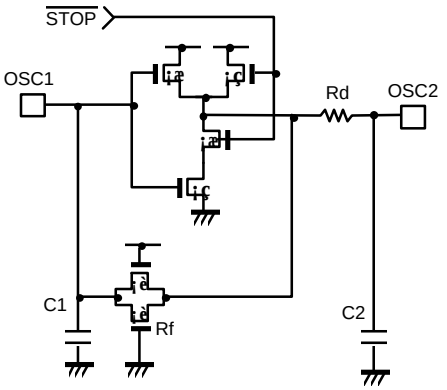
Pin Description and Circuit

Pin Description

Pin	I/O	Function
V_{DD}	-	Connected to 2.2~4.5V power supply at KHz and MHz version or 4.0 ~ 5.5V power supply at WIDE version.
GND	-	Connected to 0V power supply.
$\overline{\text{RESET}}$	Input	Used to input a manual reset. When the pin goes "L", the D-output ports and REMOUT-output port are initialized to "L", and ROM address is set to address 0 on page 0. For programming, this pin receives 12.5V programming voltage.
K0~K3	Input	4-bit input port. STOP mode is released by "L" input of each pin.
D0~D9	Output	The output is the structure of N-channel-open-drain.
R0~R3	I/O	4-bit I/O port. (Input mode is set only when each of them output "H".) In outputting, each can be set and reset independently(or at once.) The output is in the form of C-MOS. STOP mode is released by "L" input of each pin.
REMOUT	Output	High current output port. The output is in the form of C-MOS. The state of large current on is "H".
OSC1	Input	Oscillator input. Input to the oscillator circuit and connection point for ceramic resonator. Internal capacitors available at KHz version. A feedback resistor is connected between this pin and OSC2.
OSC2	Output	Connect a resonator between this pin and OSC1.

I/O circuit types and options

Pin	I/O	I/O circuit	Note
$\overline{\text{Reset}}$/Vpp	I		Hysteresis Input Type. Built in pull-up-resistor, Typical 800㏀
R0~R3	I/O		CMOS output. "H" output at reset. Built in MOS Tr for pull-up about 120㏀.
K0~K3	I		Built in MOS Tr for pull-up About 120㏀.
D0~D9	O		Open drain output. "L" output at reset.
REMOUT	O		CMOS output. "L" output at reset. High current output source.

Pin	I/O	I/O circuit	Note
OSC2	O		Built in feedback-resistor about 1§Û Built in damping-resistor Rd = 4§Ú [No resistor in MHz operation] Built in resonance Capacitor at KHz version C1=C2 = 100pF ¡¾15% [C1,C2 are not available for MHz and WIDE version]
OSC1	I		

Frequency	Resonator Maker	Part Name	Load Capacitor
320KHz	CQ	ZTB320D	C1=C2=Open
500KHz	CQ	ZTB500E	C1=C2=Open
CQ recommend 430KHz~500KHz resonator			
3.43MHz	CQ	ZTA3.43MG	C1=C2=30pF
3.52MHz	TDK	FCR3.52M5	C1=C2=33pF
3.64MHz	CQ	ZTA3.64MG	C1=C2=30pF
	TDK	FCR3.64M5	C1=C2=33pF
3.84MHz	CQ	ZTA3.84MG	C1=C2=30pF
	TDK	FCR3.84M5	C1=C2=33pF
4.00MHz	CQ	ZTA4.00MG	C1=C2=30pF

Electrical Characteristics

Absolute maximum ratings (Ta = 25¡É)

Parameter	Symbol	Max. rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Programming Voltage	V_{PP}	-0.3 ~ 13.5	V
Power dissipation	P_D	700 *	mW
Storage temperature range	Tstg	-55 ~ 125	¡É
Input voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Output voltage	V_{OUT}	-0.3 ~ V_{DD}+0.3	V

* Thermal derating above 25¡É : 6mW per degree ¡É rise in temperature.

Recommended operation condition

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	300 ~ 500KHz	2.2 ~ 4.5	V
		2.4 ~ 4MHz	2.2 ~ 4.5	
		300KHz ~ 4.2MHz	4.0 ~ 5.5	
Operating temperature	Topr	-	-20 ~ +70	¡É

Electrical characteristics for low voltage products (Ta=25¡É, V_{DD}=3V)

Parameter		Symbol	Limits			Unit	Condition
			Min.	Typ.	Max.		
Input H current		I_{IH}	-	-	1	uA	VI=V_{DD}
$\overline{\text{RESET}}$ input L current		I_{IL2}	-2	-7.5	-16	uA	VI=GND
K, R input L current		I_{IL1}	-9	-25	-50	uA	VI=GND, Output off, Pull-Up resistor provided.
K, R input H voltage		V_{IH1}	2.1	-	-	V	-
K, R input L voltage		V_{IL1}	-	-	0.9	V	-
$\overline{\text{RESET}}$ input H voltage		V_{IH2}	2.25	-	-	V	-
$\overline{\text{RESET}}$ input L voltage		V_{IL2}	-	-	0.75	V	V
D. R output L voltage		V_{OL2}	-	0.15	0.4	V	I_{OL}=1mA
REMOUT output L voltage		V_{OL1}	-	0.15	0.4	V	I_{OL}=100uA
REMOUT output H voltage		V_{OH1}	2.1	2.5	-	V	I_{OH}=-8mA
OSC2 output L voltage		V_{OL3}	-	0.4	0.9	V	I_{OL}=70uA
OSC2 output H voltage		V_{OH3}	2.1	2.5	-	V	I_{OH}=70uA
D, R output leakage current		I_{OL}	-	-	1	uA	V_{0UT}=V_{DD}, Output off
Current on STOP mode		I_{STOP}	-	-	1	uA	At STOP mode
Operating supply current 1		I_{DD1} *	-	0.3	4.0	mA	f_{OSC}=455KHz
Operating supply current 2		I_{DD2} *	-	0.5	4.0	mA	f_{OSC}=4MHz
System clock frequency	f_{OSC}/6	f_{OSC}	300	-	500	KHz	KHz version
	f_{OSC}/48	f_{OSC}	2.4	-	4	MHz	MHz version

* I_{DD1}, I_{DD2}, is measured at RESET mode.

Electrical characteristics (Ta=25¡É, V_{DD}=5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Input H current	I_{IH}	-	-	5	uA	VI=V_{DD}
$\overline{\text{RESET}}$ input L current	I_{IL2}	-2	-	-20	uA	VI=GND
K, R input L current	I_{IL1}	-9	-	-150	uA	VI=GND, Output off, Pull-Up resistor provided.
K, R input H voltage	V_{IH1}	0.7*V_{DD}	-	-	V	-
K, R input L voltage	V_{IL1}	-	-	0.3*V_{DD}	V	-
$\overline{\text{RESET}}$ input H voltage	V_{IH2}	0.75*V_{DD}	-	-	V	-
$\overline{\text{RESET}}$ input L voltage	V_{IL2}	-	-	0.25*V_{DD}	V	V
D. R output L voltage	V_{OL2}	-	-	0.4	V	I_{OL}=2mA
REMOUT output L voltage	V_{OL1}	-	-	0.4	V	I_{OL}=100uA
REMOUT output H voltage	V_{OH1}	V_{DD}-1.0	-	-	V	I_{OH}=-8mA
OSC2 output L voltage	V_{OL3}	-	-	0.9	V	I_{OL}=70uA
OSC2 output H voltage	V_{OH3}	V_{DD}-1.0	-	-	V	I_{OH}=-70uA
D, R output leakage current	I_{OL}	-	-	5	uA	V_{0UT}=V_{DD}, Output off
Current on STOP mode	I_{STOP}	-	-	10	uA	At STOP mode
Operating supply current	I_{DD}	-	-	10	mA	At RESET mode
System clock frequency f_{OSC}/6	f_{OSC}	0.3	-	4.2	MHz	WIDE version

CHAPTER 2. Architecture

BLOCK DESCRIPTION

Program Memory (EPROM)

The GMS34XXXT series can incorporate maximum 1,024 words (64 words¡¿16 pages¡¿8bits) for program memory. Program counter PC (A0~A5) and page address register (A6~A9) are used to address the whole area of program memory having an instruction (8bits) to be next executed.
The program memory consists of 64 words on each page, and thus each page can hold up to 64 steps of instructions.
The program memory is composed as shown below.

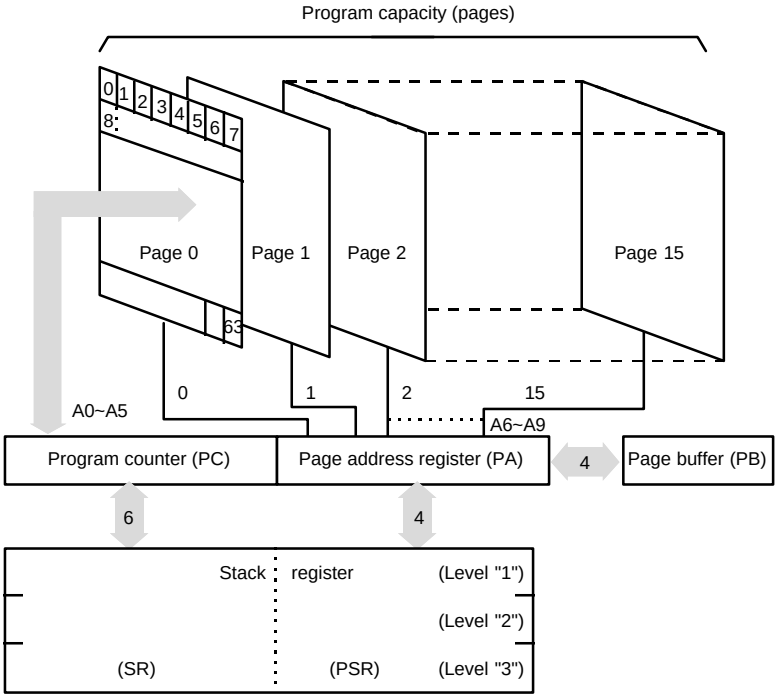


Fig 2-1 Configuration of Program Memory

EPROM Address Register

The following registers are used to address the EPROM.

- Page address register (PA) :
  Holds EPROM's page number (0~Fh) to be addressed.
- Page buffer register (PB) :
  Value of PB is loaded by an LPBI command when newly addressing a page. Then it is shifted into the PA when rightly executing a branch instruction (BR) and a subroutine call (CAL).
- Program counter (PC) :
  Available for addressing word on each page.
- Stack register (SR) :
  Stores returned-word address in the subroutine call mode.

(1) Page address register and page buffer register :

Address one of pages #0 to #15 in the EPROM by the 4-bit binary counter.
Unlike the program counter, the page address register is usually unchanged so that the program will repeat on the same page unless a page changing command is issued. To change the page address, take two steps such as (1) writing in the page buffer what page to jump (execution of LPBI) and (2) execution of BR or CAL, because instruction code is of eight bits so that page and word can not be specified at the same time.
In case a return instruction (RTN) is executed within the subroutine that has been called in the other page, the page address will be changed at the same time.

(2) Program counter :

This 6-bit binary counter increments for each fetch to address a word in the currently addressed page having an instruction to be next executed.
For easier programming, at turning on the power, the program counter is reset to the zero location. The PA is also set to "0". Then the program counter specifies the next EPROM address in random sequence.
When BR, CAL or RTN instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (a_0 to a_5), or for RTN, and address is fetched from stack register No. 1.

(3) Stack register :

This stack register provides two stages each for the program counter (6 bits) and the page address register (4bits) so that subroutine nesting can be made on two levels.

Data memory (RAM)

Up to 32 nibbles (16 words ¡¿ 2pages ¡¿ 4bits) is incorporated for storing data. The whole data memory area is indirectly specified by a data pointer (X,Y). Page number is specified by zero bit of X register, and words in the page by 4 bits in Y-register. Data memory is composed in 16 nibbles/page. Figure 2-2 shows the configuration.

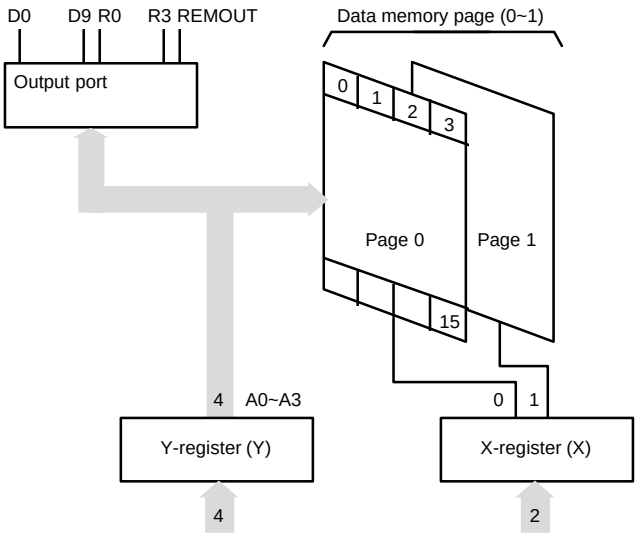


Fig 2-2 Composition of Data Memory

X-register (X)

X-register is consist of 2bit, X0 is a data pointer of page in the RAM, X1 is only used for selecting of D8~D9 with value of Y-register

	X1=0	X1=1
Y=0	D0	D8
Y=1	D1	D9

Table 2-1 Mapping table between X and Y register

Y-register (Y)

Y-register has 4 bits. It operates as a data pointer or a general-purpose register. Y-register specifies and address (a_0~a_3) in a page of data memory, as well as it is used to specify an output port. Further it is used to specify a mode of carrier signal outputted from the REMOUT port. It can also be treated as a general-purpose register on a program.

Accumulator (A_{CC})

The 4-bit register for holding data and calculation results.

Arithmetic and Logic Unit (ALU)

In this unit, 4bits of adder/comparator are connected in parallel as it's main components and they are combined with status latch and status logic (flag.)

(1) Operation circuit (ALU) :

The adder/comparator serves fundamentally for full addition and data comparison. It executes subtraction by making a complement by processing an inversed output of A_{CC} (A_{CC}+1)

(2) Status logic :

This is to bring an ST, or flag to control the flow of a program. It occurs when a specified instruction is executed in three cases such as overflow or underflow in operation and two inputs unequal.

State Counter (SC)

A fundamental machine cycle timing chart is shown below. Every instruction is one byte length. Its execution time is the same. Execution of one instruction takes 6 clocks for fetch cycle and 6 clocks for execute cycle (12 clocks in total). Virtually these two cycles proceed simultaneously, and thus it is apparently completed in 6 clocks (one machine cycle). Exceptionally BR, CAL and RTN instructions is normal execution time since they change an addressing sequentially. Therefore, the next instruction is prefetched so that its execution is completed within the fetch cycle.

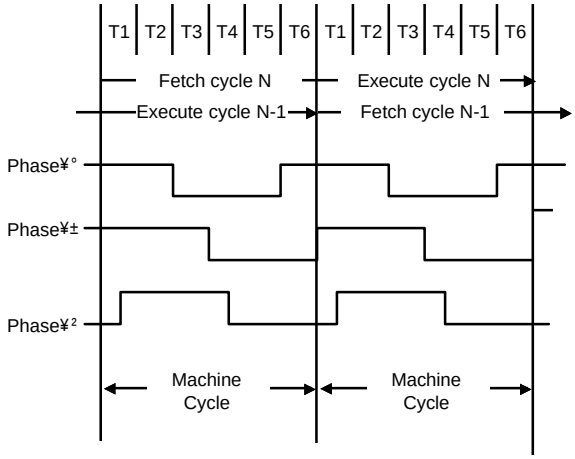
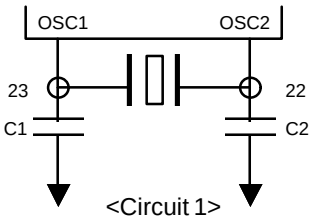


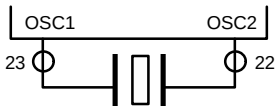
Fig. 2-3 Fundamental timing chart

Clock Generator

The GMS34XXXT series has an internal clock oscillator. The oscillator circuit is designed to operate with an external ceramic resonator. Internal capacitors are available at KHz version. Oscillator circuit is able to organize by connecting ceramic resonator to outside.
* It is necessary to connect capacitor to outside in order to change ceramic resonator, you must refer to a manufacturer`s resonator matching guide.



<Circuit 1>

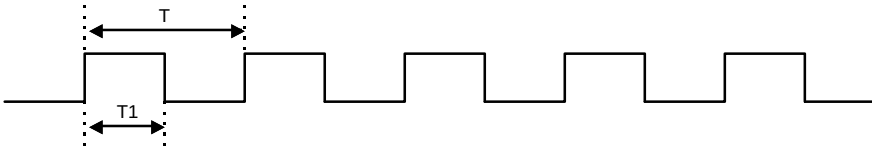


<Circuit 2>

Version	Operating Frequency		Oscillation Circuit
KHz	300KHz ~ 500KHz	Internal capacitor	Circuit 2
		No Internal capacitor	Circuit 1
MHz	2.4MHz ~ 4MHz	No Internal capacitor	Circuit 1
WIDE	300KHz ~ 4.2MHz	No Internal capacitor	Circuit 1

Pulse generator

The following frequency and duty ratio are selected for carrier signal outputted from the REMOUT port depending on a PMR (Pulse Mode Register) value set in a program.



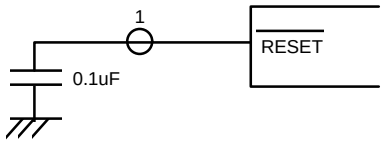
PMR	REMOUT signal
0	$T=1/f_{PUL} = 12/f_{OSC}$ [$96/f_{OSC}$], T1/T = 1/2
1	$T=1/f_{PUL} = 12/f_{OSC}$ [$96/f_{OSC}$], T1/T = 1/3
2	$T=1/f_{PUL} = 8/f_{OSC}$ [$64/f_{OSC}$], T1/T = 1/2
3	$T=1/f_{PUL} = 8/f_{OSC}$ [$64/f_{OSC}$], T1/T = 1/4
4	$T=1/f_{PUL} = 11/f_{OSC}$ [$88/f_{OSC}$], T1/T = 4/11
5	No Pulse (same to D0~D9)
6	$T=1/f_{PUL} = 12/f_{OSC}$ [$96/f_{OSC}$], T1/T = 1/4
7	No pulse (same to D0 ~ D9)

* Default value is "0"
* [ ] means the value of "T", when Instruction cycle is $f_{OSC}/48$ in MHz version

Table 2-2 PMR selection table

Initial Reset Circuit

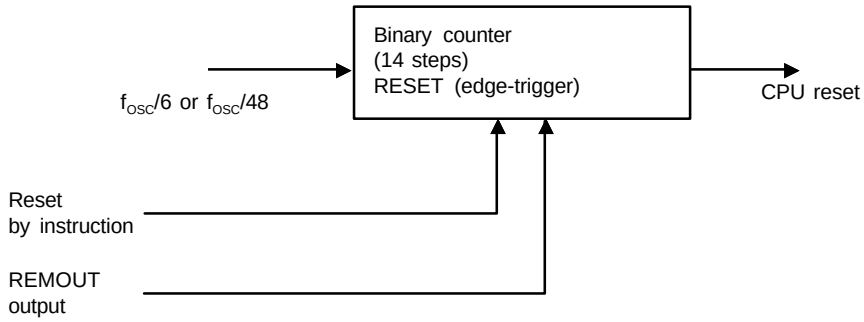
$\overline{\text{RESET}}$ pin must be down to "L" more than 4 machine cycle by outside capacitor or other for power on reset.
The mean of 1 machine cycle is $6/f_{OSC}$ or $48/f_{OSC}$, however, operating voltage must be in recommended operating conditions, and clock oscillating stability.
* It is required to adjust C value depending on rising time of power supply.
(Example shows the case of rising time shorter than 10ms.)



Watch Dog Timer (WDT)

Watch dog timer is organized binary of 14 steps. The signal of $f_{OSC}/6$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized.
The overflow time is $6 \times 2^{13}/f_{OSC}$ (108.026ms at f_{OSC}=455KHz.)
$8 \times 6 \times 2^{13}/f_{OSC}$ (108.026ms at f_{OSC} = 3.64MHz)
Normally, the binary counter must be reset before the overflow by using reset instruction (WDTR) or / and REMOUT port HIGH(Y-reg=8, So instruction execution).

* It is constantly reset in STOP mode. When STOP is released, counting is restarted. (Refer to 2-9 STOP function>)



STOP Operation

Stop mode can be achieved by STOP instructions.

In stop mode :

1. Oscillator is stopped, the operating current is low.
2. Watch dog timer is reset, D8~D9 output and REMOUT output are "L".
3. Part other than WDT, D8~D9 output and REMOUT output have a value before come into stop mode.

Stop mode is released when one of K or R input is going to "L".

1. State of D0~D7 output and REMOUT output is return to state of before stop mode is achieved.
2. After 1,024¡¿8 enable clocks for stable oscillating, First instruction start to operate.
3. In return to normal operation, WDT is counted from zero again.

But, at executing stop instruction, if one of K or R input is chosen to "L", stop instruction is same to NOP instruction.

Port Operation

Value of X-reg	Value of X-reg	Operation
0 or 1	0 ~ 7	S0 : D(Y) ¡ç 1, R0 : D(Y) ¡ç 0
0 or 1	8	REMOUT port repeats "H" and "L" in pulse frequency. (When PMR = 5, it is fixed at "H") S0 : REMOUT(PMR) ¡ç 1 R0 : REMOUT(PMR) ¡ç 0
0 or 1	9	S0 : D0 ~ D9 ¡ç 1 (High-Z) R0 : D0 ~ D9 ¡ç 0
0 or 1	A ~ D	S0 : R(Y-Ah) ¡ç 1 R0 : R(Y-Ah) ¡ç 0
0 or 1	E	S0 : R0 ~ R3 ¡ç 1 R0 : R0 ~ R3 ¡ç 0
0 or 1	F	S0 : D0 ~ D9 ¡ç 1, R0 ~ R3 ¡ç 1 R0 : D0 ~ D9 ¡ç 0, R0 ~ R3 ¡ç 0
2 or 3	0	S0 : D(8) ¡ç 1 R0 : D(8) ¡ç 0
2 or 3	1	S0 : D(9) ¡ç 1 R0 : D(9) ¡ç 0

CHAPTER 3. Instruction

Instruction Table

The GMS34XXXT series provides the following 43 basic instructions.

	Category	Mnemonic	Function	ST*1
1	Register to Register	LAY	A ¡ç Y	S
2		LYA	Y ¡ç A	S
3		LAZ	A ¡ç 0	S
4	RAM to Register	LMA	M(X,Y) ¡ç A	S
5		LMAIY	M(X,Y) ¡ç A, Y ¡ç Y+1	S
6		LYM	Y ¡ç M(X,Y)	S
7		LAM	A ¡ç M(X,Y)	S
8		XMA	A ¡ê M(X,Y)	S
9	Immediate	LYI i	Y ¡ç i	S
10		LMIIY i	M(X,Y) ¡ç i, Y ¡ç Y+1	S
11		LXI n	X ¡ç n	S
12	RAM Bit Manipulation	SEM n	M(n) ¡ç 1	S
13		REM n	M(n) ¡ç 0	S
14		TM n	TEST M(n) = 1	E
15	ROM Address	BR a	if ST = 1 then Branch	S
16		CAL a	if ST = 1 then Subroutine call	S
17		RTN	Return from Subroutine	S
18		LPBI i	PB ¡ç i	S
19	Arithmetic	AM	A ¡ç A + M(X,Y)	C
20		SM	A ¡ç M(X,Y) - A	B
21		IM	A ¡ç M(X,Y) + 1	C
22		DM	A ¡ç M(X,Y) - 1	B
23		IA	A ¡ç A + 1	S
24		IY	Y ¡ç Y + 1	C
25		DA	A ¡ç A - 1	B

	Category	Mnemonic	Function	ST*1
26	Arithmetic	DY	Y ¡ç Y - 1	B
27		EORM	A ¡ç A ⊕ M (X,Y)	S
28		NEGA	A ¡ç $\overline{A}$ + 1	Z
29	Comparison	ALEM	TEST A ¡Â M(X,Y)	E
30		ALEI i	TEST A ¡Â i	E
31		MNEZ	TEST M(X,Y) ¡Á 0	N
32		YNEA	TEST Y ¡Á A	N
33		YNEI i	TEST Y ¡Á i	N
34		KNEZ	TEST K ¡Á 0	N
35		RNEZ	TEST R ¡Á 0	N
36	Input / Output	LAK	A ¡ç K	S
37		LAR	A ¡ç R	S
38		SO	Output(Y) ¡ç 1*2	S
39		RO	Output(Y) ¡ç 0*2	S
40	Control	WDTR	Watch Dog Timer Reset	S
41		STOP	Stop operation	S
42		LPY	PMR ¡ç Y	S
43		NOP	No operation	S

Note) i = 0~f, n = 0~3, a = 6bit PC Address

*1 Column ST indicates conditions for changing status. Symbols have the following meanings

S : On executing an instruction, status is unconditionally set.
C : Status is only set when carry or borrow has occurred in operation.
B : Status is only set when borrow has not occurred in operation.
E : Status is only set when equality is found in comparison.
N : Status is only set when equality is not found in comparison.
Z : Status is only set when the result is zero.

*2 Operation is settled by a value of Y-register.

CHAPTER 4. EPROM

GMS34004TK / 34112TK / 34140TK

Mode define

Item		Device operation	Mode setting		
User mode		Exact User pgm	RESETB = 0 ~ 3V		Vcc=3V
EPROM read mode		Address in, Data out	RESETB =12.5V	K3~0=0110	Vcc=6.0V
EPROM Program mode	1Byte PGM Write	Address in, Data in	RESETB =12.5V	K3~0=0110	Vcc=6.0V
	2Byte PGM Write	Address in, Data in		K3~0=0111	
	Program verify	Address in, Data out		-	
Lock bit Program mode	Lock bit Write	Lock bit write(set D5 to 1)	RESETB =12.5V	K3~0=0100	Vcc=6.0V, Lock bit is D5. (Default : unlock)
	Lock bit Read	Lock bit out		K3~0=0101	

Port define

Port Name	User Mode	EPROM Mode			
VDD	3.0V	6.0V			
RESETB	Reset (0, 3.0V)	Vpp (0, 12.5V)			
OSC1	Clock input	Clock input			
K0	K0(Input)	Read / Write Control Address / Data Control			
K1	K1(Input)				
K2	K2(Input)				
K3	K3(Input)				
D0	D0(Output)	A0	A5	Da0	Da4
D1	D1(Output)	A1	A6	Da1	Da5
D2	D2(Output)	A2	A7	Da2	Da6
D3	D3(Output)	A3	A8	Da3	Da7
D4	D4(Output)	A4	A9	-	-
D5	D5(Output)	Lock bit output			
GND	0V				

NMOS open drain I/O in EPROM mode

* Undefined ports in this table are N.C (No Connection)

Programming data

Device Name	ROM Size	Blank data (HEX)	Lock bit	Device address	File address
GMS34004TK	512bytes	FF	Yes	0000 ~ 01FF	0000 ~ 01FF
GMS34112TK	1,024bytes	FF	Yes	0000 ~ 03FF	0000 ~ 03FF
GMS34140TK	1,024bytes	FF	Yes	0000 ~ 03FF	0000 ~ 03FF

- If lock bit is set, the EPROM of the device can not be read, because output is always FF.
- Input file : Intel Hexa format (*.RHX)

Write / Read data conversion

- You must change MSB ~ LSB ¡ê LSB ~ MSB.
- Example

File / buffer data

Hex	Binary (MSB~LSB)
2C	0010 1100
E4	1110 0100
8D	1000 1101

Write

Read

Device (D3 ~ D0)

Hex	Binary (MSB~LSB)
34	0011 0100
27	0010 0111
B1	1011 0001

Checksum

- It is calculated from the Buffer of the programmer.
- Address range is the same as device address.
- Calculate method is the same as normal EPROM devices (ex:27C128, 256 etc)

Programming control

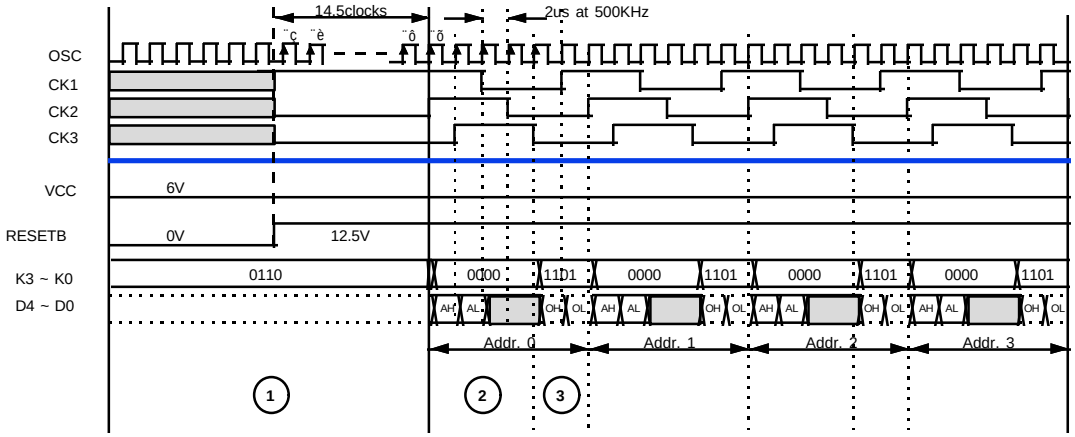
- OSC1 & RESETB control OTP device, so you must count OSC1 clocks in every state.
- K ports control the internal state of the OTP device(ex: Read, Write...).
- D5~D0 ports are NMOS open drain I/O in EPROM mode.
  It must be pulled up by resistors (about 4.7~ 47K ohm).
- The frequency rate of the OSC1 clock is 10KHz ~ 500KHz.
  You can hold OSC1 HIGH or LOW state when you need.

Programming DC specification

Item	Range
VCC	0 ~ 6.0V ¡¾ 0.25V
RESETB	0 ~ 12.5V ¡¾ 0.5V
K-port	0 ~ 0.2VCC(Low)
D-port	0.8VCC ~ VCC (High)

EPROM read mode (1/2)

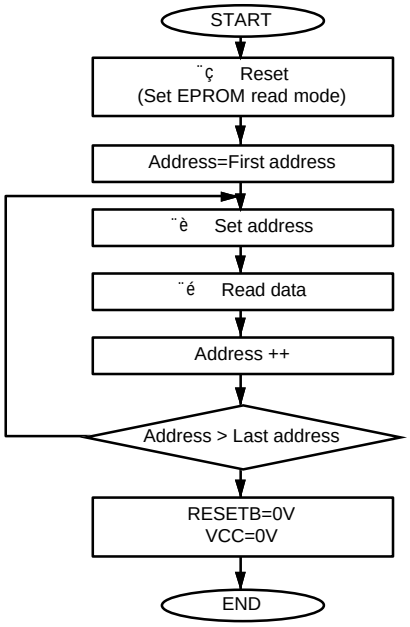
For device verify or read.
If you set Lock bit, output data is always FF.



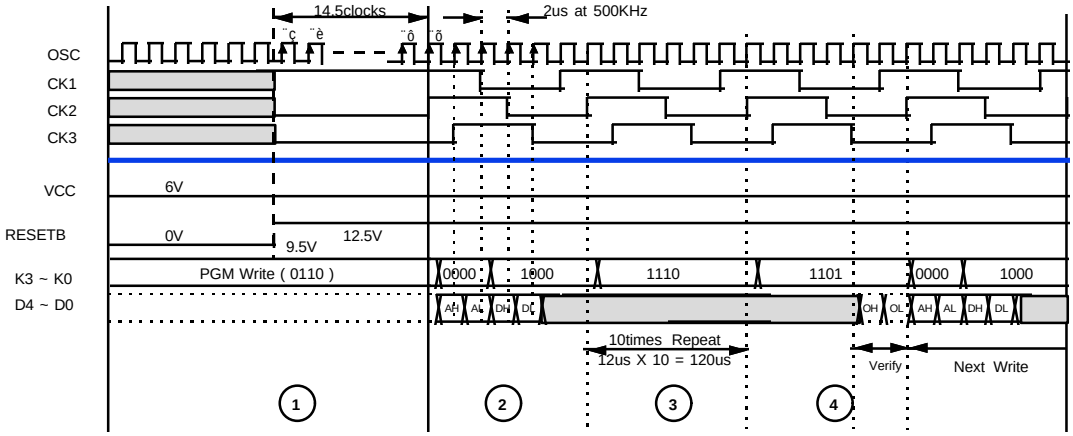
AH : High Address (A9~5) Input Latch
AL : Low Address (A4~0) Input Latch
OH : High Data (D7~4) Output
OL : Low Data (D3~0) Output

* Note : 1. AH, AL, DH, DL Inputs released at 100~200nS after OSC rising edge and width is 1OSC cycle (if OSC is 500KHz, width is 2uS).

EPROM read mode (2/2)



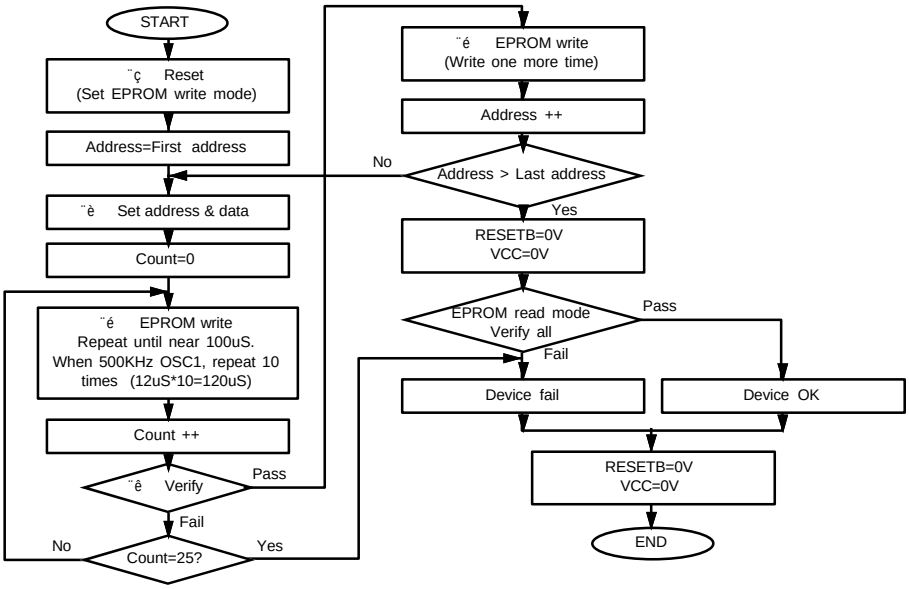
EPROM write mode (1/2)



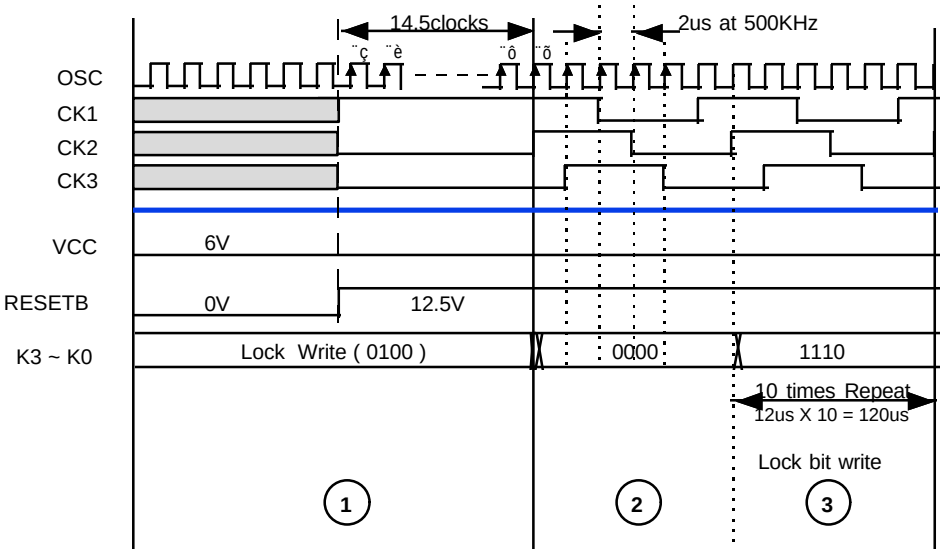
AH : High bit Address Input Latch
AL : Low bit Address Input Latch
DH : High bit Data Input Latch
DL : Low bit Data Input Latch
OH : High bit Data Output
OL : Low bit Data Output

* Note : 1. AH, AL, DH, DL Inputs are released at 100~200nS after OSC rising edge and width is 1OSC cycle (if OSC is 500KHz, width is 2uS).

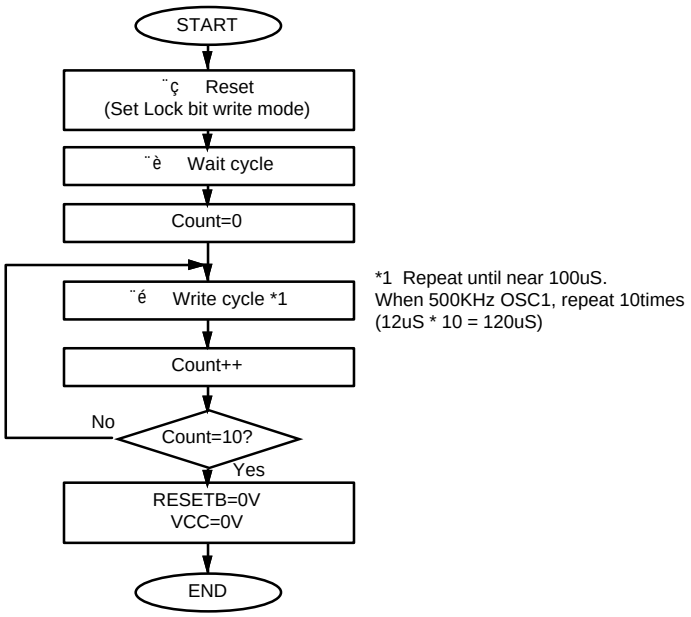
EPROM write mode (2/2)



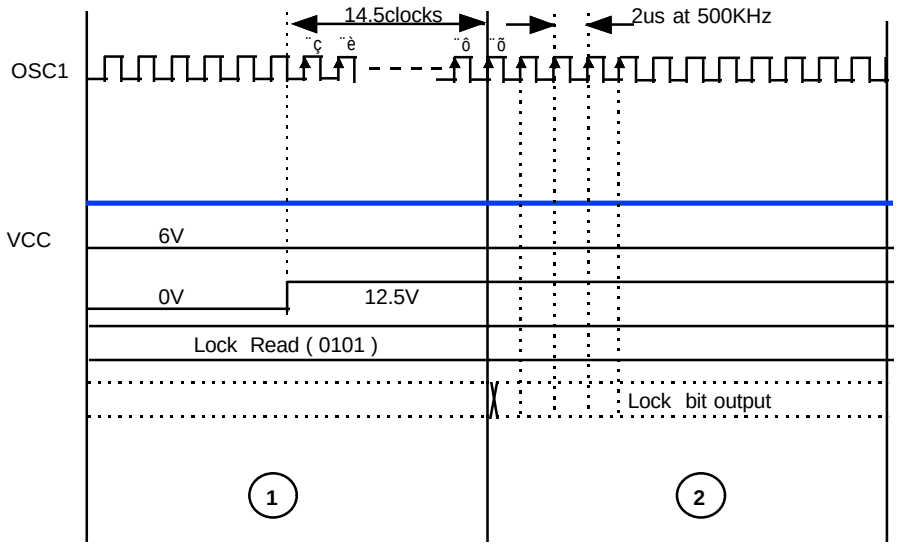
Lock bit write mode (1/2)



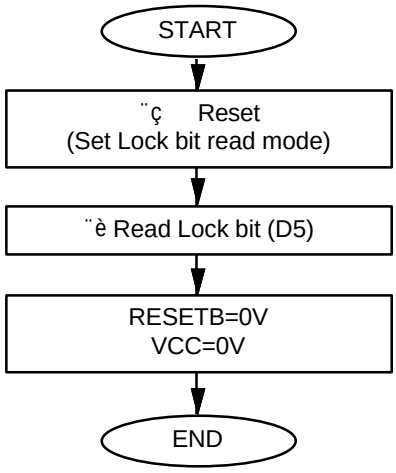
Lock bit write mode (2/2)



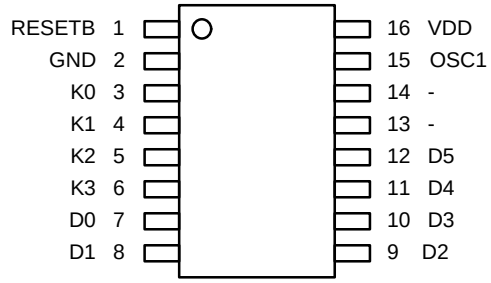
Lock bit read mode (1/2)



Lock bit read mode (2/2)

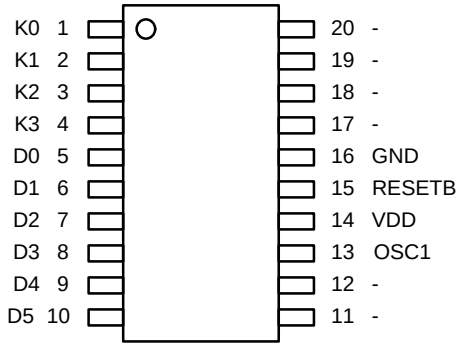


GMS34004T/112T/140T (Pin assignment & Package)



16DIP (Standard TTL DIP Size)

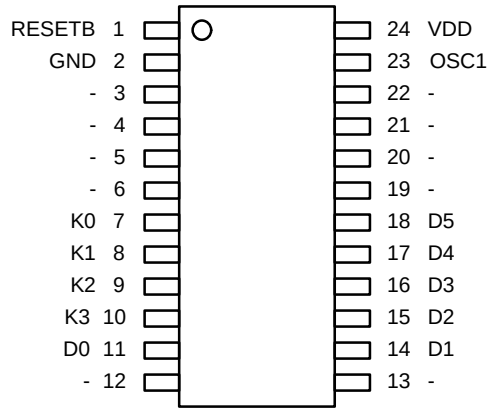
- Width 300mil
- Pin to pin 100mil



20DIP (Standard TTL DIP Size)

- Width 300mil
- Pin to pin 100mil

20SOP (Standard TTL SOP Size)



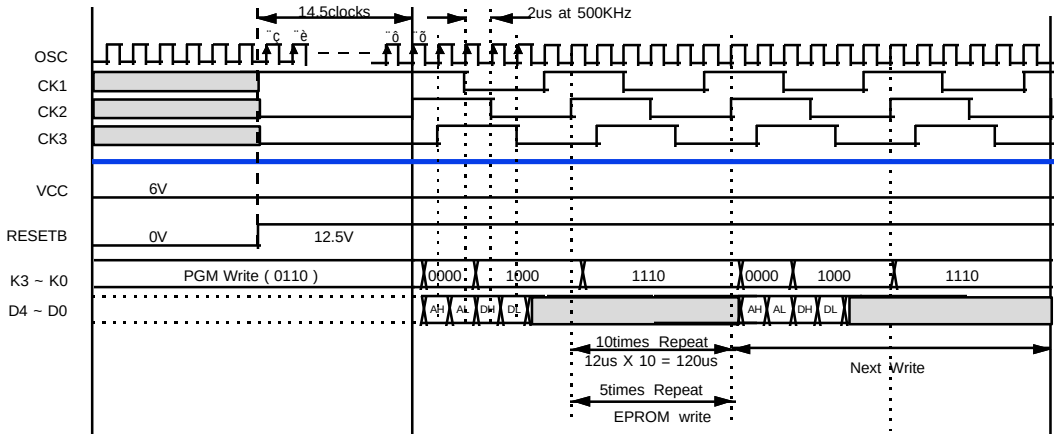
24DIP (Skinny DIP Size)

- Width 300mil
- Pin to pin 100mil

24SOP (Standard SOP Size)

EPROM(KHz) mode

EPROM write only mode



GMS34004TM / 34112TM / 34140TM

Mode define

Item		Device operation	Mode setting		
User mode		Execute User pgm	RESETB = 0 ~ 3V		Vcc=3V
EPROM read mode		Address in, Data out	RESETB =12.5V	K3~0=0010	Vcc=6.0V
EPROM Program mode	1Byte PGM Write	Address in, Data in	RESETB =12.5V	K3~0=0110	Vcc=6.0V
	2Byte PGM Write	Address in, Data in		K3~0=0111	
	Program verify	Address in, Data out		-	
Lock bit Program mode	Lock bit Write	Lock bit write(set D5 to 1)	RESETB =12.5V	K3~0=0100	Vcc=6.0V, Lock bit is D5. (Default : unlock)
	Lock bit Read	Lock bit out		K3~0=0101	

Port define

Port Name	User Mode	EPROM Mode			
VDD	3.0V	6.0V			
RESETB	Reset (0, 3.0V)	Vpp (0, 12.5V)			
OSC1	Clock input	Clock input			
K0	K0(Input)	Read / Write Control Address / Data Control			
K1	K1(Input)				
K2	K2(Input)				
K3	K3(Input)				
D0	D0(Output)	A0	A5	Da0	Da4
D1	D1(Output)	A1	A6	Da1	Da5
D2	D2(Output)	A2	A7	Da2	Da6
D3	D3(Output)	A3	A8	Da3	Da7
D4	D4(Output)	A4	A9	-	-
D5	D5(Output)	Lock bit output			
GND	0V				

NMOS open drain I/O in EPROM mode

* Undefined ports in this table are N.C (No Connection)

Programming data

Device Name	ROM Size	Blank data (HEX)	Lock bit	Device address	File address
GMS34004TK	512bytes	FF	Yes	0000 ~ 01FF	0000 ~ 01FF
GMS34112TK	1,024bytes	FF	Yes	0000 ~ 03FF	0000 ~ 03FF
GMS34140TK	1,024bytes	FF	Yes	0000 ~ 03FF	0000 ~ 03FF

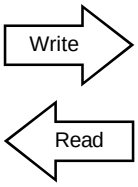
- If lock bit is set, the EPROM of the device can not be read, because output is always FF.
- Input file : Intel Hexa format (*.RHX)

Write / Read data conversion

- You must change MSB ~ LSB ¡ê LSB ~ MSB.
- Example

File / buffer data

Hex	Binary (MSB~LSB)
2C	0010 1100
E4	1110 0100
8D	1000 1101



Device (D3 ~ D0)

Hex	Binary (MSB~LSB)
34	0011 0100
27	0010 0111
B1	1011 0001

Checksum

- It is calculated from the Buffer of the programmer.
- Address range is the same as device address.
- Calculate mathod is the same as normal EPROM devices (ex:27C128, 256 etc)

Programming control

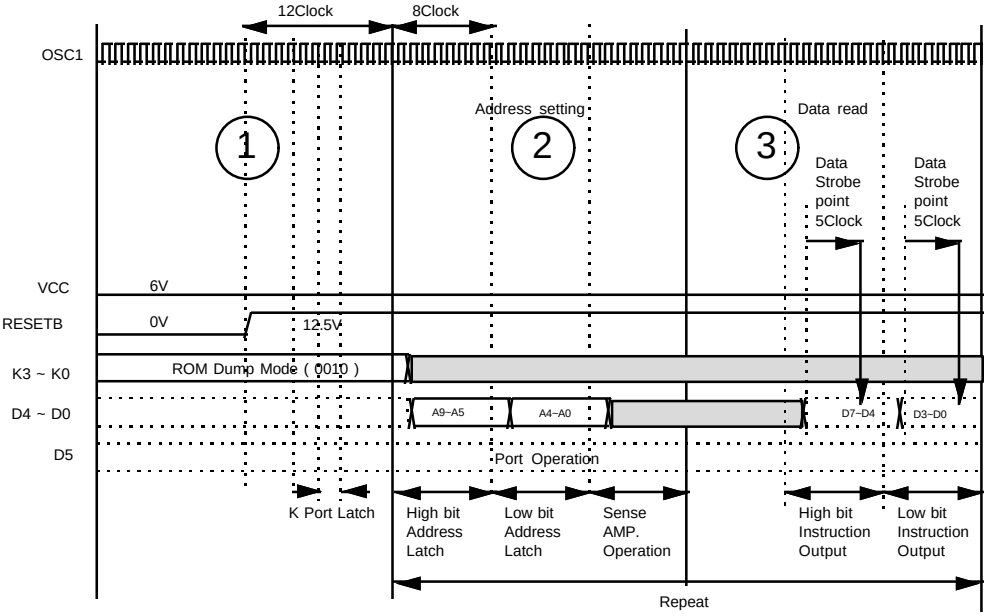
- OSC1 & RESETB control OTP device, so you must count OSC1 clocks in every state.
- K ports control the internal state of the OTP device(ex: Read, Write...).
- D5~D0 ports are NMOS open drain I/O in EPROM mode.
  It must be pulled up by resistors (about 4.7~ 47K ohm).
- The frequency rate of the OSC1 clock is 10KHz ~ 500KHz.
  You can hold OSC1 HIGH or LOW state when you need.

Programming DC specification

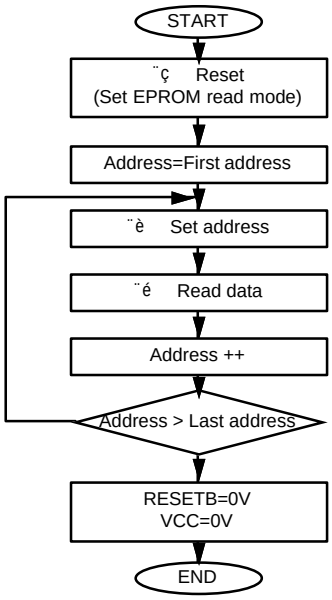
Item	Range
VCC	0 ~ 6.0V ¡¾ 0.25V
RESETB	0 ~ 12.5V ¡¾ 0.5V
K-port	0 ~ 0.2VCC(Low)
D-port	0.8VCC ~ VCC (High)

EPROM read mode (1/2)

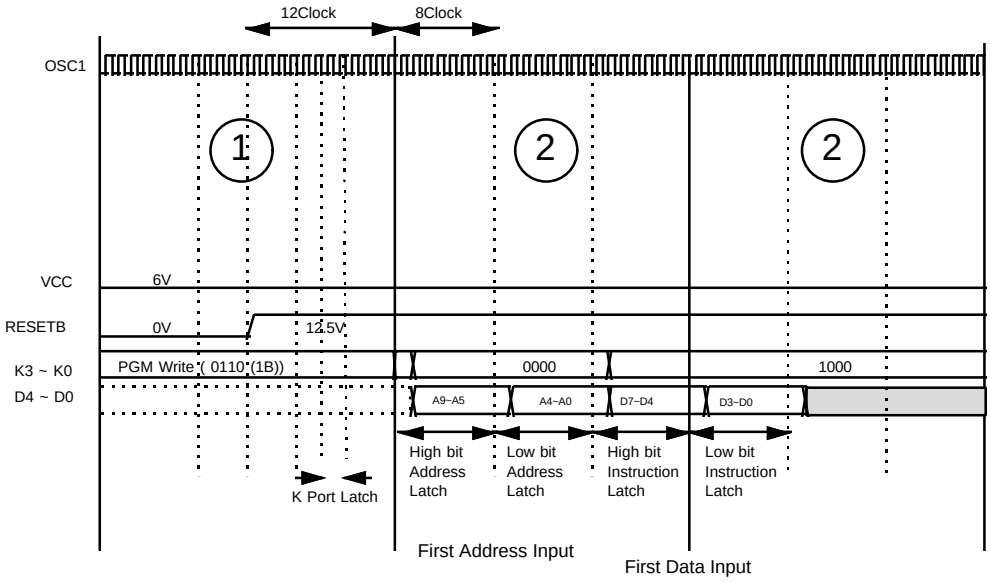
For device verify or read.
If you set Lock bit, output data is all 'FF'



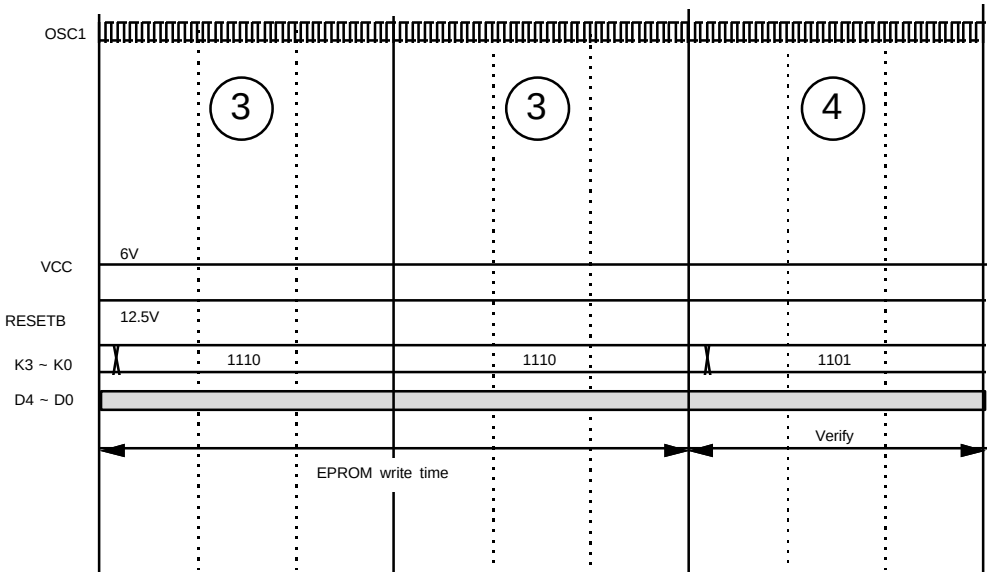
EPROM read mode (2/2)



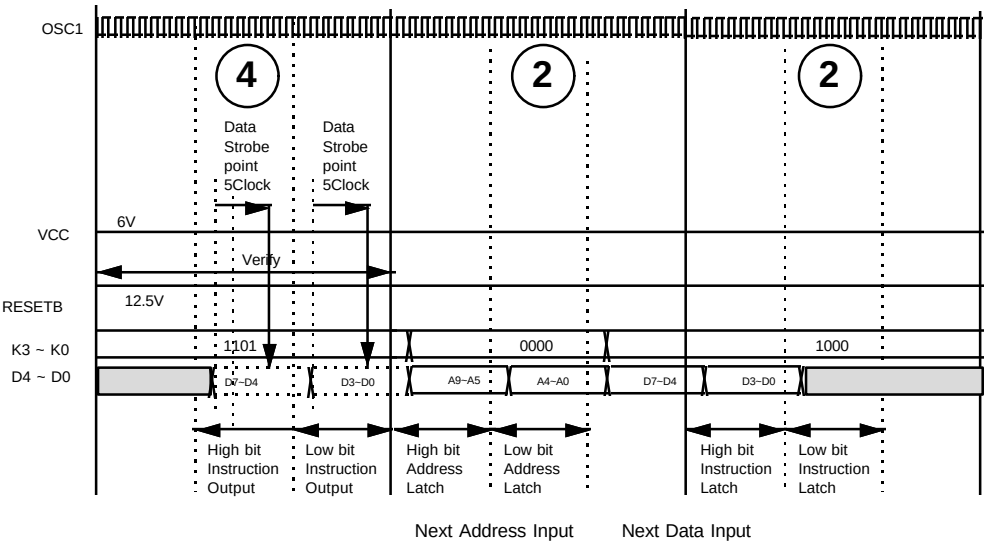
EPROM write mode (1/4)



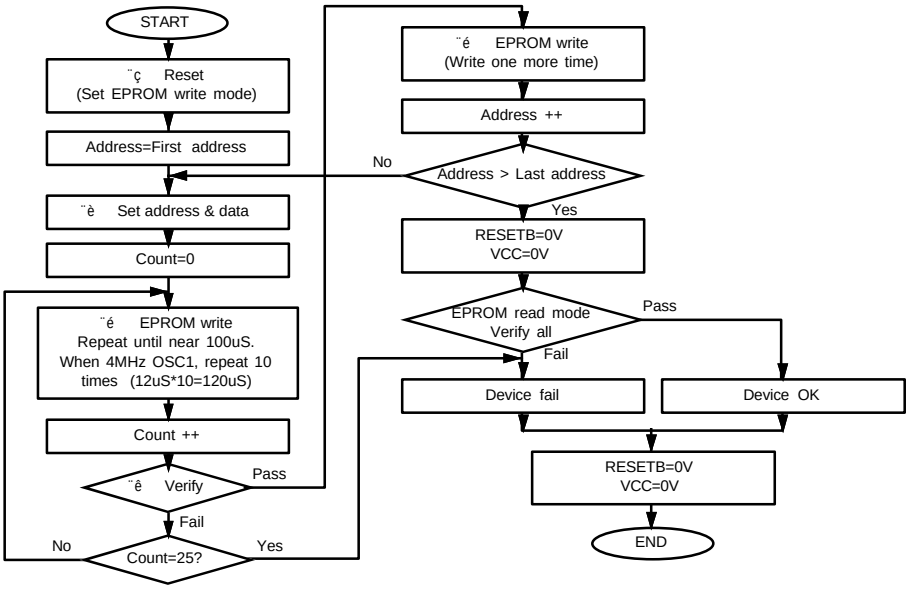
EPROM write mode (2/4)



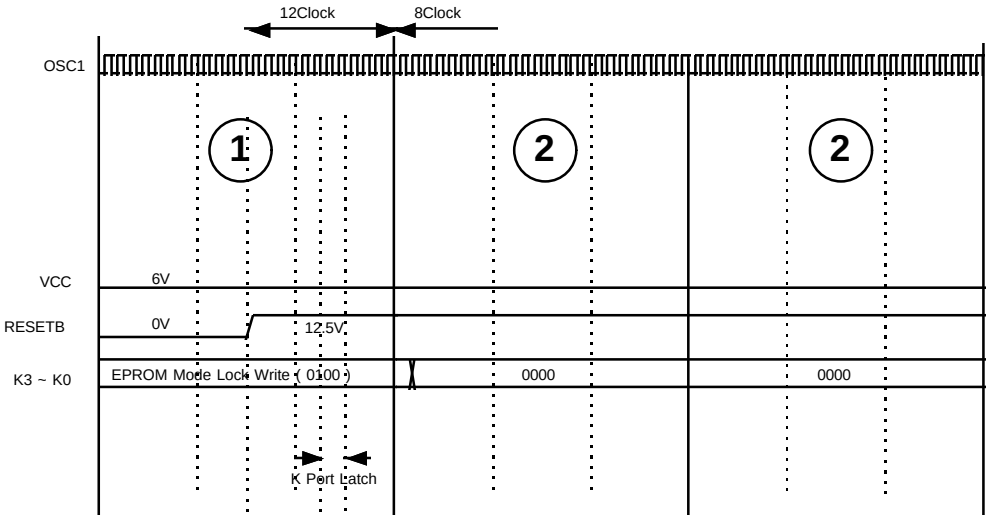
EPROM write mode (3/4)



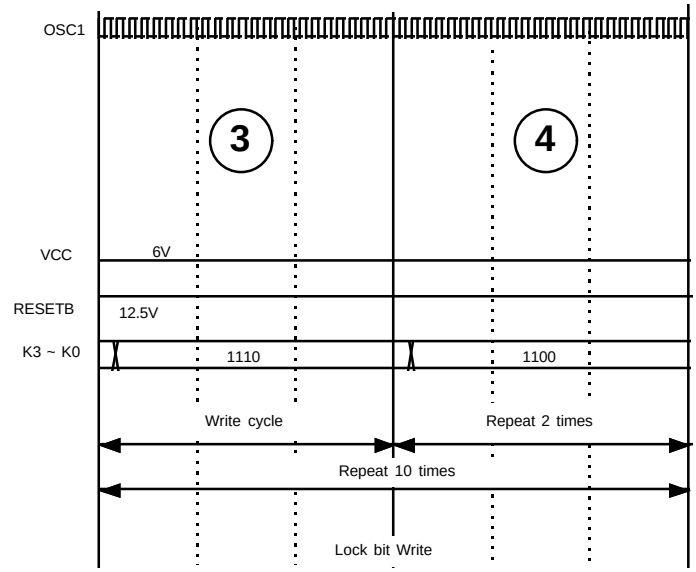
EPROM write mode (4/4)



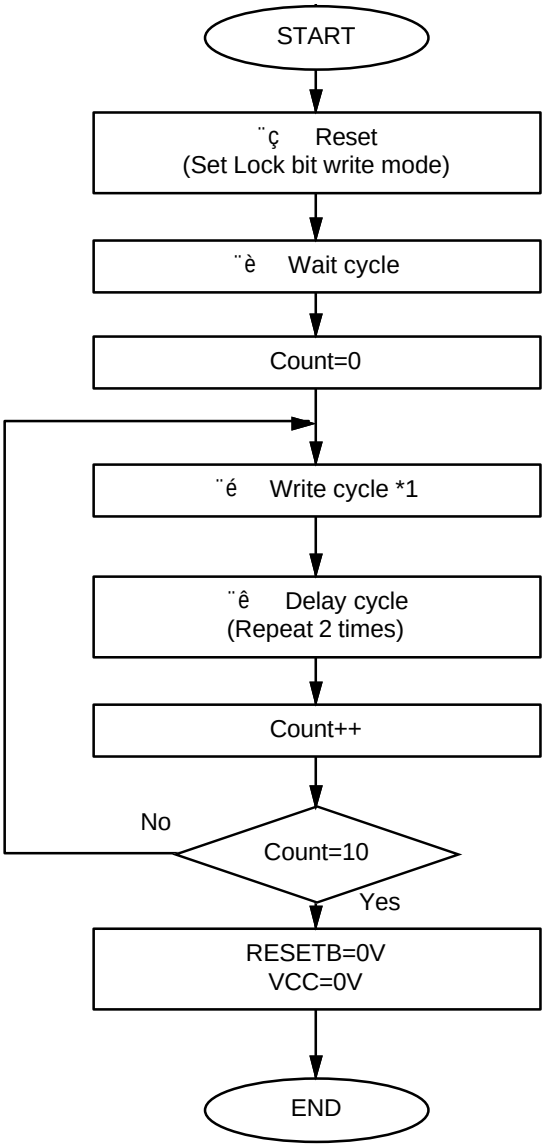
Lock bit write mode (1/3)



Lock bit write mode (2/3)

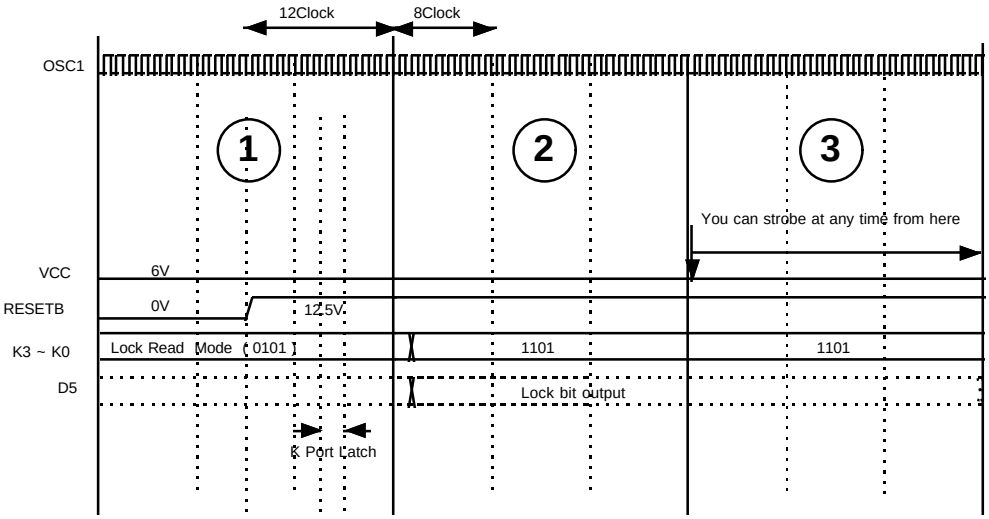


Lock bit write mode (3/3)



*1 Repeat until near 100uS.
When 4MHz OSC1, repeat 10 times
(12uS * 10 = 120uS)

Lock bit read mode (1/2)



Lock bit read mode (2/2)