



## GENERAL DESCRIPTION



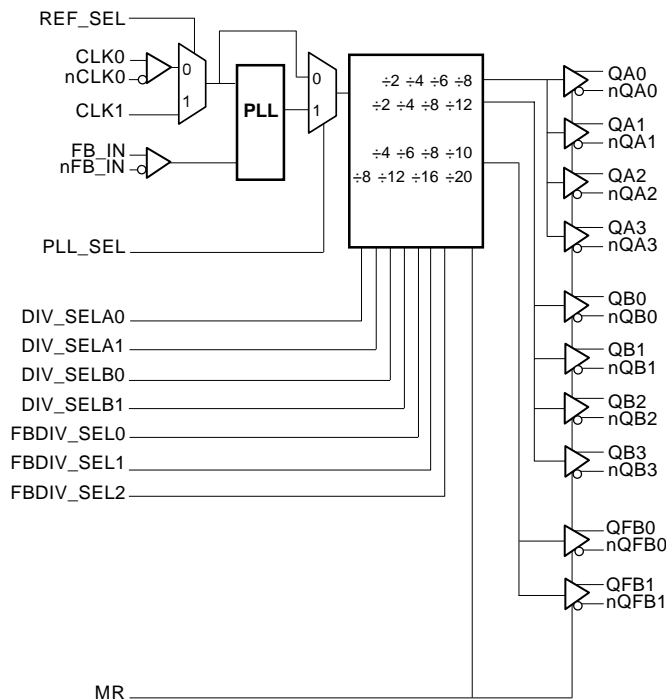
The ICS8732-01 is a low voltage, low skew, 3.3V LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8732-01 has two selectable clock inputs. The CLK0, nCLK0 pair can accept most standard differential input levels. The single ended clock input accepts LVCMOS or LVTTTL input levels. The ICS8732-01 has a fully integrated PLL along with frequency configurable outputs. An external feedback input and outputs regenerate clocks with “zero delay”.

The ICS8732-01 has multiple divide select pins for each bank of outputs along with 3 independent feedback divide select pins allowing the ICS8732-01 to function both as a frequency multiplier and divider. The PLL\_SEL input can be used to bypass the PLL for test and system debug purposes. In bypass mode, the input clock is routed around the PLL and into the internal output dividers.

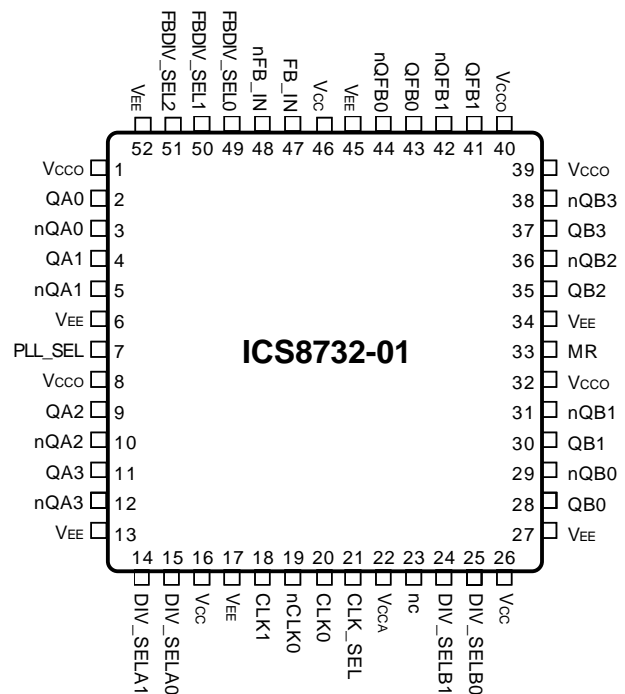
## Features

- 10 differential 3.3V LVPECL outputs
- Selectable differential CLK0, nCLK0 or LVCMOS/LVTTTL CLK1 inputs
- CLK0, nCLK0 supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK1 accepts the following input levels: LVCMOS or LVTTTL
- Maximum output frequency: 350MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Cycle-to-cycle jitter: CLK0, nCLK0, 50ps (maximum)  
CLK1, 80ps (maximum)
- Output skew: 150ps (maximum)
- Static phase offset: -150ps to 150ps
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**52-Lead LQFP**  
10mm x 10mm x 1.4mm package body  
**Y package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 8, 32, 39, 40	V <sub>CCO</sub>	Power		Output supply pins.
2, 3, 4, 5	QA0, nQA0, QA1, nQA1	Output		Differential output pair. LVPECL interface levels.
6, 13, 17, 27, 34, 45, 52	V <sub>EE</sub>	Power		Negative supply pins.
7	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTTL interface levels.
9, 10, 11, 12	QA2, nQA2, QA3, nQA3	Output		Differential output pairs. LVPECL interface levels.
14	DIV_SELA1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
15	DIV_SELA0	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
16, 26, 46	V <sub>CC</sub>	Power		Core supply pins.
18	CLK1	Input	Pulldown	LVCMOS / LVTTTL reference clock input.
19	nCLK0	Input	Pullup	Inverting differential clock input.
20	CLK0	Input	Pulldown	Non-inverting differential clock input.
21	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects CLK0, nCLK0. When HIGH, selects CLK1. LVCMOS / LVTTTL interface levels.
22	V <sub>CCA</sub>	Power		Analog supply pin.
23	nc	Unused		No connect.
24	DIV_SELB1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
25	DIV_SELB0	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
28, 29, 30, 31	QB0, nQB0, QB1, nQB1	Output		Differential output pairs. LVPECL interface levels.
33	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
35, 36, 37, 38	QB2, nQB2, QB3, nQB3	Output		Differential output pairs. LVPECL interface levels.
41, 42, 43, 44	QFB1, nQFB1, QFB0, nQFB0	Output		Differential feedback output pairs. LVPECL interface levels.
47	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
48	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
49	FBDIV_SEL0	Input	Pulldown	Selects divide value for differential feedback output pairs. LVCMOS / LVTTTL interface levels.
50	FBDIV_SEL1	Input	Pulldown	Selects divide value for differential feedback output pairs. LVCMOS / LVTTTL interface levels.
51	FBDIV_SEL2	Input	Pulldown	Selects divide value for differential feedback output pairs. LVCMOS / LVTTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.



**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLUP}$	Input Pullup Resistor			51		K $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		K $\Omega$

**TABLE 3A. CONTROL INPUT FUNCTION TABLE FOR QA0:QA3 OUTPUTS**

Inputs				Outputs
MR	PLL_SEL	DIV_SELA1	DIV_SELA0	QA0:QA3, nQA0:nQA3
1	X	X	X	Low
0	1	0	0	fVCO/2
0	1	0	1	fVCO/4
0	1	1	0	fVCO/6
0	1	1	1	fVCO/8
0	0	0	0	fREF_CLK/2
0	0	0	1	fREF_CLK/4
0	0	1	0	fREF_CLK/6
0	0	1	1	fREF_CLK/8

**TABLE 3B. CONTROL INPUT FUNCTION TABLE FOR QB0:QB3 OUTPUTS**

Inputs				Outputs
MR	PLL_SEL	DIV_SELB1	DIV_SELB0	QB0:QB3, nQB0:nQB3
1	X	X	X	Low
0	1	0	0	fVCO/2
0	1	0	1	fVCO/4
0	1	1	0	fVCO/8
0	1	1	1	fVCO/12
0	0	0	0	fREF_CLK/2
0	0	0	1	fREF_CLK/4
0	0	1	0	fREF_CLK/8
0	0	1	1	fREF_CLK/12



**TABLE 3C. CONTROL INPUT FUNCTION TABLE FOR QFB0, QFB1**

Inputs					Outputs
MR	PLL_SEL	FBDIV_SEL2	FBDIV_SEL1	FBDIV_SEL0	QFB0, QFB1 nQFB0, nQFB1
1	X	X	X	X	Low
0	1	0	0	0	fVCO/4
0	1	0	0	1	fVCO/6
0	1	0	1	0	fVCO/8
0	1	0	1	1	fVCO/10
0	1	1	0	0	fVCO/8
0	1	1	0	1	fVCO/12
0	1	1	1	0	fVCO/16
0	1	1	1	1	fVCO/20
0	0	0	0	0	fREF_CLK/4
0	0	0	0	1	fREF_CLK/6
0	0	0	1	0	fREF_CLK/8
0	0	0	1	1	fREF_CLK/10
0	0	1	0	0	fREF_CLK/8
0	0	1	0	1	fREF_CLK/12
0	0	1	1	0	fREF_CLK/16
0	0	1	1	1	fREF_CLK/20

**TABLE 4A. QX OUTPUT FREQUENCY w/FB\_IN = QFB0 OR QFB1**

Inputs							fVCO
FB_IN	FBDIV_SEL2	FBDIV_SEL1	FBDIV_SEL0	Output Divider Mode	CLK1 (MHz)		(NOTE 1)
					Minimum	Maximum	
QFB	0	0	0	÷4	62.5	175 (NOTE 2)	fREF_CLK x 4
QFB	0	0	1	÷6	41.67	116.67	fREF_CLK x 6
QFB	0	1	0	÷8	31.25	87.5	fREF_CLK x 8
QFB	0	1	1	÷10	25	70	fREF_CLK x 10
QFB	1	0	0	÷8	31.25	87.5	fREF_CLK x 8
QFB	1	0	1	÷12	20.83	58.33	fREF_CLK x 12
QFB	1	1	0	÷16	15.62	43.75	fREF_CLK x 16
QFB	1	1	1	÷20	12.5	35	fREF_CLK x 20

NOTE 1: VCO frequency range is 250MHz to 700MHz.

NOTE 2: The maximum input frequency that the phase detector can accept is 200MHz.



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	42.3°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 5A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				165	mA
$I_{CCA}$	Analog Supply Current; NOTE 1				15	mA

NOTE 1: This parameter is included in the Power Supply Current ( $I_{EE}$ ) value.

**TABLE 5B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	CLK1	2		$V_{CC} + 0.3$	V
		CLK_SEL, PLL_SEL, DIV_SELx, DIV_SELBx, FBDIV_SELx, MR	2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	CLK1	-0.3		1.3	V
		CLK_SEL, PLL_SEL, DIV_SELx, DIV_SELBx, FBDIV_SELx, MR	-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_SEL, MR, CLK1 DIV_SELx, DIV_SELBx, FBDIV_SELx	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL, MR, CLK1 DIV_SELx, DIV_SELBx, FBDIV_SELx	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu A$



**TABLE 5C. DIFFERENTIAL DC CHARACTERISTICS**,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, FB_IN	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK0, nFB_IN	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, FB_IN	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu A$
		nCLK0, nFB_IN	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for FB\_IN, nFB\_IN is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 5D. LVPECL DC CHARACTERISTICS**,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS**,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Reference Frequency				200	MHz

**TABLE 7. AC CHARACTERISTICS**,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				350	MHz
$t(\emptyset)$	Static Phase Offset; NOTE 1	PLL_SEL = 3.3V, $f_{REF} = 100MHz$ , $f_{VCO} = 400MHz$	-150		150	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3, 4				150	ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 3	CLK0, nCLK			50	ps
		CLK1			80	ps
$t_L$	PLL Lock Time				10	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f_{OUT} \leq 175MHz$	48		52	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.

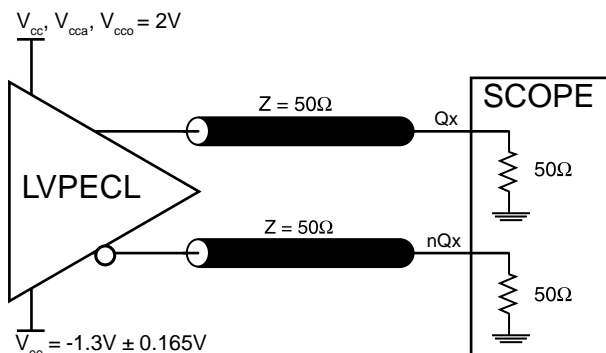
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

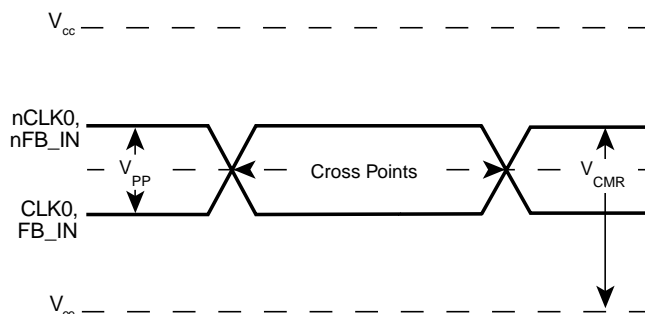
NOTE 4: All outputs in divide by 4 configuration.



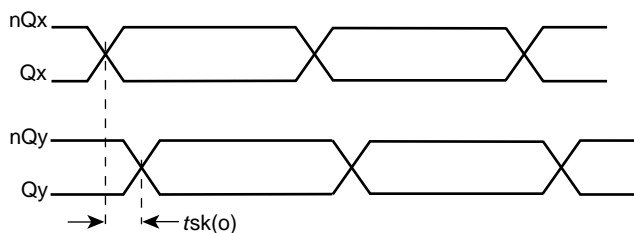
## PARAMETER MEASUREMENT INFORMATION



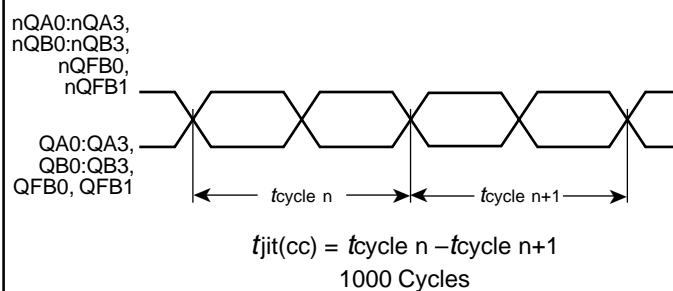
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



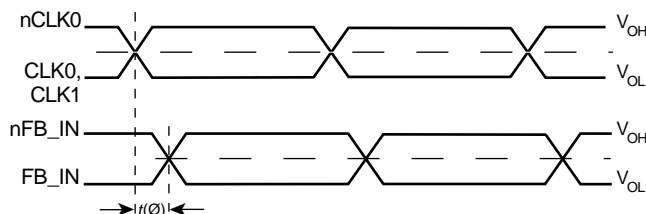
**DIFFERENTIAL INPUT LEVEL**



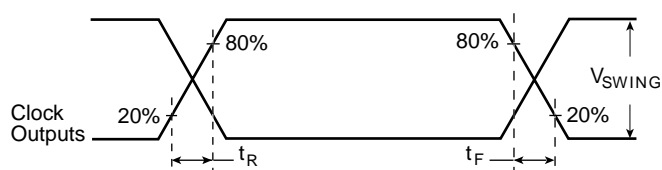
**OUTPUT SKEW**



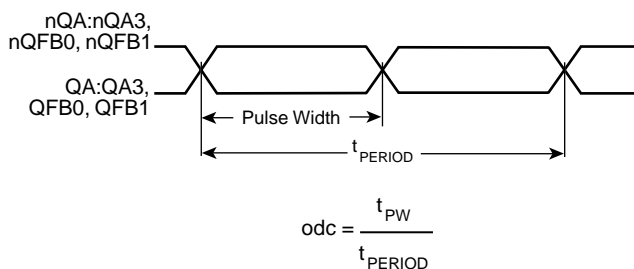
**CYCLE-TO-CYCLE JITTER**



**STATIC PHASE OFFSET**



**OUTPUT RISE/FALL TIME**



**odc &  $t_{PERIOD}$**

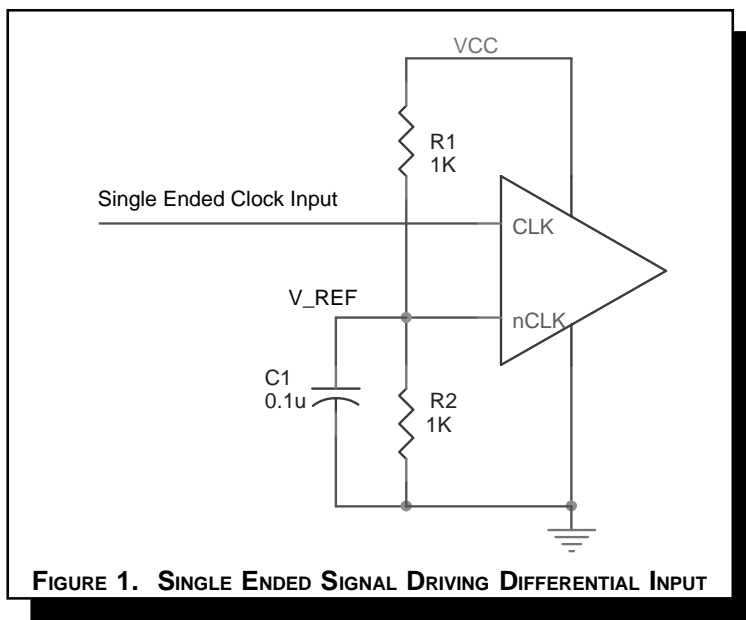


## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

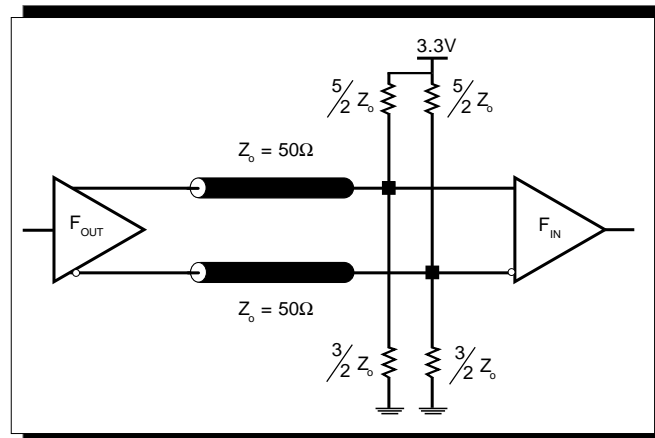
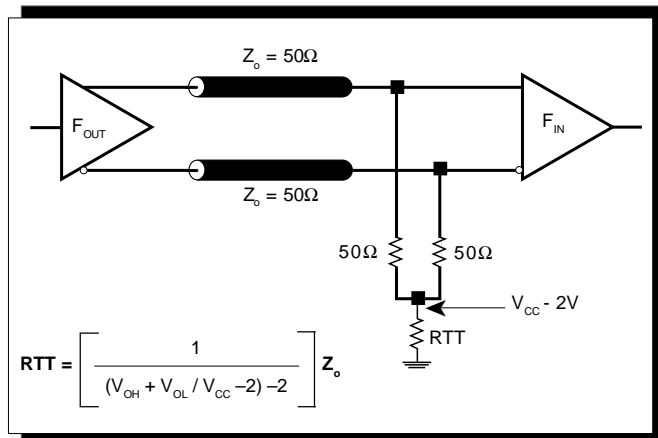


### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

F<sub>OUT</sub> and nF<sub>OUT</sub> are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 2A and 2B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.







## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8732-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$  and  $V_{CCA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

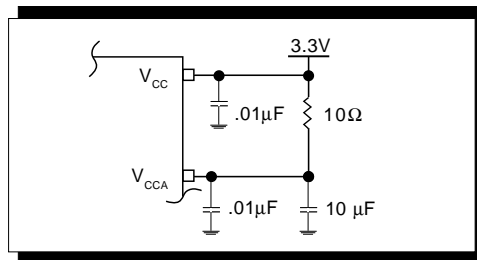


FIGURE 3. POWER SUPPLY FILTERING

## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 4A to 4D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the

driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

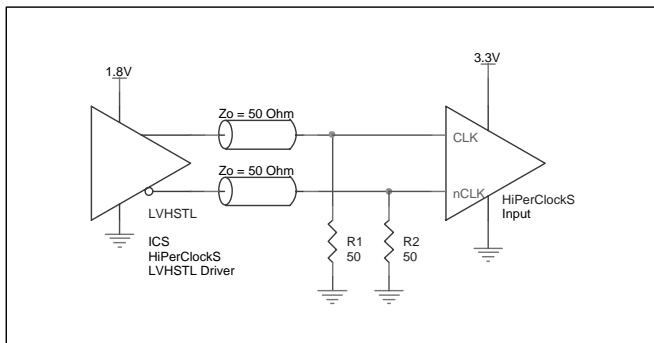


FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

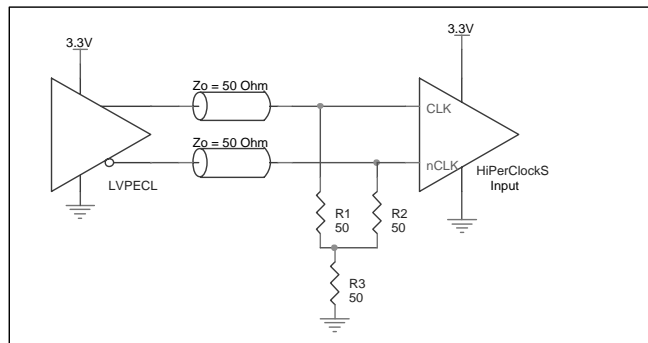


FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

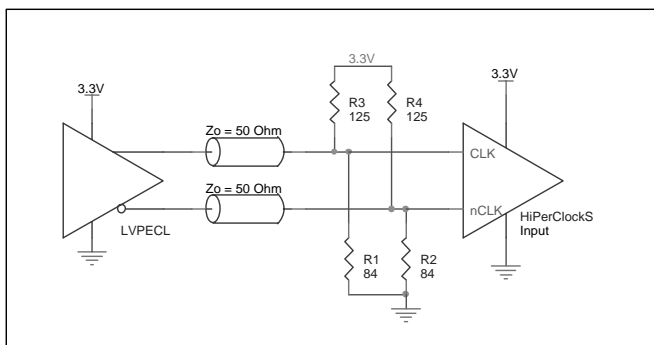


FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

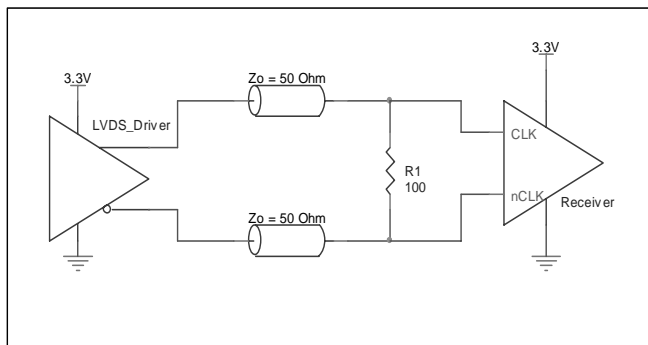


FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8732-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8732-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 165mA = 572mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $10 * 30.2mW = 302mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 572mW + 302mW = 874mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 36.4°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.874W * 36.4^\circ C/W = 102^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 8. Thermal Resistance  $\theta_{JA}$  for 52-pin LQFP, Forced Convection**

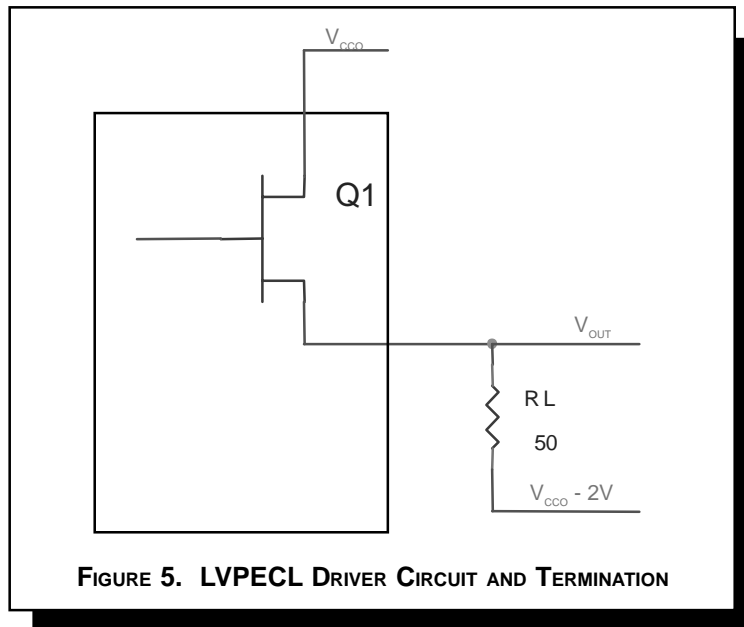
$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 5.



**FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 1.0V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 1.0V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 1V)/50\Omega] * 1V = 20.0mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30.2mW$$



## RELIABILITY INFORMATION

TABLE 9.  $\theta_{JA}$  VS. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8732-01 is: 4916



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## PACKAGE OUTLINE - Y SUFFIX

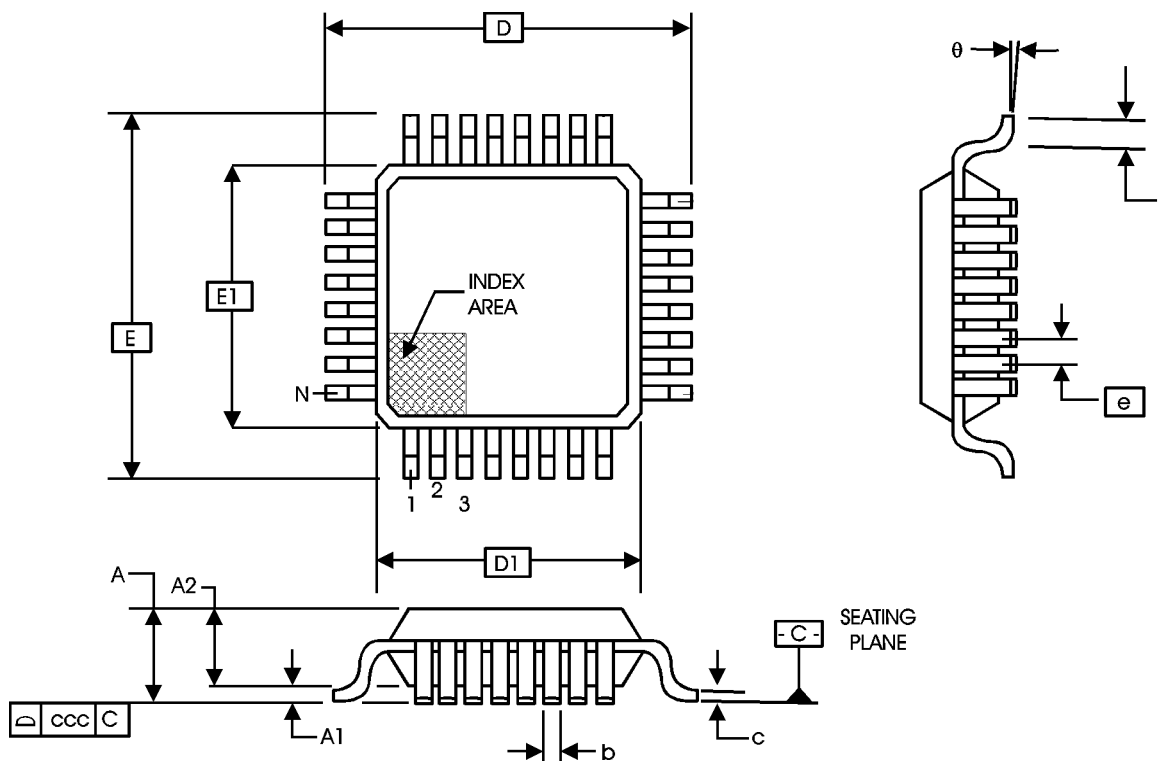


TABLE 10. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	52		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D	12.00 BASIC		
D1	10.00 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
e	0.65 BASIC		
L	0.45	--	0.75
theta	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026



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TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8732AY-01	ICS8732AY-01	52 Lead LQFP	160 per tray	0°C to 70°C
ICS8732AY-01T	ICS8732AY-01T	52 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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## REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T2 T4A	1	Features Section - changed VCO min. from 200MHz to 250MHz.	5/20/03
		3	Pin Characteristics Table - changed $C_{IN}$ from max. 4pF to typical 4pF.	
		4	Qx Output Frequency Table - changed the CLK1 min. column to correlate with the VCO change.	
		5	Absolute Maximum Ratings - changed $V_O$ to $I_O$ and included Continuous Current and Surge Current	
		8	Added <i>Differential Clock Input Interface</i> in the Application Information section.	
C	5A	5	Power Supply DC Characteristics Table - changed IEE from 240mA max. to 165mA max., and ICCA from 14mA max. to 15mA max. Power Considerations - recalculated Power Dissipation and Junction Temperatures to correspond with Table 5A.	6/23/03