SWITCHStAR™ ATM CELL BASED 1.24Gbps NON-BLOCKING INTEGRATED SWITCH CONTROLLER

PRELIMINARY
IDT77V500

Features

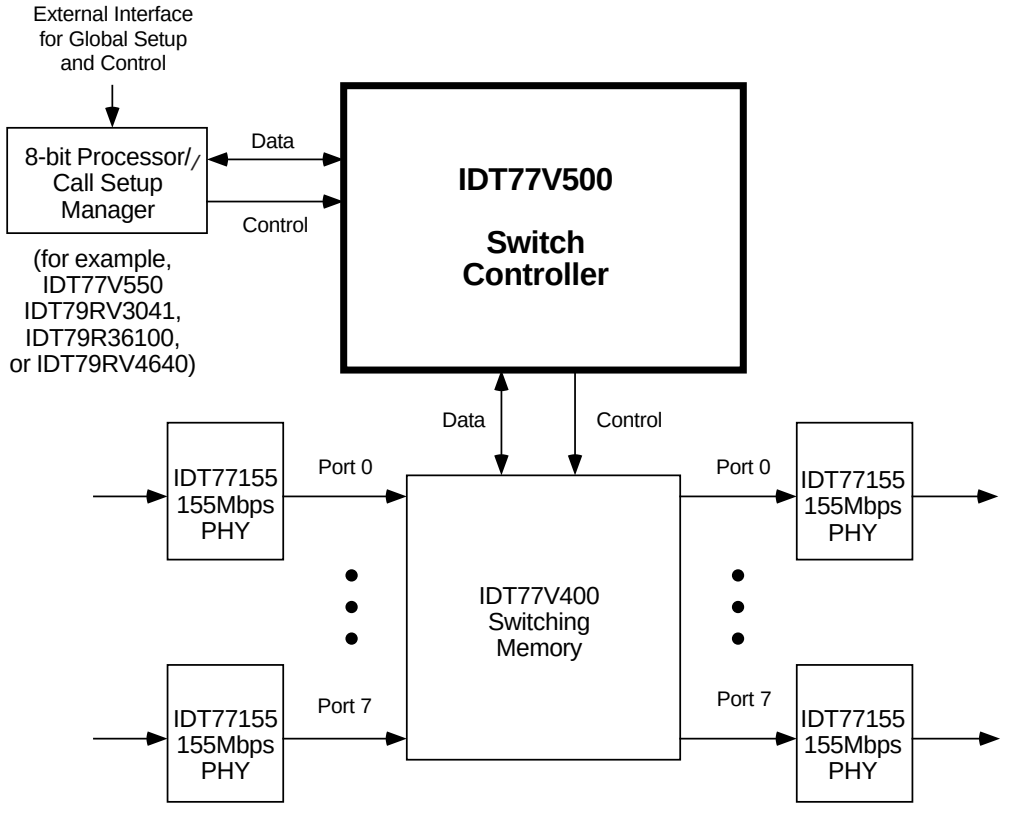
- **Single chip controller for IDT77V400 Switching Memory**
- **One IDT77V500 and one IDT77V400 form the core required for a 1.24Gbps 8 x 8 port non-blocking switch**
- **Supports up to 8192 Virtual Connections (VCs)**
- **Per VC queuing for fairness, with four priorities per VC available for each output port of the switch**
- **Capable of supporting CBR, VBR, UBR, and ABR (EFCI) service classes**
- **Low power dissipation**
  –430mW (typ.)
- **Optional header modification operation**
- **Multicasting and Broadcasting capability**
- **Provides congestion management support through EFCI, CLP, and EPD functionality**
- **System clock cycle times as fast as 27ns (37MHz)**
- **Option available for resolving contention issues between multiple IDT77V500 configurations**
- **One IDT77V500 can manage up to eight IDT77V400's without derating for larger switch configurations**
- **Industrial temperature range (-40° C to +85° C) is available**
- **Single +3.3V ± 300mV power supply**
- **Available in a 100-pin Thin Plastic Quad Flat Pack (TQFP)**

Description

The IDT77V500 ATM Cell Based Switch Controller, when paired with the IDT77V400 Switching Memory, forms the core control logic and switch fabric for a 1.24Gbps non-blocking ATM switch. The IDT77V500 manages all of the switch traffic moving through the IDT77V400, commanding the storage of incoming ATM cells and interpreting and modifying the cell header information as necessary for data flow through the switch. It then uses the header information, including priority indicators, to queue and direct the individual cells for transmission out the appropriate output port of the IDT77V400.

The IDT77V500 utilizes Per Virtual Connection (VC) Queuing to keep track of each call, and has the capacity to keep track of as many

Typical 8 x 8 Switch Configuration using the IDT77V500 Switch Controller



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Description (cont.)

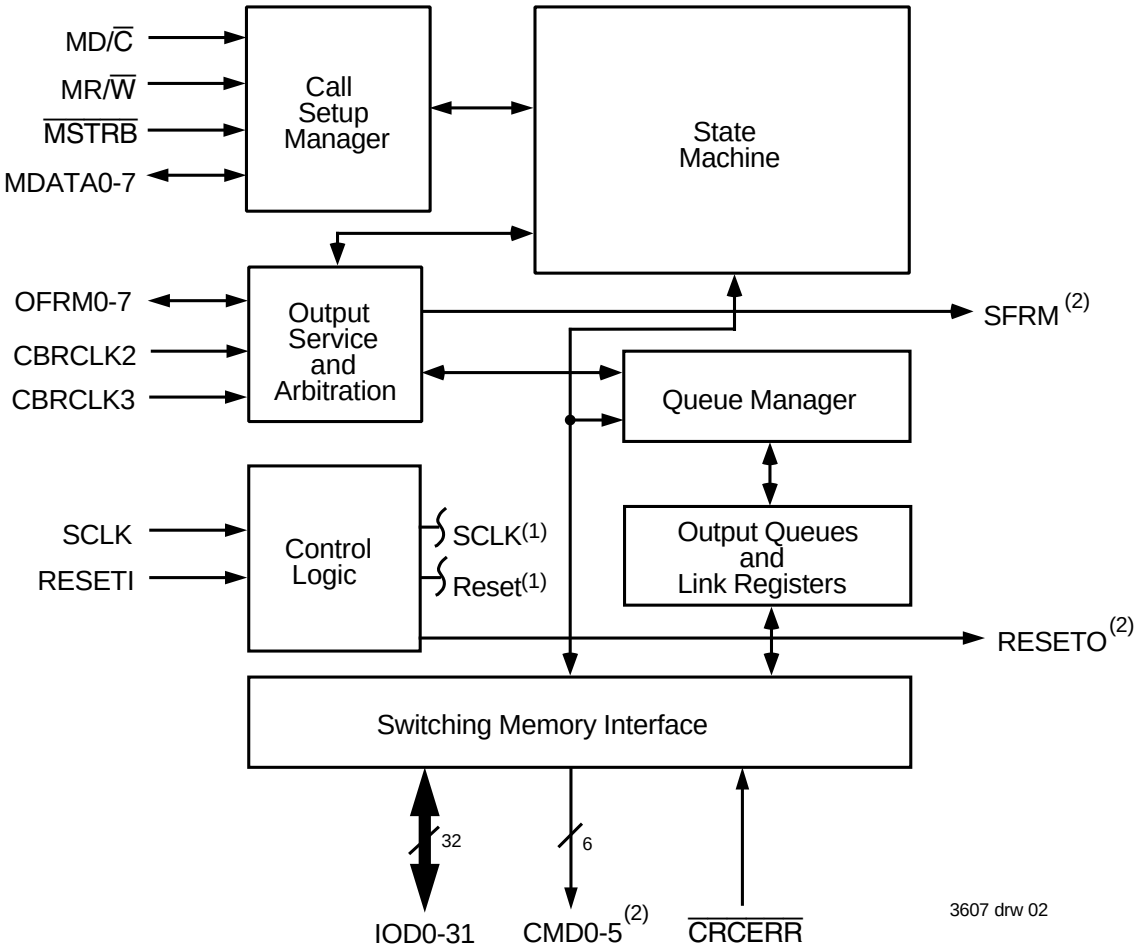
as 8192 individual VC queues. There are four possible priorities available for each of the assigned outputs of the Switching Memory, and CBR, VBR, UBR, and ABR-EFCI service classes are supported by the Switch Controller. Multicasting and broadcasting services are provided, requiring only the appropriate header information to execute these operations automatically without requiring multiple Switching Memory entries.

The IDT77V500 also has a mode for managing and transmitting pocketized data, enabling easy transition between packet oriented networks such as Ethernet and FDDI and ATM cell oriented networks. The IDT77V500 has an 8-bit Manager Bus interface, MDATA0-7, to a Call Setup Manager processor for the configuration activity and call setup operation. When a Call Setup Cell is received by the IDT77V400, the cell is directed to a specified output port and the payload processed by the Call Setup Manager. The new Virtual Connection (VC) is then established in the Queue Manager of the IDT77V500, with all operations executed across the 8-bit Manager Bus. Subsequent cells of that particular VC are then prioritized and directed by the Switch Controller as they are received by the IDT77V400; no further interaction with the Call Manager processor is required for ongoing queue and cell management.

The IDT77V500 supports a major subset of the available commands and configurations of the IDT77V400 Switching Memory. Please refer to the SWITCHStAR User Manual for additional feature details and implementation information.

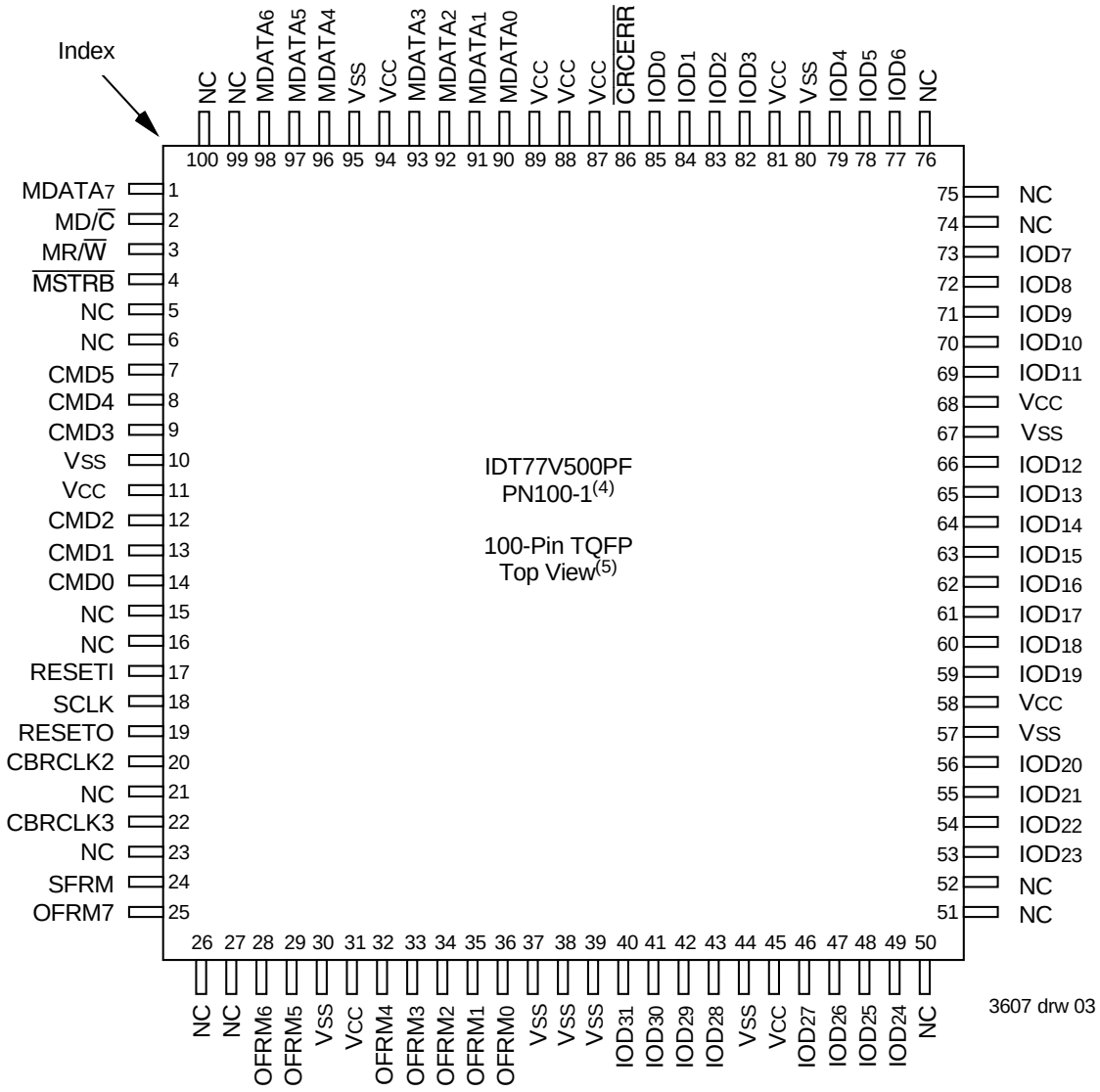
The IDT77V500 is fully 3.3V LVTTL compatible, and is packaged in an 100-pin Thin Plastic Quad Flatpack (TQFP).

Functional Block Diagram



NOTES:
1. SCLK and Reset are inputs to all blocks.
2. Outputs are always enabled (active).

Package Diagram(1,2,3)



NOTES:

1. All VCC pins must be connected to power supply.
2. All VSS pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part marking.

Pin Description

Pin Number	Symbol	Type	Description
18	SCLK	I	System clock: Refererence clock input for all synchronous pins of the IDT77V500 Switch Controller. All synchronous signals are referenced to the rising edge of SCLK.
22,20	CBRCLK3, CBRCLK2	I	CBR Clocks 3 and 2: External clock signals used when Constant Bit Rate (CBR) Service classes are utilized. These clock signals correspond to Output Port priorities 3 and 2 respectively and are used to determine the constant bit rate for the controller. Priority 3 is the highest priority. If CBR mode is not used these pins should be pulled up to Vcc with a resistor with a recommended value of 5K ohm or less.
86	$\overline{\text{CRCERR}}$	I	Cyclical Redundancy Check Error: Synchronous input on the rising edge of SCLK. $\overline{\text{CRCERR}}$ asserted LOW by the IDT77V400 Switching Memory during a store operation indicates that a HEC CRC error has occured in the cell header.
2	MD/$\overline{\text{C}}$	I	Manager Control: Selects the data or control registers of the IDT77V500 for the Manager Bus Operation. MD/$\overline{\text{C}}$ asserted HIGH selects the data registers, and MD/$\overline{\text{C}}$ LOW selects the command/status registers of the IDT77V500.
3	MR/$\overline{\text{W}}$	I	Manager Read/Write: MR/$\overline{\text{W}}$ LOW will write the data on the Manager Bus into the registers selected by the MD/$\overline{\text{C}}$ input. In write mode (MR/$\overline{\text{W}}$ LOW) the data on MDATA0-7 is written synchronously with respect to the rising edge of $\overline{\text{MSTRB}}$; in read mode (MR/$\overline{\text{W}}$ HIGH) the data is accessed asynchronously.
4	$\overline{\text{MSTRB}}$	I	Manager Strobe: Input which acts as a clock for the Manager Bus (MDATA0-7). Other Manager Bus inputs are synchronous to the rising edge of $\overline{\text{MSTRB}}$ during write operations (MR/$\overline{\text{W}}$ LOW) and must meet the specified Setup and Hold parameters. $\overline{\text{MSTRB}}$ performs an asynchronous Output Enable function when a read operation (MR/$\overline{\text{W}}$ HIGH) is executed on the Manager Bus. When $\overline{\text{MSTRB}}$ is LOW and MR/$\overline{\text{W}}$ is HIGH (Read Mode) the Manager Bus is enabled in output mode and the contents of the IDT77V500 registers (determined by the MD/C input) are available to be read on MDATA0-7.
17	RESETI	I	Reset Input: When asserted HIGH, this signal asynchronously initiates the internal reset sequence of the IDT77V500.
19	RESETO	O	Reset Output: Asserted HIGH upon initiating the reset of the IDT77V500 (RESETI HIGH). In multiple IDT77V500 configurations, this output is connected to the RESETI input of the next controller in the chain. RESETO will remain HIGH until a START command is received from the Call Setup Manager.
7-9, 12-14	CMD0-5	O	Command Bus: Synchronized with SCLK, instructions to be executed by the IDT77V400 Switching memory are output by the IDT77V500 on this 6-bit bus.
24	SFRM	O	Synchronize Output Frame: Synchronous output used when multiple IDT77V500's contend for a common bus. The Master IDT77V500 generates this signal which then drives the OFRM0 input of the other IDT77V500s.
40-43, 46-49, 53-56, 59-66, 69-73, 77-79 82-85	IOD0-31	I/O	Control Data Bus: Synchronous with SCLK and one cycle latent to the Command Bus (CMD0-5). Used for transfer of the header bytes, configuration register, error and status registers, and the cell memory address between the IDT77V500 and the IDT77V400 Switching Memory.
1, 90-93, 96-98	MDATA6-7	I/O	Manager Bus: Communications between the Call Setup Manager and the IDT77V500 occur over this 8-bit bi-directional bus. MD/$\overline{\text{C}}$, MR/$\overline{\text{W}}$, and $\overline{\text{MSTRB}}$ dtermine the mode and data type transferred across the MDATA bus. Write operations are synchronous with respect to $\overline{\text{MSTRB}}$, while MDATA behaves asynchronously for read operations.
25, 28-29, 32-35, 36	OFRM1-7 OFRM0	I/O I	Output Frame: Asynchronous input pins used by the IDT77V500 to detect when the next cell can be loaded to the specified IDT77V400 output port 0 through 7. When in multiple IDT77V500 configurations, the OFRM1-7 are redefined as CBUS1-7 for arbitration. OFRM0 is always an input pin (There is no CBUS0).
11, 31, 45, 58, 68, 81, 87-89, 94	V_{CC}	Power	Power Supply (+3.3V ± 300mV)
10, 30, 37-39, 44, 57, 67, 80, 95	V_{SS}	Power	Ground
5-6, 15-16, 21, 23, 26-27, 50-52, 74-76, 99-100	NC	—	No Connect

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Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +3.9	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3607 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.3V.

Capacitance (T_A = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 3dV	10	pF

3607 tbl 05

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3607 tbl 03

NOTE:
1. This is the parameter T_A.

Recommended DC Operating Conditions(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC}+0.3V(3)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3607 tbl 04

NOTES:
1. V_{IL}≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V or Vss – 0.3V.
3. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.3V.

DC Electrical Ccharacteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V500S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$(1)	Output Leakage Current	RESTI = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3607 tbl 06

NOTE:
1. For MDATA, IOD, and OFRM pins only.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	77V500S25/27PFI		77V500S25/27PF		Unit
			Typ.	Max.	Typ.	Max.	
I_{CC}	Operating Current	V_{CC} = 3.6V, RESETI = V_{IL}, f = f_{MAX}(1)	130	200	130	175	mA
I_{CCR}	Reset Current	V_{CC} = 3.6V, RESETI = V_{IH}, f = f_{MAX}(1)	150	325	150	300	mA

3607 tbl 07

NOTE:
1. At f = f_{max} SCLK is cycling at maximum frequency and all inputs are cycling at 1/t_{CYC1}, using AC input levels of V_{SS} to 3.0V.

AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3607 tbl 08

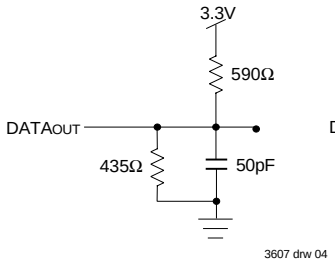

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Figure 1. AC Output Test Load

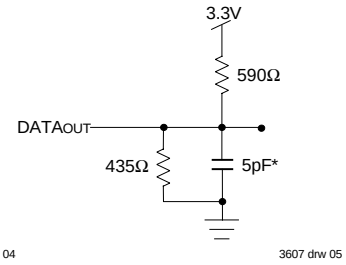

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Figure 2. Output Test Load
(for High-Impedance parameters)
* Including scope and jig.

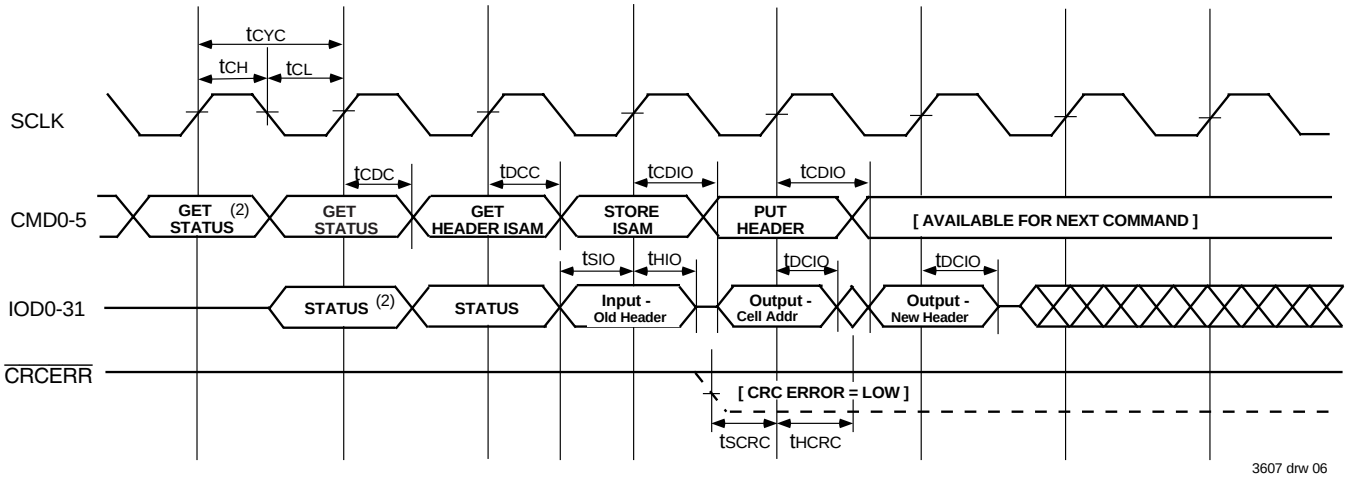
AC Electrical Characteristics Over the Operating Temperature Range
(Vcc = 3.3V ± 0.3V)

		77V500S25 Com'l & Ind		77V500S27 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	System Clock Cycle Time	25	—	27	—	ns
t_{CH}	Systen Clock High Time	10	—	11	—	ns
t_{CL}	System Clock Low Time	10	—	11	—	ns
t_R	Clock Rise Time	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	ns
t_{MCYC}	Manager Clock Cycle Time	25	—	27	—	ns
t_{MCH}	Manager Clock High Time	6	—	7	—	ns
t_{MCL}	Manager Clock Low Time	19	—	20	—	ns
t_{SM}	MD/$\overline{C}$ Setup Time to $\overline{MSTRB}$ High	10	—	10	—	ns
t_{HM}	MD/$\overline{C}$ Hold Time after $\overline{MSTRB}$ High	2	—	2	—	ns
t_{SMRW}	MR/$\overline{W}$ Setup Time to $\overline{MSTRB}$ High	10	—	10	—	ns
t_{HMRW}	MR/$\overline{W}$ Hold Time after $\overline{MSTRB}$ High	2	—	2	—	ns
t_{SMD}	MDATA Setup Time to $\overline{MSTRB}$ High	10	—	10	—	ns
t_{HMD}	MDATA Hold Time after $\overline{MSTRB}$ High	2	—	2	—	ns
t_{SCRC}	$\overline{CRCERR}$ Setup Time to SCLK High	5	—	5	—	ns
t_{HCRC}	$\overline{CRCERR}$ Hold Time after SCLK High	2	—	2	—	ns
t_{SIO}	IOD Setup Time to SCLK High	5	—	5	—	ns
t_{HIO}	IOD Hold Time after SCLK High	2	—	2	—	ns
t_{OFP}	OFRM High Pulse Width	5	—	5	—	ns
t_{CDC}	SCLK to CMD Valid	—	18	—	20	ns
t_{DCC}	CMD Output Hold after SCLK High	—	2	—	2	ns
t_{CDS}	SCLK to SFRM Valid	—	18	—	20	ns
t_{DCS}	SFRM Output Hold after SCLK High	—	2	—	2	ns
t_{CDIO}	SCLK to IOD Valid	—	18	—	20	ns
t_{DCIO}	IOD Output Hold after SCLK High	—	2	—	2	ns
t_{AMD}	$\overline{MSTRB}$ Low to MDATA Valid	—	18	—	20	ns
t_{OHMD}	MDATA Output Hold after $\overline{MSTRB}$ High	—	2	—	2	ns
t_{CDOF}	SCLK to OFRM/CBUS Valid	—	18	—	20	ns
t_{DCOF}	OFRM/CBUS Output Hold after SCLK High	—	2	—	2	ns
t_{RSI}	RESETI High Pulse Width[1]	8	—	8	—	t_{CYC}
t_{RSO}	RESETO High after RESETI High	—	2	—	2	t_{CYC}
t_{CDR}	SCLK to RESETO Valid	—	18	—	20	ns
t_{CKHZ}	SCLK High to Output High-Z[2]	—	10	—	10	ns
t_{CKLZ}	SCLK High to Output Low-Z[2]	2	—	2	—	ns
t_{CYC3}	CBRCLK3 Clock Cycle Time[3]	3	—	3	—	t_{CYC}
t_{CH3}	CBRCLK3 Clock High Time[3]	1.2	—	1.2	—	t_{CYC}
t_{CL3}	CBRCLK3 Clock Low Time[3]	1.2	—	1.2	—	t_{CYC}
t_{CYC2}	CBRCLK2 Clock Cycle Time[3]	3	—	3	—	t_{CYC}
t_{CH2}	CBRCLK2 Clock High Time[3]	1.2	—	1.2	—	t_{CYC}
t_{CL2}	CBRCLK2 Clock Low Time[3]	1.2	—	1.2	—	t_{CYC}

3607 tbl 09

NOTES:
1. RESETI must be held High for 8 SCLK cycles. After RESETI transitions Low 8191 cycles are required before the Status Acknowledge bits will indicate that the internal reset process in complete.
2. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
3. Cycle units insure that the SCLK recognizes the state of CBRCLK.

Control Interface Timing Waveform(1)



NOTES:
1. This waveform describes the command interaction across the IOD Bus to the IDT77V400 Switching Memory.
2. The result of this GET STATUS command is that an ISAM is full and ready to be stored to the Fusion Memory of the IDT77V400.

Control Interface Commands(1)

		COMMAND Bus Bit (CMD5:0)					
		MSb					LSb
Command	Command Description	5	4	3	2	1	0
GHIx	Get Header from ISAMx(2)	0	0	1	n(3)	n(3)	n(3)
GST	Get ISAM Status Register Bits	0	1	0	0	1	0
GER	Get Error Register Bits	0	1	0	1	1	0
STEx	Store Cell in ISAMx(2) and Edit Buffer in Memory	1	0	0	n(3)	n(3)	n(3)
LDOx	Load Cell from Memory into OSAMx(2)	1	1	0	n(3)	n(3)	n(3)
PHE	Put new Header in Edit Buffer	1	1	1	1	0	0
PHEC	Put new Header and new CRC byte in Edit Buffer	1	1	1	1	0	1
REF	Refresh Fusion Memory	0	1	0	1	1	1
LDC	Load Configuration Register	1	1	1	0	1	0
OHE	Put new Header in Output Edit Register	1	1	1	1	1	0
OHEC	Put new Header and new CRC byte in Output Edit Register	1	1	1	0	0	1

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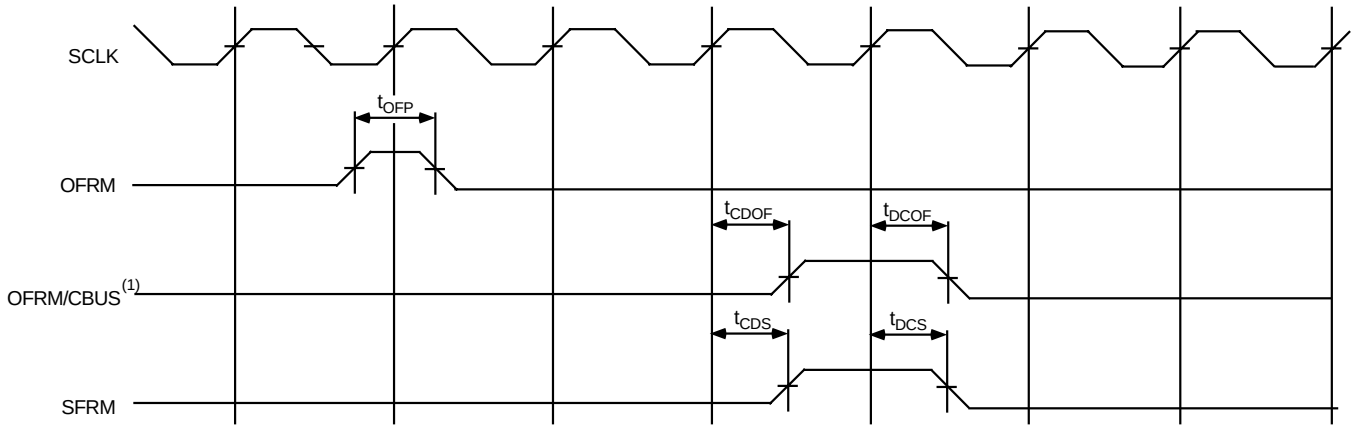
NOTES:
1. CMD bus commands not defined in this table are undefined and are not implemented by the IDT77V500.
2. "x" represents the specific ISAM or OSAM being accessed (IP0-IP7 or OP0-OP7 respectively).
3. "n" represents the appropriate bit of the binary representation of the ISAM or OSAM being accessed (000 to 111).

SFRM, CBUS, and OFRM Timing Waveforms



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NOTE:
1. OFRM1-7 become CBUS1-7 (Outputs) during cell bus operations to arbitrate between multiple IDT77V500's.

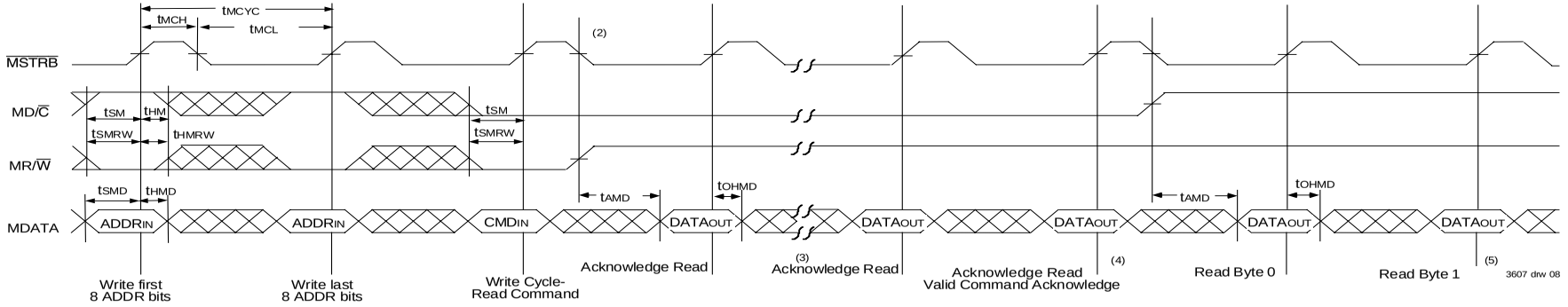
Manager Commands(1)

Command	Command Name	Command Description	Code (in Hex)
WRSL	Write Service Link Memory	Write into Service Link Memory to initialize scheduled service lists.	03
STAT	Read IDT77V500 status	Reads the internal status of the IDT77V500. Available information includes various error registers and counts.	07
LDCFG	Load IDT77V400 Configuration Bits	Passes configuration information to the IDT77V400.	08
SUP	Call setup	Writes the appropriate information into an entry of the Per VC Memory to perform the call setup function.	09
INT	Initialize IDT77V500	Initializes the internal configuration registers of the IDT77V500.	0A
SEL	Select a IDT77V500	Selects the IDT77V500 to be enabled in a multiple device configuration.	0B
START	End of IDT77V500 Initialization	Sets the IDT77V500 into an enabled state after it has been initialized.	0C
CBR	Set up a CBR Scheduler	Sets up a selected output service list in the Constant Bit Rate (CBR) mode.	0D
PARM	Set Parameters	Sets various parameters in the IDT77V500, including the CLP low water mark, the EFCI low water mark, and the EPD low water mark.	0E

3607 tbl 11

NOTE:
1. Manager Command codes not defined in this table are not to be used.

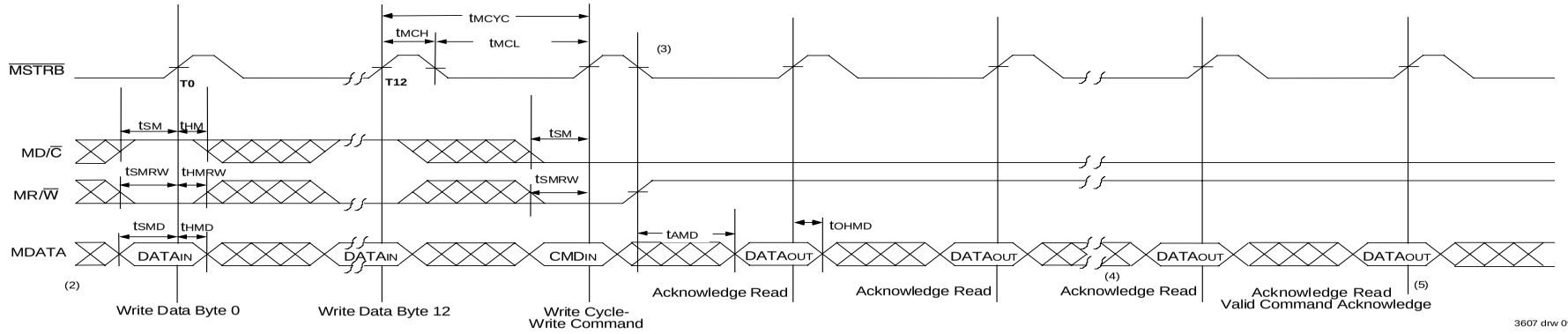
Manager Bus Read Timing Waveform(1)



NOTES:

1. Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{MSTRB}$. The data placed on the MDATA pins is determined by the state of the MD/$\overline{C}$ pin.
2. The combination of $\overline{MSTRB}$ Low and MR/$\overline{W}$ High (Read mode) asynchronously enables the MDATA pins as outputs. That is, data is available to be read one asynchronous t_{AMD} time after the falling edge of $\overline{MSTRB}$ if MR/$\overline{W}$ is HIGH.
3. After the Command is written, the Manager must take MR/$\overline{W}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.
4. A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).
5. Waveform illustrates first two bytes of data only. Additional bytes may be available based on command used.

Manager Bus Write Timing Waveform(1)



NOTES:

1. Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{MSTRB}$. The data placed on the MDATA pins is determined by the state of the MD/$\overline{C}$ pin.
2. Either a Read cycle was completed or a Status Acknowledge was executed immediately prior to the first $\overline{MSTRB}$ of this write waveform.
3. The combination of $\overline{MSTRB}$ Low and MR/$\overline{W}$ High (Read mode) asynchronously enables the MDATA pins as outputs. The data placed on the MDATA pins is determined by the state of the MD/$\overline{C}$ pin.
4. After the Command is written, the Manager must take MR/$\overline{W}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.
5. A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).

CBR Functional Description

The Constant Bit Rate (CBR) functionality of the IDT77V500 provides both the opportunity for scheduling priority traffic at a regular interval and traffic shaping capability. Two external CBR clocks, CBRCLK3 and CBRCLK2, are available and associated with Output Priority 3 (Highest Priority) and Priority 2 respectively. Calls assigned to a particular CBR VC in the IDT77V500 Per VC Table are linked together in a CBR Per VC list by output, so that a cell from each VC of a particular CBR Per VC list are serviced on each cycle through the list. The CBR Per VC List is identified by both the output and CBR priority on that output; for example, OPyCBRx VC list represents Output y (Output number 0-7) and CBR priority x (CBR priority 3 or 2). Figure 3 is an example of an OPyCBRx VC List with four VCs in the list: 100 (the first entry in the list), 200, 300 and 400. The arrows indicate the linking sequence in this VC List. Figure 3 will be used with the CBR Clock Functional Waveforms to illustrate two basic functional implementations using the CBR Clocks.

CBR Clock Functional Waveform Example 1 uses the CBR clocks to frame execution of the OPyCBRx VC List. A cell from a specific VC on the OPyCBRx VC List is scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx. The cell will then be transmitted when output y is available and other previously scheduled Input and Output ports of the IDT77V400 have been serviced. This delay can be as long as 65 SCLK cycles maximum for each cell in the CBR VC List , although it will typically be significantly less. This delay needs to be taken into account, as the next cell in the OPyCBRx VC List will not be scheduled until the previous cell in the list has been serviced. Thus enough CBRCLKx pulses need to be provided to make sure all potential cells in the OPyCBRx VC List are scheduled. This waveform illustrates the ideal case of each cell being immediately transmitted after scheduling, enabling the scheduling and transmission of the next cell in the OPyCBRxVC List on the next SCLK rising edge. CBRCLKx HIGH for eight SCLK cycles or more tells the controller that the pointer should be moved back to the top of the CBR VC List if all the VCs in the list have been serviced. Thus the user can establish a frame duration and be assured that a cell from each VC in the OPyCBRx VC List is transmitted in each frame time. Sub lists can also be established within the CBR VC List so that a particular VC could be weighted to ship more cells per frame than the others.

Example 2 illustrates using very slow CBR clocks (tCHx greater than or equal to 8 SCLKs) toshape traffic in a VBR form of implementation. A cell from a VC on the OPyCBRx VC List is again scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx, but since t_{CHx} is HIGH for more than eight SCLKs, there is more direct control over the exact time in which each cell of the VC List is scheduled. The single cell will then be transmitted when the output is available and other previously scheduled Input and Output ports of the IDT77V400 have been serviced (there is again the potential 65 SCLK delay based on other traffic passing through the IDT77V400). The IDT77V500 will service all of the VCs in the OPyCBRx VC List because the count will prevent the pointer from returning to the top of the CBR VC List until all VCs on the list with cells have been serviced. The user can thus more closely manage the transmission of cells with this slower CBR clock rate because it is more directly related to individual CBRCLKx High-to-Low transitions.

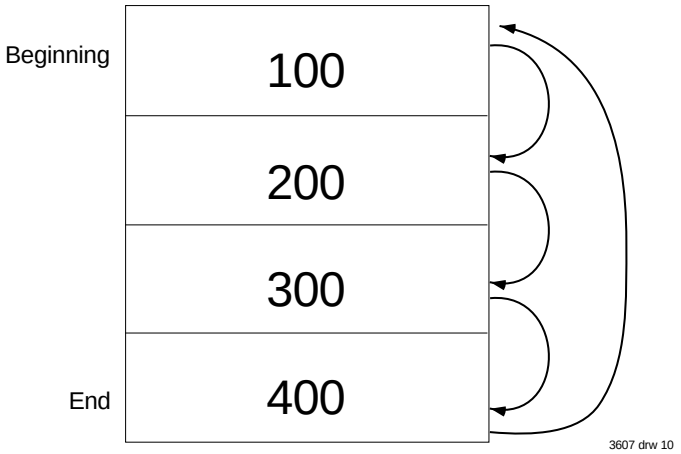
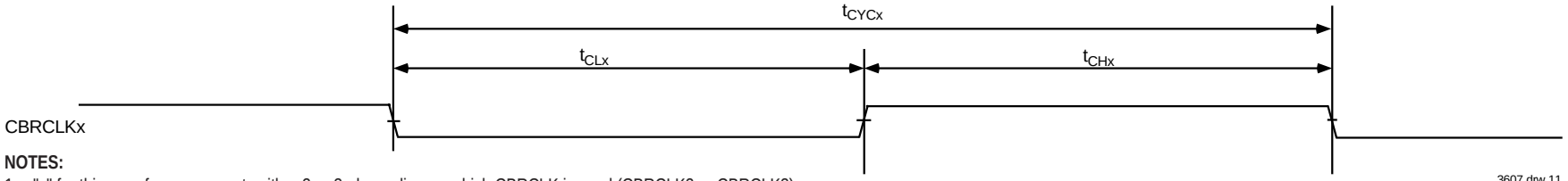


Figure 3.
OPyCBRx VC List Example

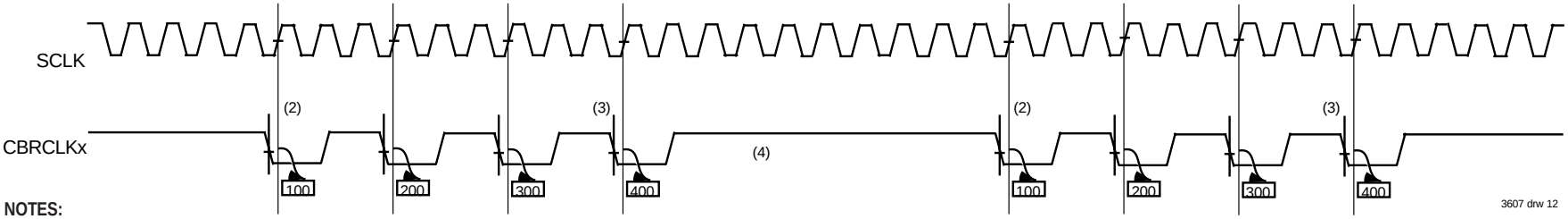
CBR Clock Parameters(1)



3607 drw 11

NOTES:
1. "x" for this waveform represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3).

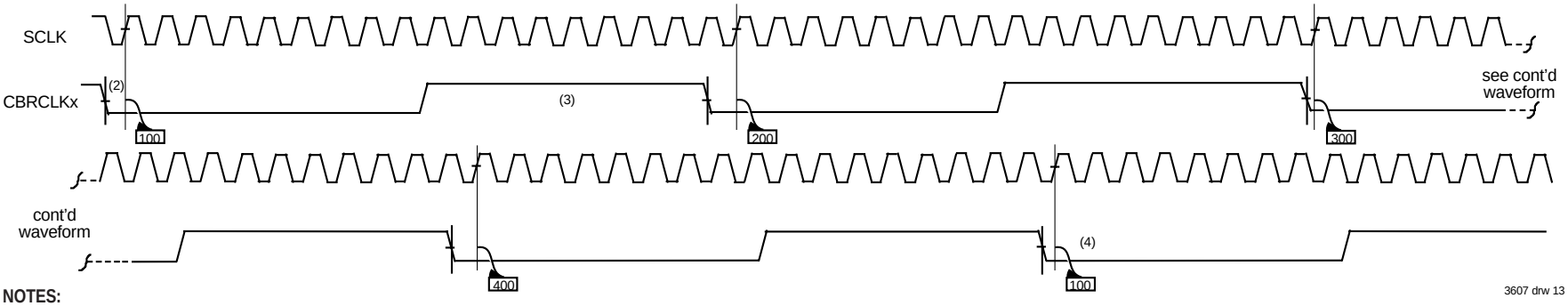
CBR Clock Functional Waveform Example 1 - CBR Frame Implementation (Fast CBRCLK with Frame Timing)(1)



3607 drw 12

NOTES:
1. This example shows the procedure recommended for use of direct CBR scheduling. "x" for this waveform represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3) ("y" represents the specific output (0-7)). The OPyCBRx VC List for this example is defined in figure 3.
2. A cell from a VC on the OPyCBRx VC List is scheduled on each rising clock edge of SCLK after a falling edge of CBRCLKx.
3. This example shows four VC's in the OPyCBRx VC List. The number of VC's in the OPxCBRx VC List may be as large as 8192.
4. The period between reinitiation of the OPyCBRx VC List defines the frame size; that is, the amount of time between starting the transmissions from the top of the OPyCBRx VC List. CBRCLKx must be HIGH for eight clocks or more to reinitiate the transmission sequence at the start of the OPyCBRx VC List.

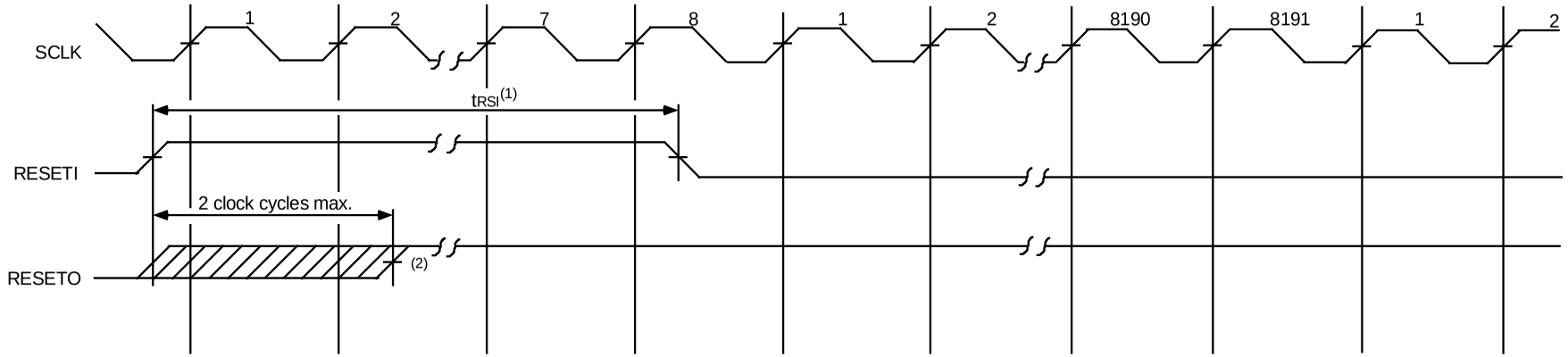
CBR Clock Functional Waveform Example 2 - VBR/CBR Implementation (tCHx > 8 SCLK)(1)



3607 drw 13

NOTES:
1. This example shows the use of a slower CBRCLK (tCHX > 8 SCLK) to provide VBR/CBR traffic shaping. For this waveform "x" represents either 2 or 3, depending on which CBRCLK is used (CBRCLK2 or CBRCLK3). ("y" represents the specific output (0-7)) The OPyCBRx VC List for this example is defined in Figure 3.
2. A cell from a VC on the OPyCBRx VC List is scheduled on each rising edge of SCLK after a falling edge of CBRCLKx.
3. tCHX > 8 SCLK so that a cell is scheduled after each falling edge of CBRCLKx.
4. The pointer has moved back to the beginning of the OPyCBRx VC List.

Reset WaveformS

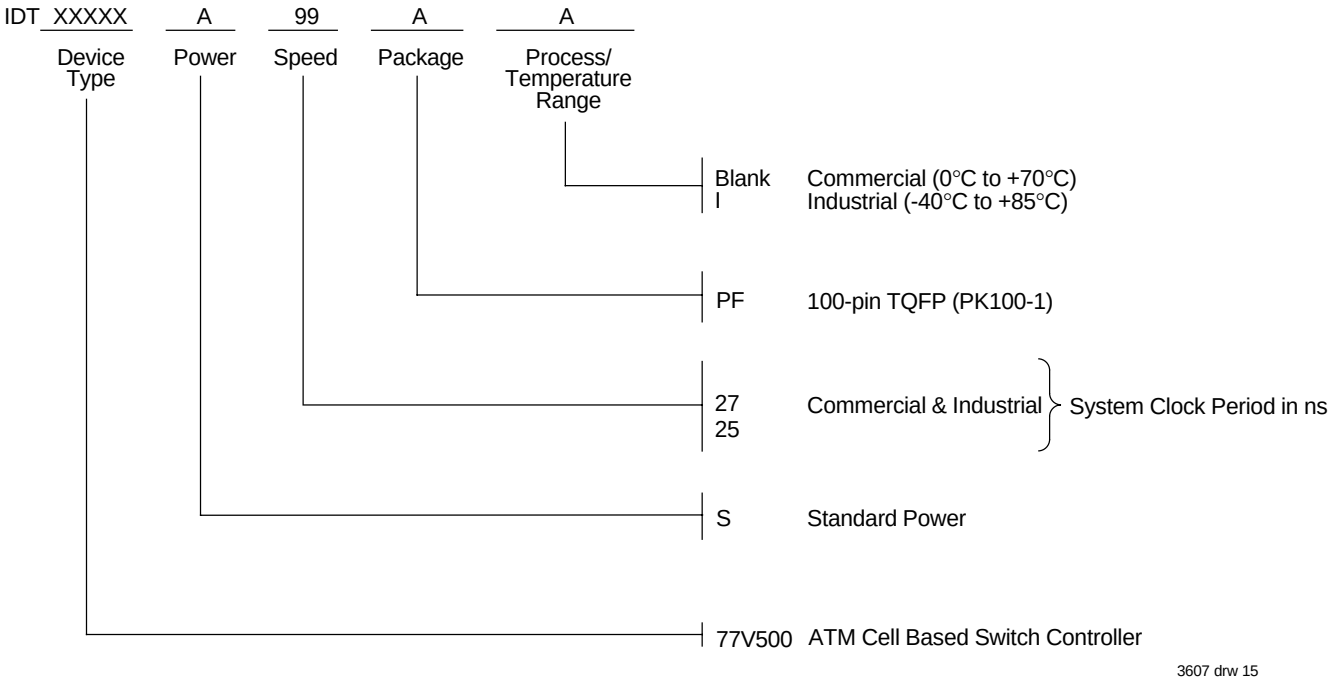


3607 drw 14

NOTES:

1. RESETI must be held HIGH for 8 SCLK cycles. When RESETI goes LOW again 8191 cycles are used prior to the Status Acknowledge bits showing the internal reset process is complete.
2. This delay should typically be much less than two SCLK cycles. RESETO remains HIGH until START Command is received from the Call Setup Manager.

Ordering Information



3607 drw 15

Preliminary Datasheet: Definition

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

Datasheet Document History

3/1/99: Updated to new format.
Added Industrial Specifications.
Added S25 Speed Grade.

Pg. 3 Package Diagram noes added for clarification.
Pg. 4 Pin description table descriptions corrected. OFRM and Vss pin number corrections made.
Pg. 5 V_{TERM} in Maximum ratings table reduced to 3.9V.
Pg. 10 Manager Bus Sequence Waveforms Figures 9 and 10 and their notes modified for clarity.
Pg. 14 Updated Ordering Information for S156 speed grade and Industrial temperature product. Added Preliminary Datasheet definition and Datasheet Document History.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
SWITCHStARhelp@idt.com