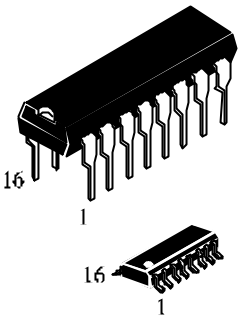
IN74HC157A

Quad 2-Input Data Selectors/Multiplexer

The IN74HC157A is identical in pin out to the LS/ALS157. The device inputs are compatible with standard CMOS outputs; with pull up resistors, they are compatible with LS/ALSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in non inverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

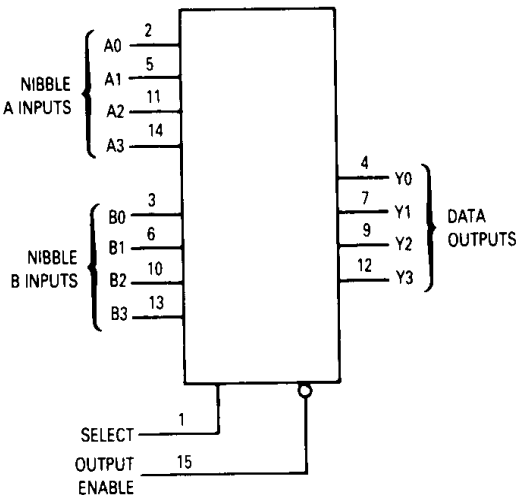
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



ORDERING INFORMATION

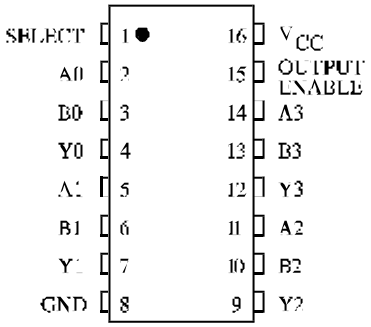
IN74HC157AN Plastic
IN74HC157AD SOIC
IZ74HC157A Chip
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Output Enable	Select	Y0-Y3
H	X	L
L	L	A0-A3
L	H	B0-B3

X=don't care
A0-A3, B0-B3=the levels of the respective Data-Word Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0µA	6.0	4.0	40	160	µA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1and 4)	2.0 4.5 6.0	105 21 18	130 26 22	160 32 27	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Select to Output Y (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Output Enable to Output Y (Figures 3 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 33	pF

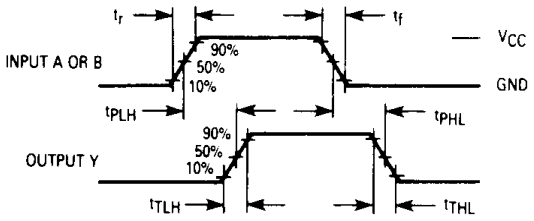


Figure 1. Switching Waveforms

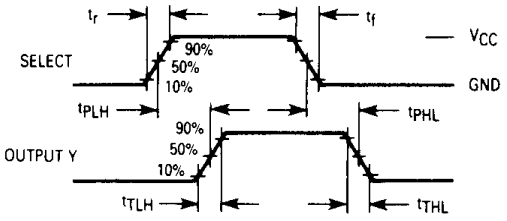


Figure 2. Switching Waveforms

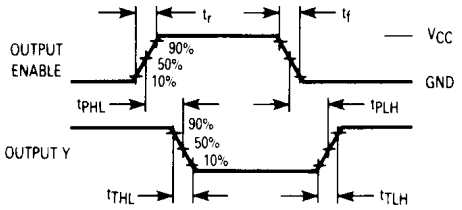


Figure 3. Switching Waveforms

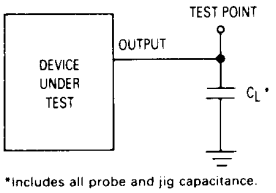
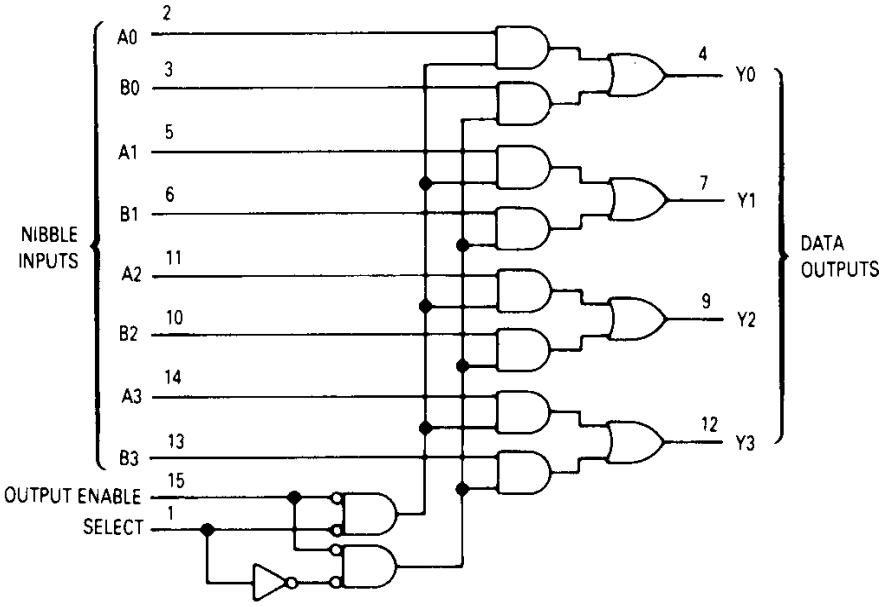
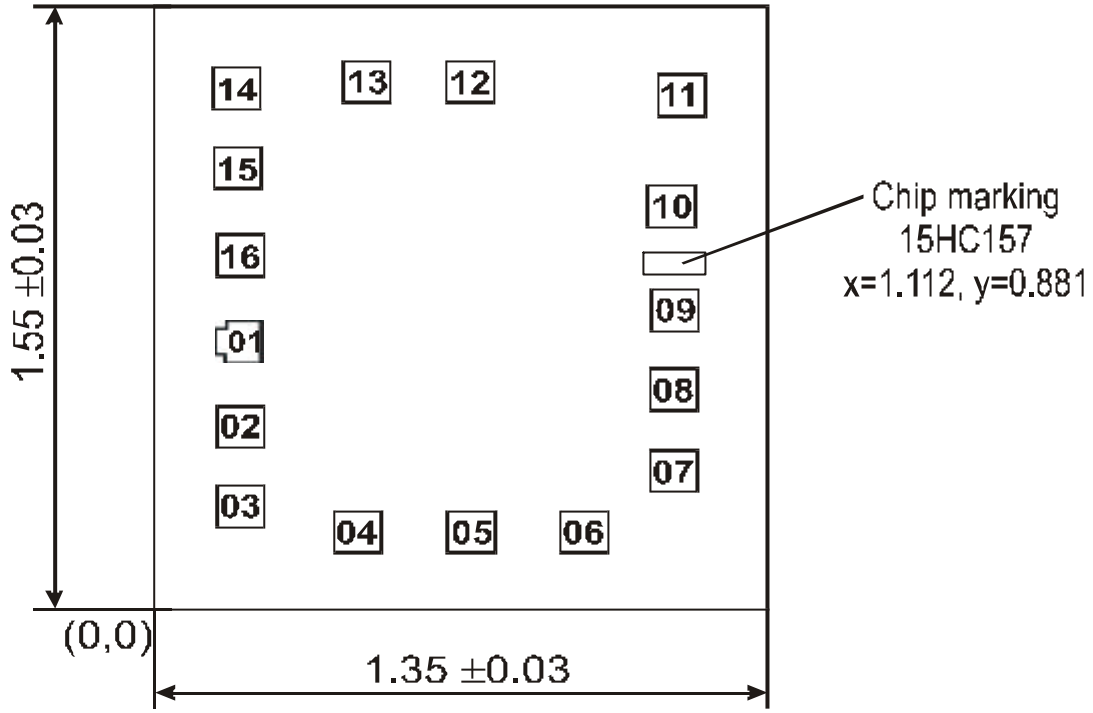


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM IZ74HC157A



Pad size 0.120 x 0.120 mm (Pad size is given as per passivation layer)
Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y	Pad size
01	SELECT	0.143	0.668	0.106x0.106
02	A0	0.143	0.443	0.106x0.106
03	B0	0.143	0.173	0.106x0.106
04	Y0	0.377	0.133	0.106x0.106
05	A1	0.644	0.133	0.106x0.106
06	B1	0.848	0.133	0.106x0.106
07	Y1	1.132	0.244	0.106x0.106
08	GND	1.132	0.468	0.106x0.159
09	Y2	1.131	0.748	0.106x0.106
10	B2	1.101	1.036	0.106x0.106
11	A2	1.122	1.27	0.106x0.106
12	Y3	0.650	0.311	0.106x0.106
13	B3	0.442	1.311	0.106x0.106
14	A3	0.153	1.271	0.106x0.106
15	OUTPUT ENABLE	0.143	1.069	0.106x0.106
16	Vcc	0.143	0.838	0.106x0.159