

IN74HCT373A

Octal 3-State Noninverting
Transparent Latch
High-Performance Silicon-Gate CMOS

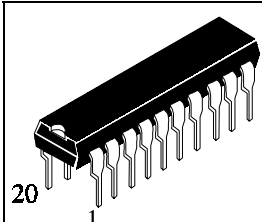
The IN74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The IN74HCT373A is identical in pinout to the LS/ALS373.

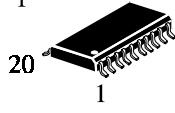
The eight latches of the IN74HCT373A are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



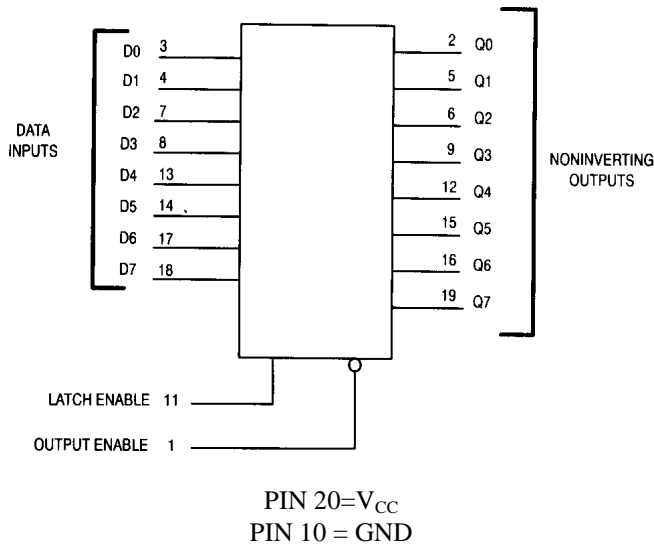
N SUFFIX
PLASTIC



DW SUFFIX
SOIC

ORDERING INFORMATION
IN74HCT373AN Plastic
IN74HCT373ADW SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC}	Guaranteed Limit			Unit
			V	25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} =V _{CC} or GND	5.5	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{IN} =2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Inputs		≥-55°C		25°C to 125°C	mA
		I _{OUT} =0μA	5.5	2.9		2.4	

AC ELECTRICAL CHARACTERISTICS($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	28	35	42	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Latch Enable to Q (Figures 2 and 5)	32	40	48	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay ,Output Enable to Q (Figures 3 and 6)	30	38	45	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Latch)	Typical @25°C,V _{CC} =5.0 V	pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}	65	

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	10	13	15	ns
t_h	Minimum Hold Time,Latch Enable to Input D (Figure 4)	10	13	15	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	12	15	18	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

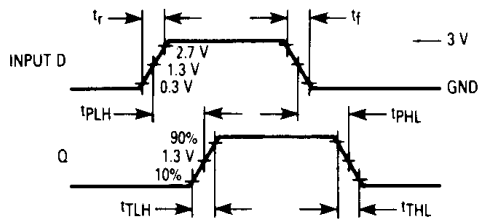


Figure 1. Switching Waveforms

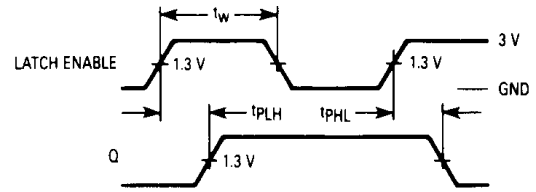


Figure 2. Switching Waveforms

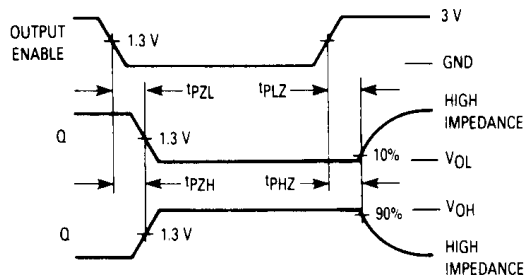


Figure 3. Switching Waveforms

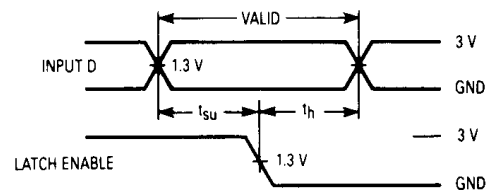
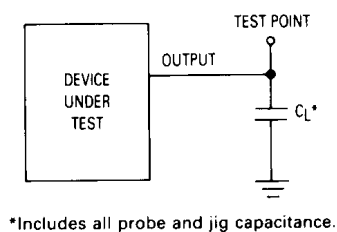
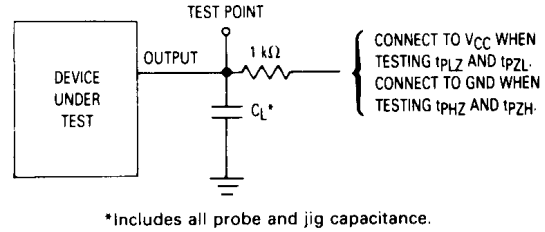


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM

