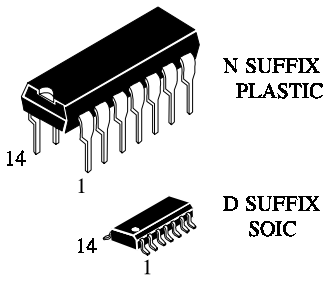
IW4013B

Dual D Flip-Flop
High-Voltage Silicon-Gate CMOS

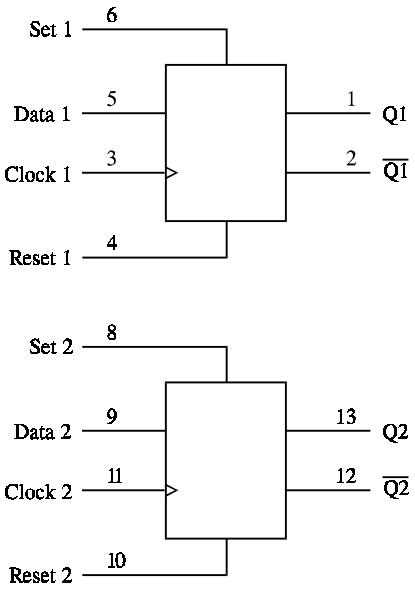
The IW4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting Q output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply



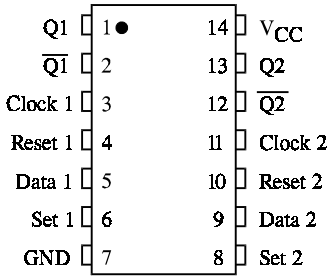
ORDERING INFORMATION
IW4013BN Plastic
IW4013BD SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Clock	Data	Reset	Set	Q	$\overline{Q}$
⌐¯	L	L	L	L	H
⌐¯	H	L	L	H	L
¯⌐	X	L	L	Q	$\overline{Q}$
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	1 2 4 20	1 2 4 20	30 60 120 600	µA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Maximum Clock Frequency (Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	1.75 4 6	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1)	5.0 10 15	300 130 90	300 130 90	600 260 180	ns
t_{PLH}	Maximum Propagation Delay, Set to Q or Reset to Q (Figure 2)	5.0 10 15	300 130 90	300 130 90	600 260 180	ns
t_{PHL}	Maximum Propagation Delay, Set to $\overline{Q}$ or Reset to Q (Figure 2)	5.0 10 15	400 170 120	400 170 120	800 340 240	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	140 60 40	140 60 40	280 120 80	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	5.0 10 15	180 80 50	180 80 50	360 160 100	ns
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	5.0 10 15	40 20 15	40 20 15	80 40 30	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0 10 15	5 5 5	5 5 5	10 10 10	ns
t_r, t_f	Maximum Input Rise or Fall Time, Clock (Figure 1)	5.0 10 15	500 30 6	500 30 6	1000 60 12	μs

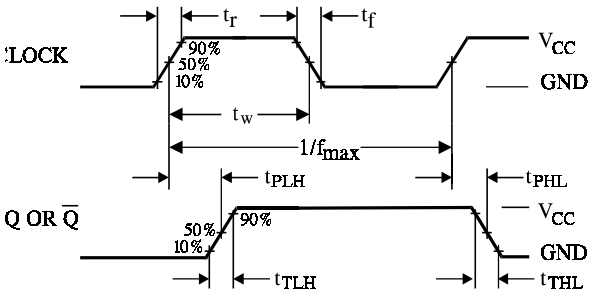


Figure 1. Switching Waveforms

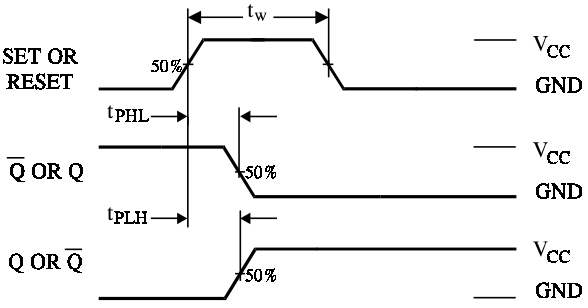


Figure 2. Switching Waveforms

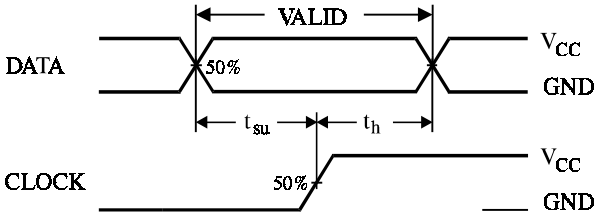


Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/2 of the Device)