LINEAR SYSTEMS

Linear Integrated Systems

SD-SST211/213/215

N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ V_{GS} = 10 V	0.5	2
SD213DE	10	1.5	45 @ V_{GS} = 10 V	0.5	2
SD215DE	20	1.5	45 @ V_{GS} = 10 V	0.5	2
SST211	30	1.5	50 @ V_{GS} = 10 V	0.5	2
SST213	10	1.5	50 @ V_{GS} = 10 V	0.5	2
SST215	20	1.5	50 @ V_{GS} = 10 V	0.5	2

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

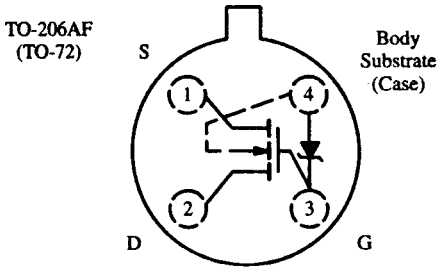
Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

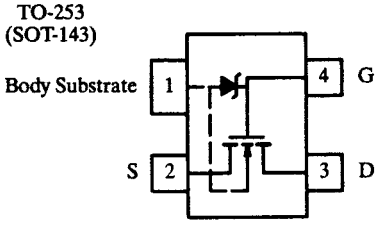
Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211 may be used for ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, and non-Zener protection—SD210DE/214DE.



Top View
SD211DE, SD213DE, SD215DE



Top View
SST211 (D1)*, SST213 (D3)*, SST215 (D5)*
*Marking Code for TO-253

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Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage	(SD211DE/SST211)	-30/25 V
	(SD213DE/SST213)	-15/25 V
	(SD215DE/SST215)	-25/30 V
Gate-Substrate Voltage[a]	(SD211DE/SST211	-0.3/25 V
	(SD213DE/SST213)	-0.3/25 V
	(SD215DE/SST215)	-0.3/30 V
Drain-Source Voltage	(SD211DE/SST211)	30 V
	(SD213DE/SST213)	10 V
	(SD215DE/SST215)	20 V
Source-Drain Voltage	(SD211DE/SST21)	10 V
	(SD213DE/SST213)	10 V
	(SD215DE/SST215)	20 V
Drain-Substrate Voltage	(SD211DE/SST211)	30 V
	(SD213DE/SST213)	15 V
	(SD215DE/SST215)	25 V
Source-Substrate Voltage	(SD211DE/SST211)	15 V
	(SD213DE/SST213)	15 V
	(SD215DE/SST215)	25 V
Drain Current		50 mA
Lead Temperature (1/16" from case for 10 seconds)		300°C
Storage Temperature		-65 to 150°C
Operating Junction Temperature		-55 to 125°C
Power Dissipation[a]		300 mW

Notes:
a. Derate 3 mW/°C above 25°C

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	211 Series Max	213 Series Min	213 Series Max	215 Series Min	215 Series Max	Unit
Static											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		35	15		15		25		
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V (SD Series)	58		70		70		70	Ω
			$V_{GS} = 5$ V (SST Series)	60		75		75		75	
			$V_{GS} = 10$ V (SD Series)	38		45		45		45	
			$V_{GS} = 10$ V (SST Series)	40		50		50		50	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	211 Series Max	213 Series Min	213 Series Max	215 Series Min	215 Series Max	Unit
Dynamic											
Forward Transconductance	g_{fs}	V_{DS} = 10 V V_{SB} = 0 V I_D = 20 mA, f = 1 kHz	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
	g_{os}		All	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V f = 1 MHz V_{GS} = V_{BS} = −15 V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
			SST Series	4.2							
Reverse Transfer Capacitance	C_{rss}		SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{d(on)}$	SD Series Only V_{SB} = 0 V, V_{IN} 0 to 5 V, R_G = 25 Ω V_{DD} = 5 V, R_L = 680 Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{d(off)}$			2							
	t_f			6							

Notes:
a. T_A = 25°C unless otherwise noted.
b. B is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.