SCOPE: IMPROVED, QUAD, SPST ANALOG SWITCHES

Device Type	Generic Number
01	DG411A(x)/883B
02	DG412A(x)/883B
03	DG413A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
K	E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
L	X	CDFP4-F16	16 LEAD FLATPACK	F16
Z	2	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

V^+ to V^- 44V
GND to V- 25V
Logic Supply Voltage (V_L) to V- 2/ ..... (GND-0.3V) to 44Vdc
Digital Inputs, V_S, V_D 2/ .....(V^-) -2Vdc to (V^+) +2Vdc
or 30mA whichever occurs first.
Continuous Current, Any terminal 30mA
Source or drain Current (Pulsed at 1ms, 10% duty cycle max) 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
16 lead FLATPACK(derate 6.1mW/°C above +70°C) 485mW
20 lead LCC (derate 9.1 mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 16 lead FLATPACK ..... 65°C/W
Case Outline 20 lead LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 16 lead FLATPACK ..... 165°C/W
Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Unipolar Supply Voltage (V^+) 12V
(V^-) 0V
Bipolar Supply Voltage (V^+) 15V
(V^-) 15V
Logic Supply Voltage (V_L) ..... +5.25V

NOTE 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2: Signals on SX, DX or INX exceeding V^+ or V^- are clamped by internal diodes. Limit forward current to maximum current ratings.

TABLE 1 ELECTRICAL TESTS

TEST	Symbol	CONDITIONS 1/ -55 °C <=T_A<= +125°C Unless otherwise specified		Group A Subgroup	Device type	Limits Min	Limits Max	Units
Drain-to-Source ON Resistance	$r_{DS(ON)}$	V+=13.5V V-=-13.5V I_S=-10mA V_D=±8.5V	V_{IN}=0.8V	1,3 2	01	0 0	35 45	Ω
			V_{IN}=2.4V	1,3 2	02	0 0	35 45	
			V_{IN}=0.8V or 2.4V 2/	1,3 2	03	0 0	35 45	
Drain-to-Source ON Resistance	$r_{DS(ON)}$	V+=10.8V V-=0V I_S=-10mA V_D=3.0V and 8.0V	V_{IN}=0.8V	1,3 2	01	0 0	80 100	Ω
			V_{IN}=2.4V	1,3 2	02	0 0	80 100	
			V_{IN}=0.8V or 2.4V 2/	1,3 2	03	0 0	80 100	
Source OFF leakage current and Drain OFF leakage current	$I_{S(OFF)}$ and $I_{D(OFF)}$	V+=16.5V V-=-16.5V V_D=-15.5V V_S=15.5V	V_{IN}=2.4V	1 2,3	01	-0.25 20.0	0.25 20.0	nA
			V_{IN}=0.8V	1 2,3	02	-0.25 -20.0	0.25 20.0	
			V_{IN}=0.8V or 2.4V 2/	1 2,3	03	-0.25 -20.0	0.25 20.0	
Source OFF leakage current and Drain OFF leakage current	$I_{S(OFF)}$ and $I_{D(OFF)}$	V+=16.5V V-=-16.5V V_D=15.5V V_S=-15.5V	V_{IN}=2.4V	1 2,3	01	-0.25 20.0	0.25 20.0	nA
			V_{IN}=0.8V	1 2,3	02	-0.25 -20.0	0.25 20.0	
			V_{IN}=0.8V or 2.4V 2/	1 2,3	03	-0.25 -20.0	0.25 20.0	
Channel ON leakage current	$I_{D(ON)}$ + $I_{S(ON)}$	V+=16.5V V-=-16.5V V_D=15.5V V_S=V_D=±15.5V	V_{IN}=2.4V	1 2,3	01	-0.4 40.0	0.4 40.0	nA
			V_{IN}=0.8V	1 2,3	02	-0.4 -40.0	0.4 40.0	
			V_{IN}=0.8V or 2.4V 2/	1 2,3	03	-0.4 -40.0	0.4 40.0	
Input current with V_{IN} low	I_{IL}	Input under test=0.8V, all others = 2.4V		1,2,3	All	-0.5	+0.5	µA
Input current with V_{IN} high	I_{IH}	Input under test=2.4V, all others = 0.8V		1,2,3	All	-0.5	+0.5	µA

TABLE 1 ELECTRICAL TESTS

TEST	Symbol	CONDITIONS 1/ -55 °C <=T_A<= +125°C Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Turn ON time	t_{ON}	See Figure 4, C_L=35pF, V_S=±10V, R_L=300Ω See Figure 4, V+=12V, V-=0V, V_S=±8V, C_L=35pF, R_L=300Ω	9,11 10 9,11 10	All All	0 0 0 0	175 240 250 400	nS
Turn OFF time	t_{OFF}	See Figure 4, C_L=35pF, V_S=±10V, R_L=300Ω See Figure 4, V+=12V, V-=0V, V_S=±8V, C_L=35pF, R_L=300Ω	9,11 10 9,11 10	All All	0 0 0 0	145 160 125 140	nS
Charge Injection	Q	See Figure 5, V_{GEN}=0V, R_{GEN}=0Ω, C_L=10nF See Figure 5, V_{GEN}=6.0V, R_{GEN}=0Ω,C_L=10nF, V+=12V, V-=0V	9	All	-100 -100	+100 +100	pC
Positive Supply Current	I+	V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V V+=13.2V, V-=0V, V_{IN}=0V or 5V, V_L=5.25V	1 2,3 1 2,3	All		+1.0 +5.0 +1.0 +5.0	µA
Negative Supply Current	I-	V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V V+=13.2V, V-=0V, V_{IN}=0V or 5V, V_L=5.25V	1 2,3 1 2,3	All	-1.0 -5.0 -1.0 -5.0		µA
Logic Supply Current	I_L	V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V V+=13.2V, V-=0V, V_{IN}=0V or 5V, V_L=5.25V	1 2,3 1 2,3	All		+1.0 +5.0 +1.0 +5.0	µA
Ground Current	I_{GND}	V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V V+=13.2V, V-=0V, V_{IN}=0V or 5V, V_L=5.25V	1 2,3 1 2,3	All	-1.0 -5.0 -1.0 -5.0		µA

NOTE 1: V+=15V, V-=-15V, V_L=5V and GND = 0V, unless otherwise specified.
NOTE 2: V_{IN}=input voltage to perform proper function.

Ordering Information.		SMD #	PKG.Code
01	DG411AK/883B	5962-9073101MEA	J16
01	DG411AL/883B	5962-9073101MXC	F16
01	DG411AZ/883B	5962-9073101M2A	L20
02	DG412AK/883B	5962-9073102MEA	J16
02	DG412AL/883B	5962-9073102MXC	F16
02	DG412AZ/883B	5962-9073102M2A	L20
03	DG413AK/883B	5962-9073103MEA	J16
03	DG413AL/883B	5962-9073103MXC	F16
03	DG413AZ/883B	5962-9073103M2A	L20

FIGURE 1 TERMINAL CONNECTIONS
DEVICE TYPES 01, 02, 03

CASE OUTLINES	SMD=E OR X MAXIM= K OR L		SMD = 2 MAXIM = Z	
TERMINAL NUMBER	TERMINAL SYMBOL		TERMINAL SYMBOL	
1	INPUT 1	IN1	NC	
2	DRAIN 1	D1	INPUT 1	IN1
3	SOURCE 1	S1	DRAIN 1	D1
4	V-		SOURCE 1	S1
5	GROUND	GND	V-	
6	SOURCE 4	S4	NC	
7	DRAIN 4	D4	GROUND	GND
8	INPUT 4	IN4	SOURCE 4	S4
9	INPUT 3	IN3	DRAIN 4	D4
10	DRAIN 3	D3	INPUT 4	IN4
11	SOURCE 3	S3	NC	
12	V_L		INPUT 3	IN3
13	V+		DRAIN 3	D3
14	SOURCE 2	S2	SOURCE 3	S3
15	DRAIN 2	D2	V_L	
16	INPUT2	IN2	NC	
17			V+	
18			SOURCE 2	S2
19			DRAIN 2	D2
20			INPUT 2	IN2

FIGURE 2. TRUTH TABLES

	DG411	DG412	DG413	DG413
SWITCH	1,2,3,4	1,2,3,4	1,4	2,3
LOGIC				
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

FIGURE 3:

Block Diagrams: See commercial datasheet or SMD 5962-90731

FIGURE 4:

TEST CIRCUITS: Switching Times. See commerical datasheet or SMD 5962-90731

FIGURE 5:

Charge Injection test circuit and waveforms. See Commercial datasheet or SMD 5962-90731

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125C, minimum
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.