NEC

MOS INTEGRATED CIRCUIT

μPD434016A

4M-BIT CMOS FAST SRAM
256K-WORD BY 16-BIT

Description

The μPD434016A is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

Operating supply voltage is 5.0 V ± 0.5 V.

The μPD434016A is packaged in 44-pin plastic SOJ and 44-pin plastic TSOP (II).

Features

- 262,144 words by 16 bits organization
- Fast access time : 12, 15, 17, 20 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Output Enable input for easy application
- Single +5.0 V power supply

Ordering Information

Part number	Package	Access time (MAX.)	Supply current (MAX.)	
			At operating	At standby
μPD434016ALE-12	44-pin plastic SOJ (400 mil)	12 ns	230 mA	10 mA
μPD434016ALE-15		15 ns	220 mA	
μPD434016ALE-17		17 ns	210 mA	
μPD434016ALE-20		20 ns	200 mA	
μPD434016AG5-12-7JF	44-pin plastic TSOP (II) (400 mil) (Normal bent)	12 ns	230 mA	
μPD434016AG5-15-7JF		15 ns	220 mA	
μPD434016AG5-17-7JF		17 ns	210 mA	
μPD434016AG5-20-7JF		20 ns	200 mA	

The information in this document is subject to change without notice.

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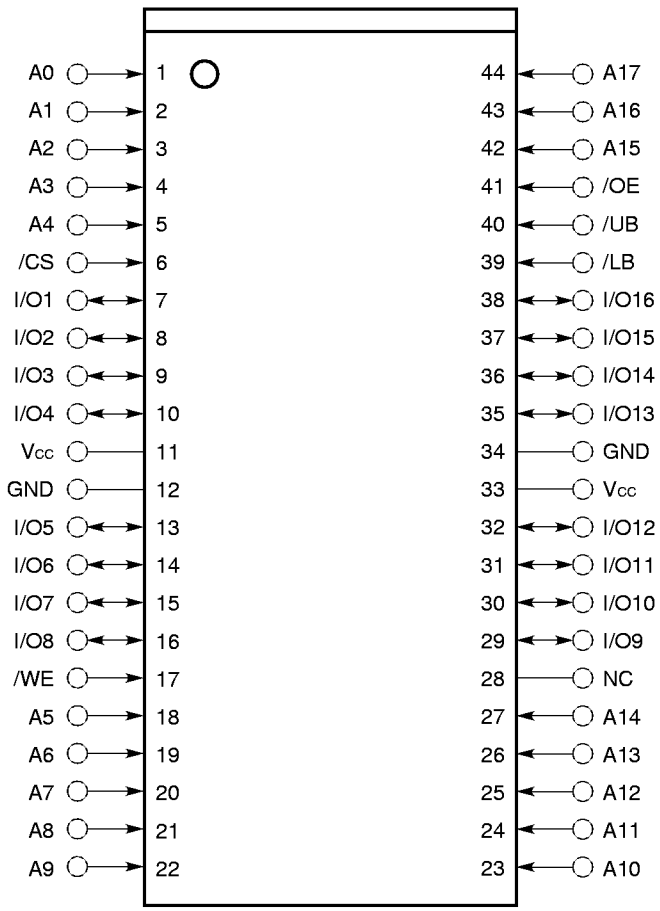
The mark ★ shows major revised points.

Pin Configurations (Marking Side)

/xxx indicates active low signal.

44-pin plastic SOJ (400 mil)

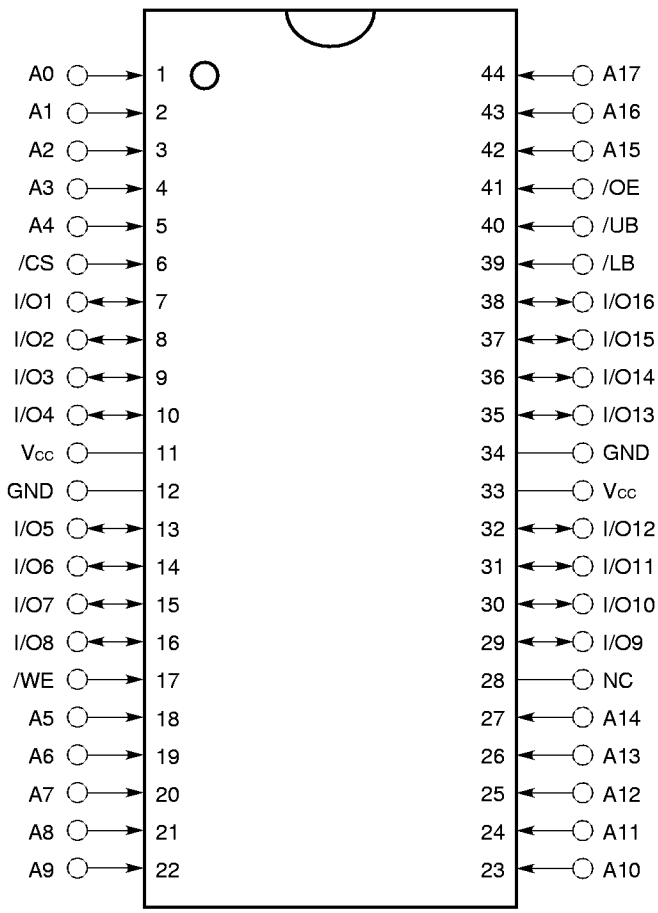
[μPD434016ALE]



A0 - A17	:	Address Inputs
I/O1 - I/O16	:	Data Inputs / Outputs
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

44-pin plastic TSOP (II) (400 mil) (Normal Bent)

[μPD434016AG5-7JF]



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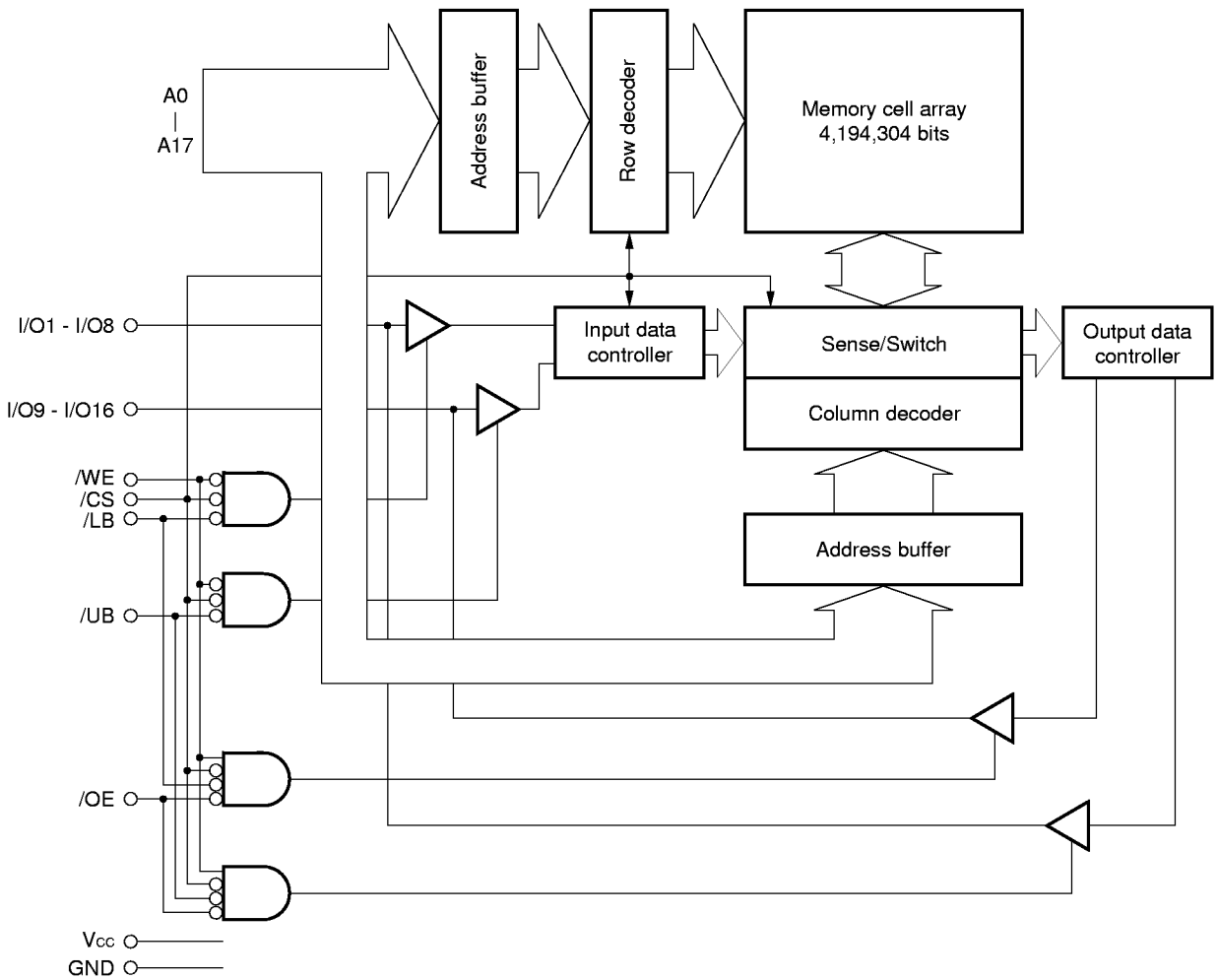
/LB, /UB	:	Byte data select
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Block Diagram



Truth Table

/CS	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
						I/O1 - I/O8	I/O9 - I/O16	
H	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
L	L	H	L	L	Read	D_{OUT}	D_{OUT}	I_{CC}
			L	H		D_{OUT}	High impedance	
			H	L		High impedance	D_{OUT}	
L	×	L	L	L	Write	D_{IN}	D_{IN}	
			L	H		D_{IN}	High impedance	
			H	L		High impedance	D_{IN}	
L	H	H	×	×	Output disable	High impedance	High impedance	
L	×	×	H	H		High impedance	High impedance	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 [Note] to +7.0	V
Input / Output voltage	V_T		–0.5 [Note] to V_{CC}+0.5	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –2.0 V (MIN.) (pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low level input voltage	V_{IL}		–0.5 [Note]		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Note –2.0 V (MIN.) (pulse width : 2 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–2		+2	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL} or /LB = V_{IH} or /UB = V_{IH}		–2		+2	μA
Operating supply current	I_{CC}	/CS = V_{IL}, $I_{I/O}$ = 0 mA, Minimum cycle time	Cycle time : 12 ns			230	mA
			Cycle time : 15 ns			220	
			Cycle time : 17 ns			210	
			Cycle time : 20 ns			200	
Standby supply current	I_{SB}	/CS = V_{IH}, V_{IN} = V_{IH} or V_{IL}				50	mA
	I_{SB1}	V_{CC} – 0.2 V ≤ /CS, V_{IN} ≤ 0.2 V or V_{CC} – 0.2 V ≤ V_{IN}				10	
High level output voltage	V_{OH}	I_{OH} = –4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA				0.4	V

Remark V_{IN} : Input voltage

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

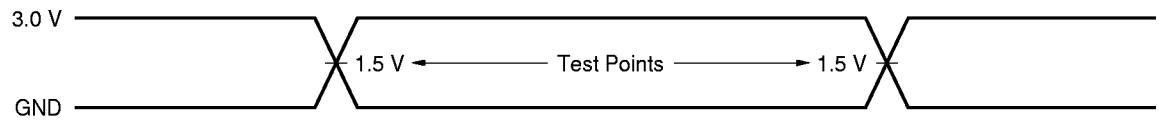
Remarks 1. V_{IN} : Input voltage

2. These parameters are periodically sampled and not 100% tested.

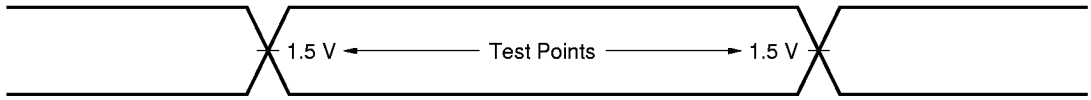
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

Figure 1

(for t_{AA}, t_{ACS}, t_{OE}, t_{ABD}, t_{OH})

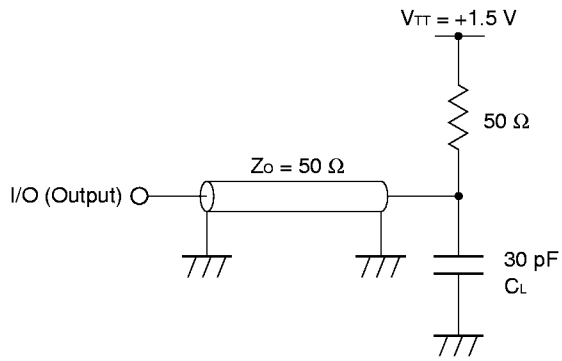
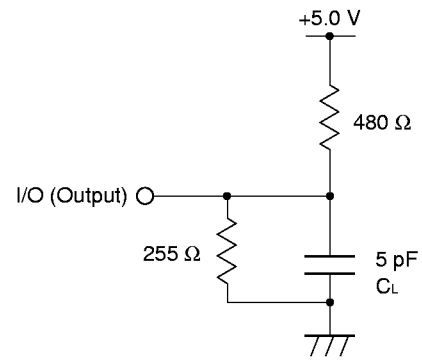


Figure 2

(for t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

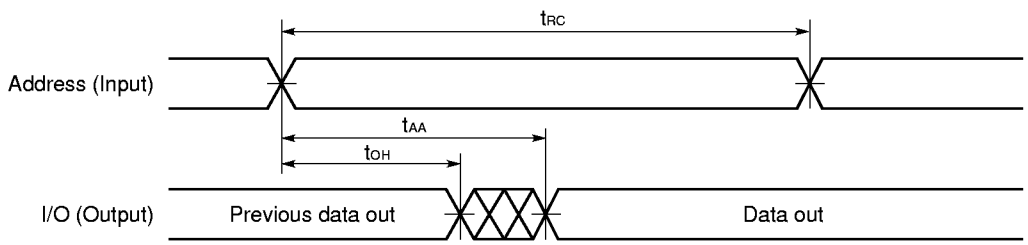
Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	12		15		17		20		ns	
Address access time	t_{AA}		12		15		17		20	ns	1
/CS access time	t_{ACS}		12		15		17		20	ns	
/OE access time	t_{OE}		6		7		8		10	ns	
/LB, /UB access time	t_{ABD}		6		7		8		10	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
/CS to output in low impedance	t_{CLZ}	3		3		3		3		ns	2, 3
/OE to output in low impedance	t_{OLZ}	0		0		0		0		ns	
/LB, /UB to output in low impedance	t_{BLZ}	0		0		0		0		ns	
/CS to output in high impedance	t_{CHZ}		6		7		8		8	ns	
/OE to output hold in high impedance	t_{OHZ}		6		7		8		8	ns	
/LB, /UB to output hold in high impedance	t_{BHZ}		6		7		8		8	ns	

Notes 1. See the output load shown in **Figure 1**.

2. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

3. These parameters are periodically sampled and not 100% tested.

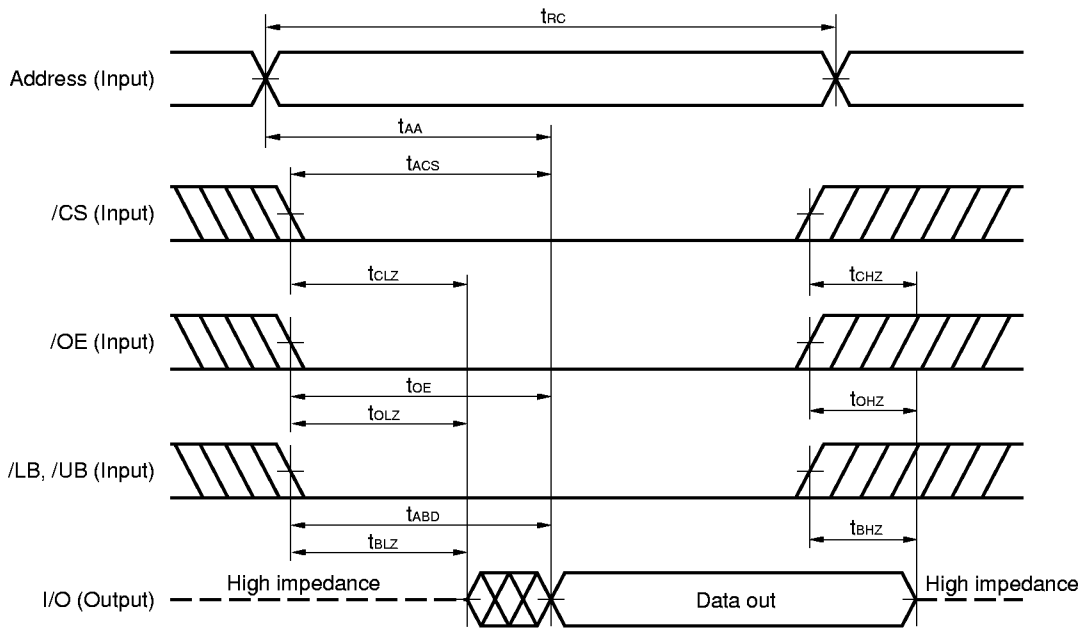
Read Cycle Timing Chart 1 (Address Access)



Remarks 1. In read cycle, /WE should be fixed to high level.

2. /CS = /OE = /LB (or /UB) = V_{IL}

Read Cycle Timing Chart 2 (/CS Access)



Caution Address valid prior to or coincident with /CS low level input.

Remark In read cycle, /WE should be fixed to high level.

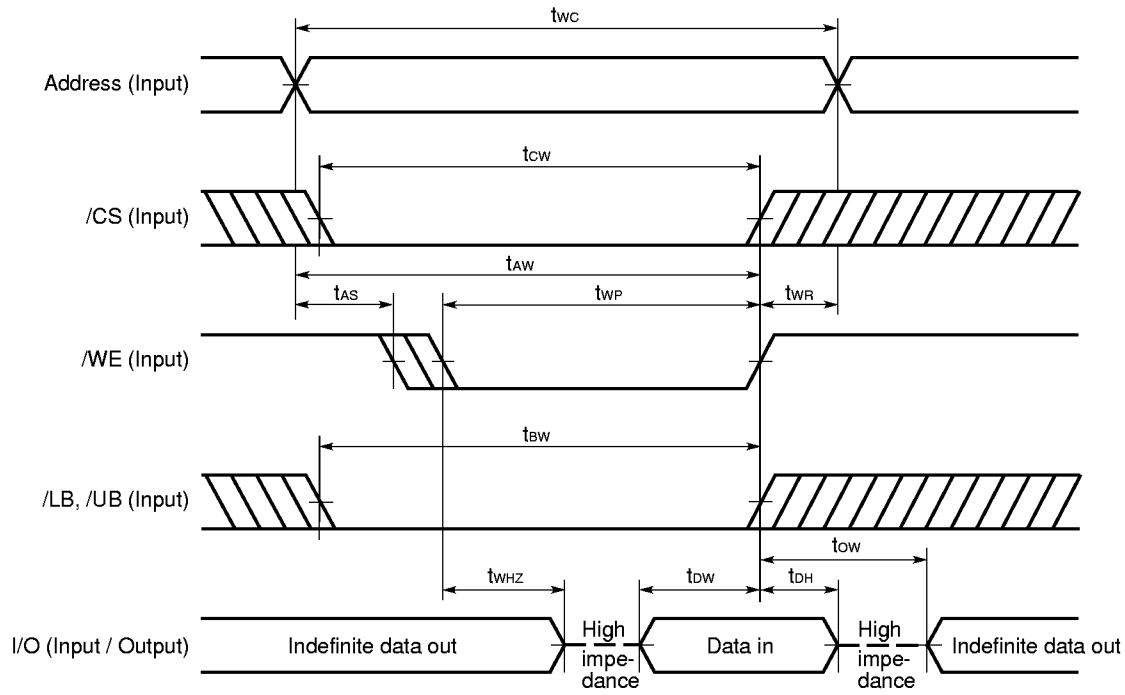
Write Cycle

	Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
	Write cycle time	t_{WC}	12		15		17		20		ns	
	/CS to end of write	t_{CW}	8		10		11		12		ns	
	Address valid to end of write	t_{AW}	8		10		11		12		ns	
	Write pulse width	t_{WP}	8		10		11		12		ns	
	/LB, /UB to end of write	t_{BW}	8		10		11		12		ns	
	Data valid to end of write	t_{DW}	6		7		8		9		ns	
	Data hold time	t_{DH}	0		0		0		0		ns	
	Address setup time	t_{AS}	0		0		0		0		ns	
★	Write recovery time	t_{WR}	1		1		1		1		ns	
	/WE to output in high impedance	t_{WHZ}		6		7		8		8	ns	1, 2
	Output active from end of write	t_{OW}	3		3		3		3		ns	

Notes 1. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

2. These parameters are periodically sampled and not 100% tested.

Write Cycle Timing Chart 1 (/WE Controlled)



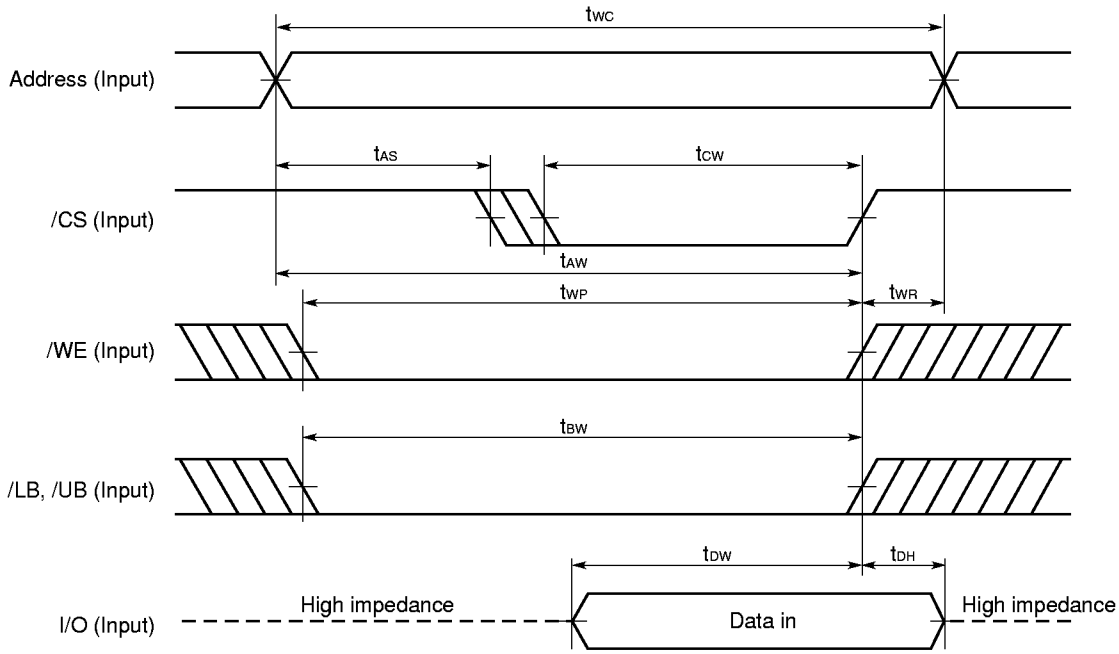
Caution /CS or /WE should be fixed to high level during address transition.

Remarks 1. Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

2. During t_{WHZ}, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

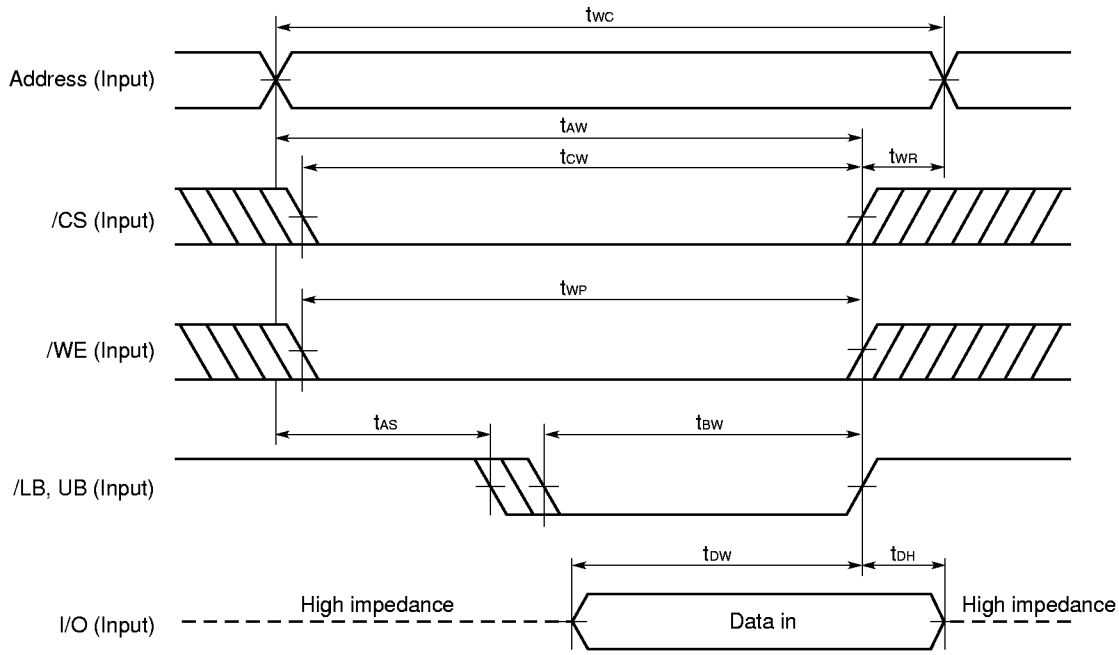
Write Cycle Timing Chart 2 (/CS Controlled)



Caution /CS or /WE should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)

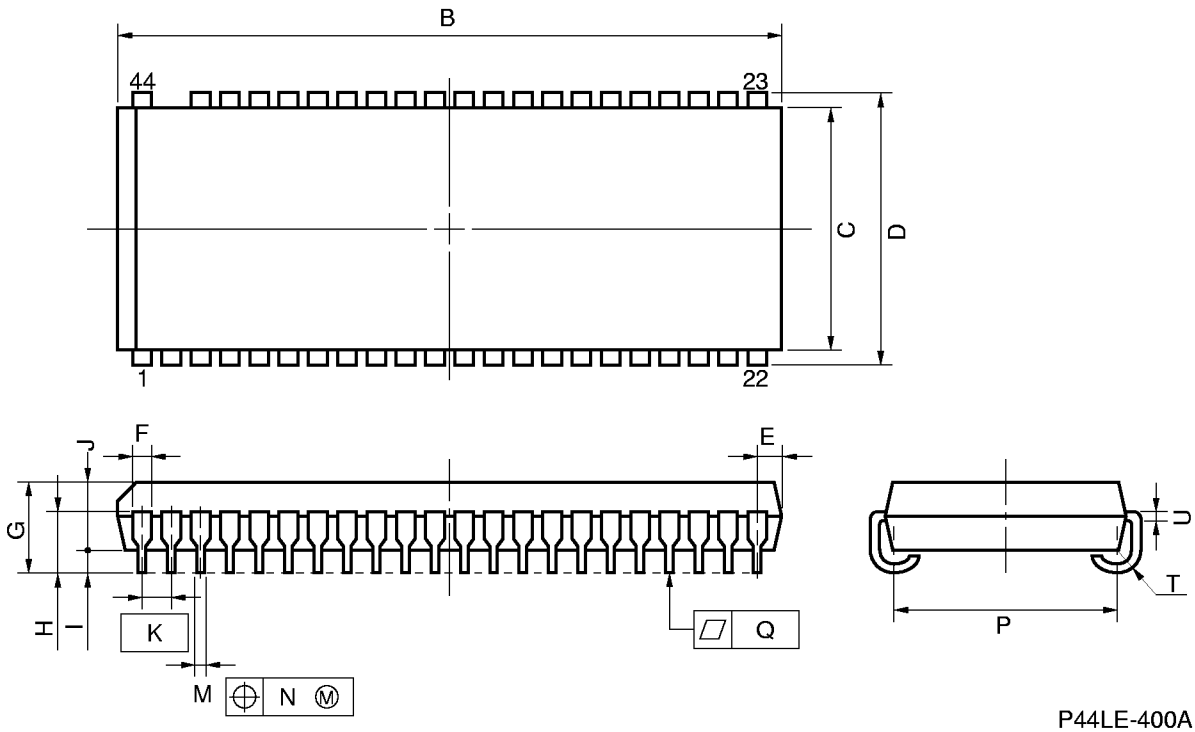


Caution /CS or /WE should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Package Drawings

44 PIN PLASTIC SOJ (400 mil)



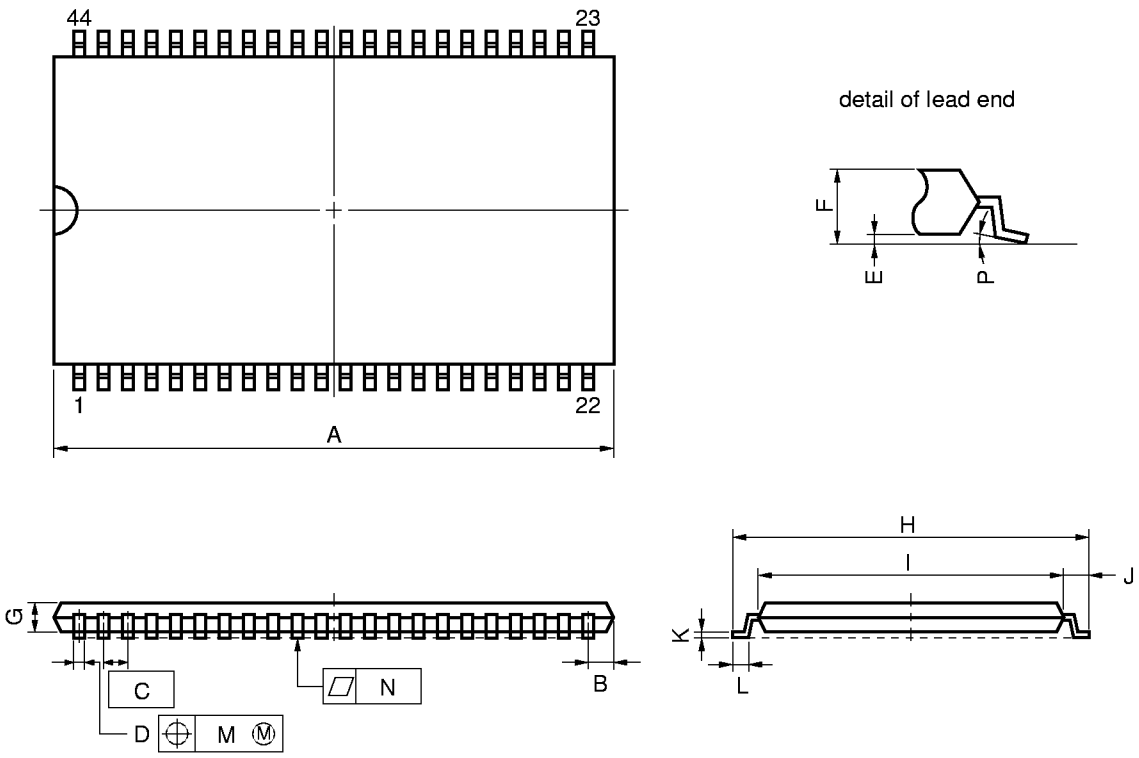
P44LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$28.73^{+0.2}_{-0.35}$	$1.131^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.20	0.440±0.008
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.3±0.2	$0.091^{+0.008}_{-0.009}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

44 PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S44G5-80-7JF5

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD434016A.

Type of Surface Mount Device

μPD434016ALE : 44-pin plastic SOJ (400 mil)

μPD434016AG5-7JF : 44-pin plastic TSOP (II) (400 mil) (Normal Bent)