

CD4071BM/CD4071BC **Quad 2-Input OR Buffered B Series Gate** **CD4081BM/CD4081BC** **Quad 2-Input AND Buffered B Series Gate**

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs protected against static discharge with diodes to V_{DD} and V_{SS} .

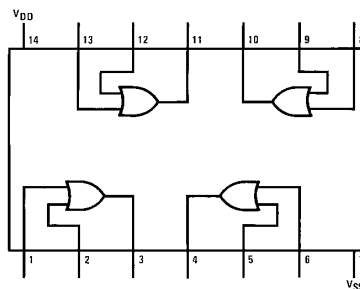
Features

- Low power TTL compatibility
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Fan out of 2 driving 74L or 1 driving 74LS

Connection Diagrams

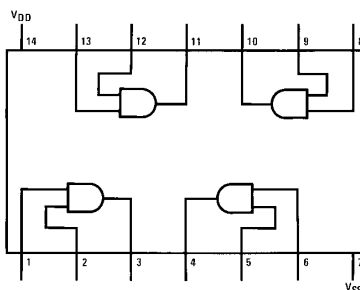
CD4071B Dual-In-Line Package



Top View

TL/F/5977–3

CD4081B Dual-In-Line Package



Top View

TL/F/5977–6

Order Number CD4071B or CD4081B

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature (T_S)	−65°C to +150°C

Lead Temperature (T_L)
(Soldering, 10 seconds)

260°C

Operating Conditions

Operating Range (V_{DD})	3 V_{DC} to 15 V_{DC}
Operating Temperature Range (T_A)	
CD4071BM, CD4081BM	−55°C to +125°C
CD4071BC, CD4081BC	−40°C to +85°C

DC Electrical Characteristics CD4071BM/CD4081BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$	$ I_O < 1 \mu A$	0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	$ I_O < 1 \mu A$	4.95		4.95	5		4.95	V
		$V_{DD} = 10V$		9.95		9.95	10		9.95	V
		$V_{DD} = 15V$		14.95		14.95	15		14.95	V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		−10 ^{−5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10 ^{−5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4071BC/CD4081BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		1 2 4		0.004 0.005 0.006	1 2 4		7.5 15 30	μA μA μA
V _{OL}	Low Level Output Voltage	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V	} I _O < 1 μA			0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V _{OH}	High Level Output Voltage	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V			4.95 9.95 14.95		5 10 15	4.95 9.95 14.95		V V V
V _{IL}	Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V V _{DD} = 10V, V _O = 1.0V V _{DD} = 15V, V _O = 1.5V		1.5 3.0 4.0		2 4 6	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V _{IH}	High Level Input Voltage	V _{DD} = 5V, V _O = 4.5V V _{DD} = 10V, V _O = 9.0V V _{DD} = 15V, V _O = 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	3 6 9		3.5 7.0 11.0		V V V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V V _{DD} = 10V, V _O = 0.5V V _{DD} = 15V, V _O = 1.5V	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V V _{DD} = 10V, V _O = 9.5V V _{DD} = 15V, V _O = 13.5V	−0.52 −1.3 −3.6		−0.44 −1.1 −3.0	−0.88 −2.25 −8.8		−0.36 −0.9 −2.4		mA mA mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V V _{DD} = 15V, V _{IN} = 15V		−0.30 0.30		−10 ^{−5} 10 ^{−5}	−0.30 0.30		−1.0 1.0	μA μA

AC Electrical Characteristics* CD4071BC/CD4071BM

T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, Typical temperature coefficient is 0.3%/°C

Symbol	Parameter	Conditions	Typ	Max	Units
t _{PHL}	Propagation Delay Time, High-to-Low Level	V _{DD} = 5V	100	250	ns
		V _{DD} = 10V	40	100	ns
		V _{DD} = 15V	30	70	ns
t _{PLH}	Propagation Delay Time, Low-to-High Level	V _{DD} = 5V	90	250	ns
		V _{DD} = 10V	40	100	ns
		V _{DD} = 15V	30	70	ns
t _{THL} , t _{TLH}	Transition Time	V _{DD} = 5V	90	200	ns
		V _{DD} = 10V	50	100	ns
		V _{DD} = 15V	40	80	ns
C _{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C _{PD}	Power Dissipation Capacity	Any Gate	18		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* CD4081BC/CD4081BM

$T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, Typical temperature coefficient is $0.3\%/^\circ\text{C}$

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	100 40 30	250 100 70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	120 50 35	250 100 70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	90 50 40	200 100 80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

*AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics

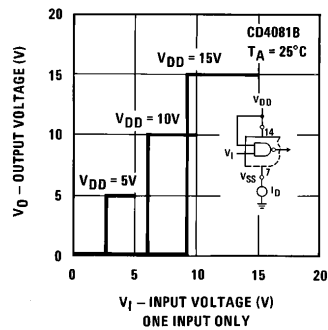


FIGURE 1. Typical Transfer Characteristics

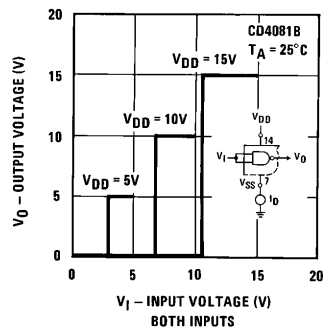


FIGURE 2. Typical Transfer Characteristics

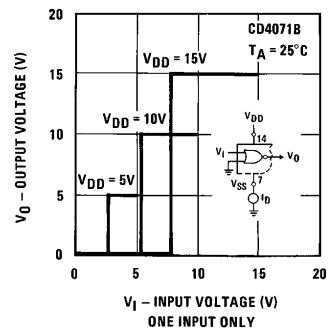


FIGURE 3. Typical Transfer Characteristics

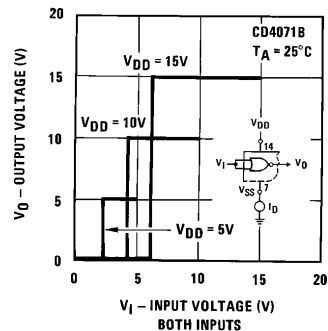


FIGURE 4. Typical Transfer Characteristics

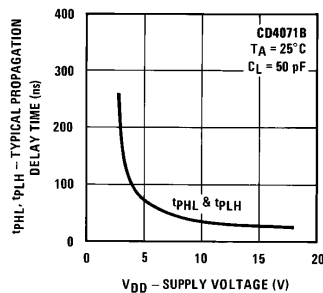


FIGURE 5

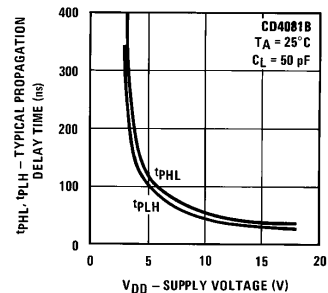


FIGURE 6

Typical Performance Characteristics (Continued)

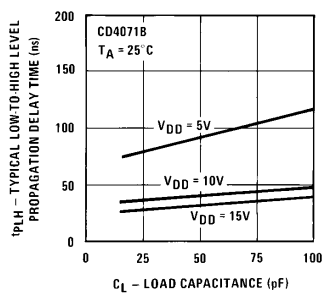


FIGURE 7

TL/F/5977-13

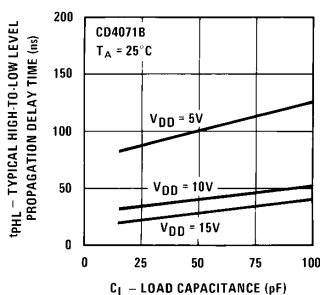


FIGURE 8

TL/F/5977-14

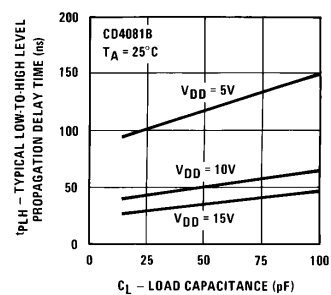


FIGURE 9

TL/F/5977-15

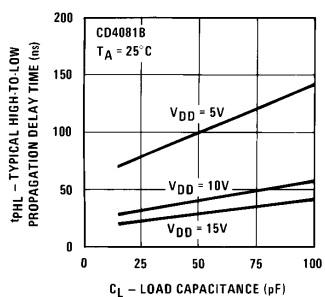


FIGURE 10

TL/F/5977-16

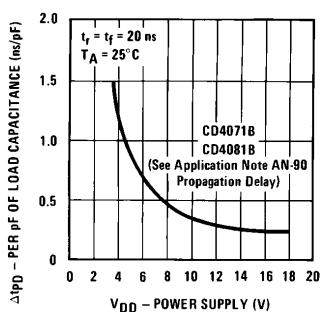


FIGURE 11

TL/F/5977-17

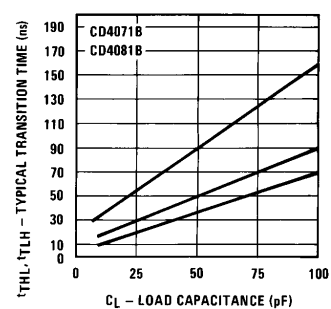


FIGURE 12

TL/F/5977-18

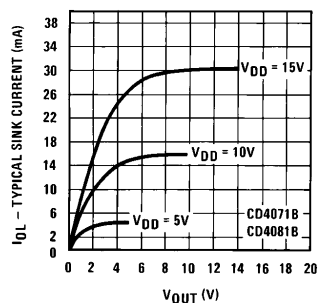


FIGURE 13

TL/F/5977-19

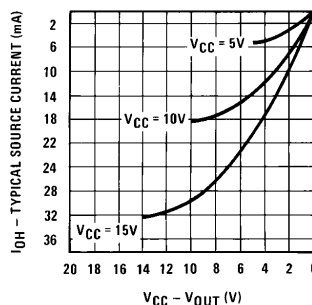
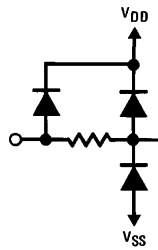
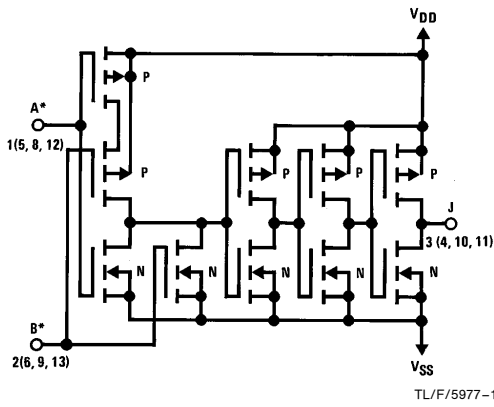


FIGURE 14

TL/F/5977-20

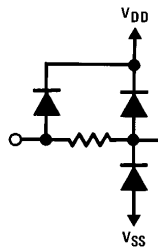
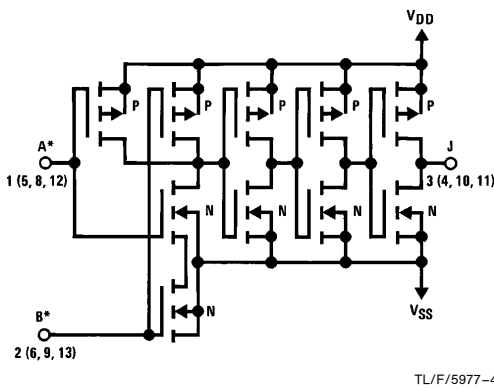
Schematic Diagrams

CD4071B



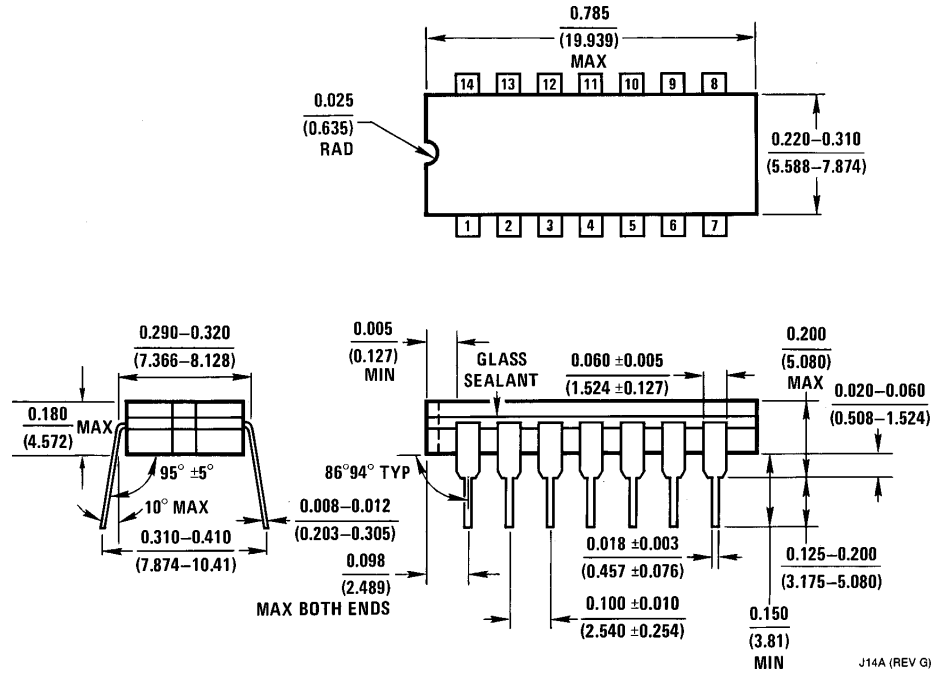
1/4 of device shown
 $J = A + B$
 Logical "1" = High
 Logical "0" = Low
 *All inputs protected by standard CMOS protection circuit.

CD4081B



1/4 of device shown
 $J = A \cdot B$
 Logical "1" = High
 Logical "0" = Low
 *All inputs protected by standard CMOS protection circuit.

Physical Dimensions inches (millimeters)

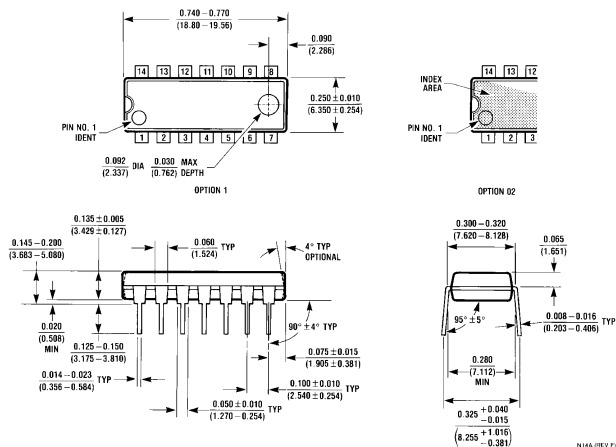


Ceramic Dual-In-Line Package (J)
Order Number CD4071BMJ, CD4071BCJ
CD4081BMJ or CD4081BCJ
NS Package Number J14A

J14A (REV G)

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4071BMN, CD4071BCN
CD4081BMN or CD4081BCN
NS Package Number N14A

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