

NTE5570, NTE5572, & NTE5574 Silicon Controlled Rectifier for Phase Control Applications

Electrical Characteristics: (Maximum values @ $T_J = +125^\circ\text{C}$ unless otherwise specified)

Repetitive Peak Voltages, V_{DRM} & V_{RRM}

NTE5570	200V
NTE5572	600V
NTE5574	1200V

Non-Repetitive Peak Reverse Blocking Voltage, V_{RSM}

NTE5570	500V
NTE5572	900V
NTE5574	1300V

Average On-State Current (Half Sine Wave, 180° , $T_C = +85^\circ\text{C}$), $I_{\text{T(AV)}}$ 80A

RMS On-State Current (DC @ $T_C = +75^\circ\text{C}$), $I_{\text{T(RMS)}}$ 125A

Peak One-Cycle, Non-Repetitive Surge Current (10ms Duration, Sinusoidal Half Wave), I_{TSM}

No Voltage Reapplied	1900A
100% V_{RRM} Reapplied	1600A

Maximum I^2t for Fusing (10ms Duration, Sinusoidal Half Wave), I^2t

No Voltage Reapplied	18000A ² sec
100% V_{RRM} Reapplied	12700A ² sec

Peak Positive Gate Current (5ms Pulse Width), I_{GM} 3A

Peak Positive Gate Voltage (5ms Pulse Width), $+V_{\text{GM}}$ 20V

Peak Negative Gate Voltage (5ms Pulse Width), $-V_{\text{GM}}$ 10V

Average Gate Power ($f = 50\text{Hz}$, Duty Cycle = 50%), P_{G} 3W

Peak Gate Power (50ms Pulse Width), P_{GM} 12W

Rate of Rise of Off-State Voltage (Exponential to 67% Rated V_{DRM}), dv/dt 500V/ μs

Rate of Rise of ON-State Current, di/dt

(Gate Drive 20V, 65 Ω , with $t_r = 0.5\mu\text{s}$, $V_d = \text{Rated } V_{\text{DRM}}$, $I_{\text{TM}} = 2 \times di/dt$ snubber 0.2 μF)

Non-Repetitive 300A/ μs

Typical Delay Time, t_d

(Gate Pulse: 10V, 15 Ω Source, $t_p = 6\mu\text{s}$, $t_r = 0.1\mu\text{s}$, $V_d = \text{rated } V_{\text{DRM}}$, $I_{\text{TM}} = 50\text{A}$) 1 μs

Typical Turn-On Time, t_q

($I_{\text{TM}} = 50\text{A}$, $di/dt = -5\text{A}/\mu\text{s}$ min, $V_R = 50\text{V}$, $dv/dt = 20\text{V}/\mu\text{s}$, Gate Bias: 0V 25 Ω , $t_p = 500\mu\text{s}$) 110 μs

On-State Voltage ($I_{\text{PK}} = 250\text{A}$, 10ms Sine Pulse), V_{TM} 1.6V

Repetitive Peak Off-State Current (At V_{DRM}), I_{DRM} 15mA

Repetitive Peak Reverse Current (At V_{RRM}), I_{RRM} 15mA

Maximum Gate Current Required to Trigger, I_{GT}

(6V Anode-to-Cathode Applied, $T_J = +25^\circ\text{C}$) 120mA

Maximum Gate Voltage Required to Trigger, V_{GT}

(6V Anode-to-Cathode Applied, $T_J = +25^\circ\text{C}$) 2.5V

Maximum Holding (Anode Supply 12V Resistive Load, $T_J = +25^\circ\text{C}$), I_{H} 150mA

Maximum Gate Voltage which will not Trigger any Device, V_{GD} 0.25V

Electrical Characteristics (Cont'd): (Maximum values @ $T_J = +125^\circ\text{C}$ unless otherwise specified)

Operating Temperature Range, T_J	-40° to $+125^\circ\text{C}$
Storage Temperature Range, T_{stg}	-40° to $+150^\circ\text{C}$
Thermal Resistance, Junction-to-Case (DC Operation), R_{thJC}	0.3°C/W
Thermal Resistance, Case-to-Heat Sink, $R_{\text{thC-HS}}$ (Mounting Surface Smooth, Flat, and Greased)	0.1°C/W

