

Octal latched transceiver with dual enable,  
inverting (3-State)

74ABT544

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/−32mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17

- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ( $\overline{LEAB}$ ,  $\overline{LEBA}$ ) and Output Enable ( $\overline{OEAB}$ ,  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

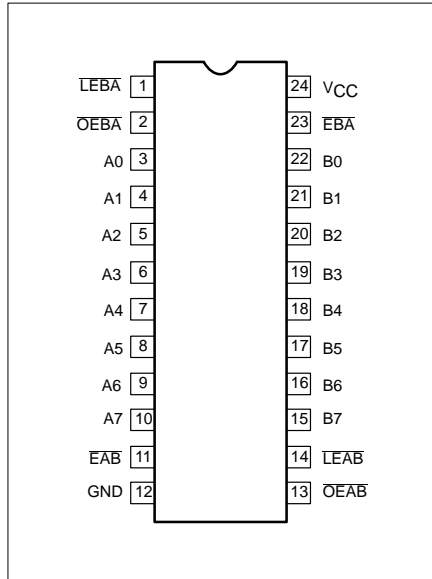
The 'ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ( $\overline{EAB}$ ) input and the A-to-B Latch Enable ( $\overline{LEAB}$ ) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the  $\overline{LEAB}$  signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With  $\overline{EAB}$  and  $\overline{OEAB}$  both Low, the 3-State B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the  $\overline{EBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

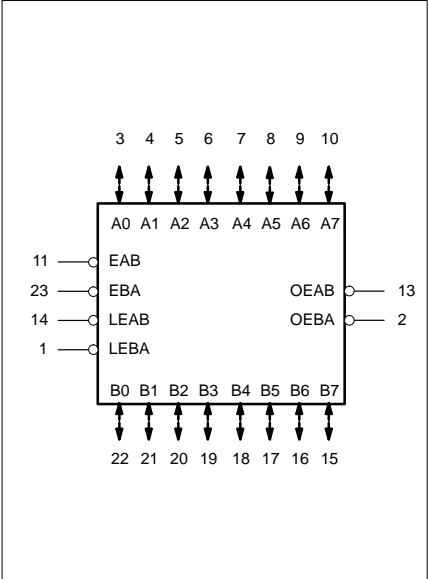
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	−40°C to +85°C	74ABT544N	0410D
24-pin plastic SOL	−40°C to +85°C	74ABT544D	0173D
24-pin plastic SSOP Type II	−40°C to +85°C	74ABT544DB	1641A

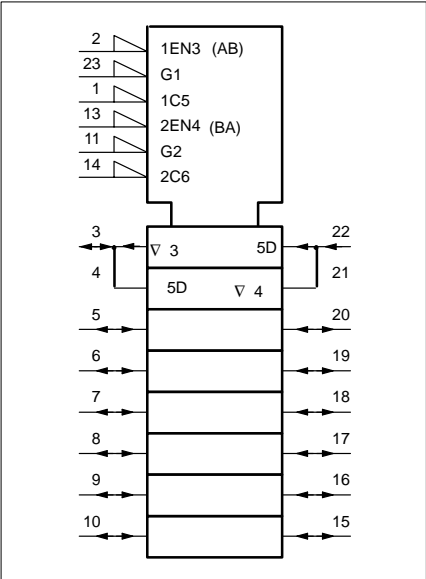
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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74ABT544

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{\text{LEAB}} / \overline{\text{LEBA}}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{\text{EAB}} / \overline{\text{EBA}}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{\text{OEAB}} / \overline{\text{OEBA}}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{\text{A0}} - \overline{\text{A7}}$	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	$\overline{\text{B0}} - \overline{\text{B7}}$	Port B, 3-State outputs
12	GND	Ground (0V)
24	$V_{\text{CC}}$	Positive supply voltage

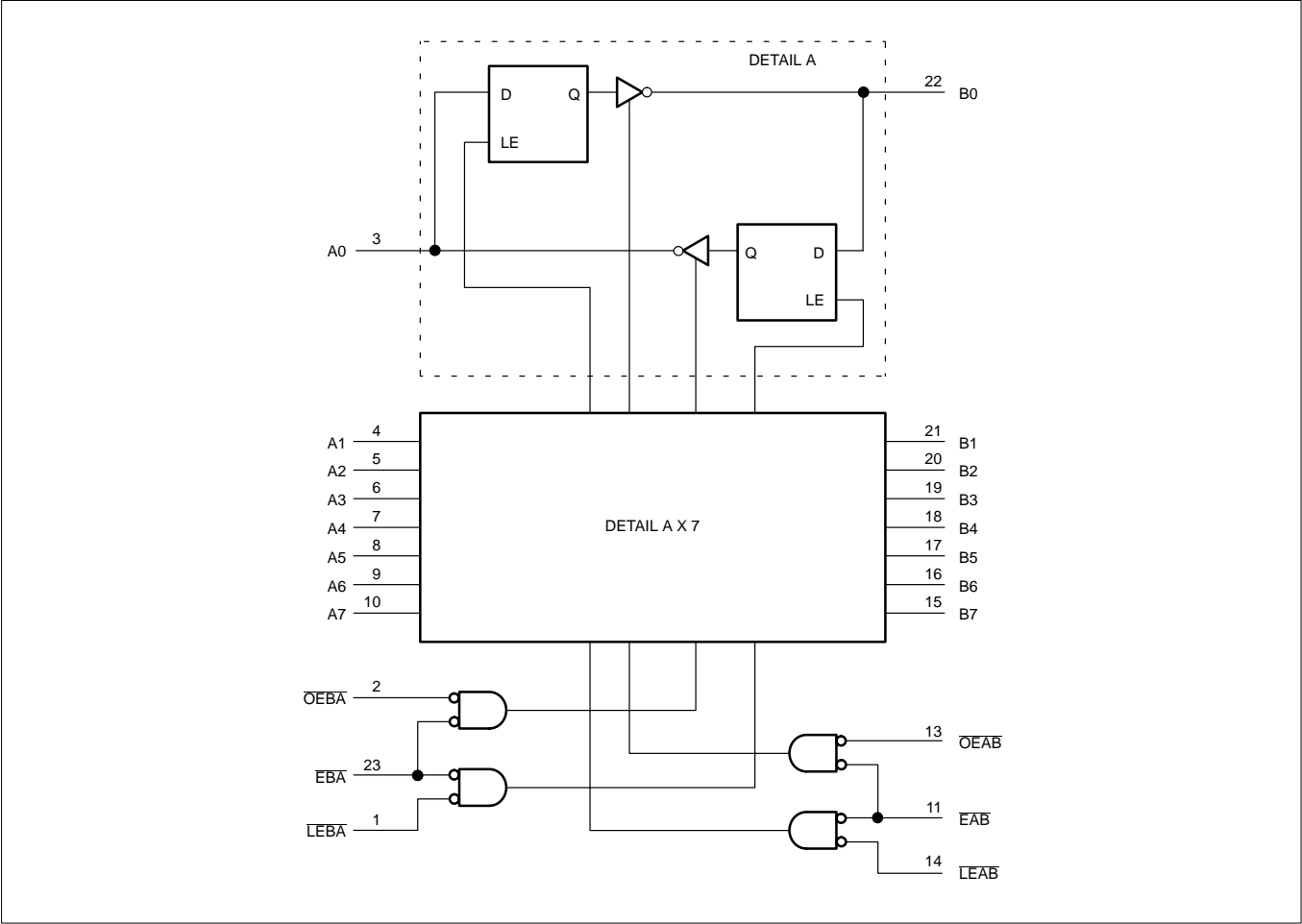
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay $\overline{\text{A}}_n$ to $\overline{\text{B}}_n$ or $\overline{\text{B}}_n$ to $\overline{\text{A}}_n$	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$	3.9	ns
$C_{\text{IN}}$	Input capacitance	$V_I = 0\text{V}$ or $V_{\text{CC}}$	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_O = 0\text{V}$ or $V_{\text{CC}}$	7	pF
$I_{\text{CCZ}}$	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	110	$\mu\text{A}$

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74ABT544

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OEXX	EXX	LEXX	An or Bn	An or Bn	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	L	Latch + Display
L	L	↑	l	H	
L	L	L	H	L	Transparent
L	L	L	L	H	
L	L	H	X	NC	Hold

H = High voltage level  
h = High voltage level one set-up time prior to the Low-to-High clock transition  
L = Low voltage level  
l = Low voltage level one set-up time prior to the Low-to-High clock transition  
X = Don't care  
↑ = Low-to-High clock transition  
NC= No change  
Z = High impedance or "off" state

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74ABT544

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		−0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	−18	mA
$V_I$	DC input voltage <sup>3</sup>		−1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	−50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	−0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
$T_{stg}$	Storage temperature range		−65 to 150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level Input voltage		0.8	V
$I_{OH}$	High-level output current		−32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_{amb}$	Operating free-air temperature range	−40	+85	°C

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74ABT544

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T <sub>amb</sub> = +25°C			T <sub>amb</sub> = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = −18mA		−0.9	−1.2		−1.2	V
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = −3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	3.2		2.5		V
			V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = −3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.7		3.0		V
			V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = −32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.3		2.0		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
V <sub>RST</sub>	Power-up output low voltage <sup>3</sup>		V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V
I <sub>I</sub>	Input leakage current	Control pins	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±5	±100		±100	μA
I <sub>OFF</sub>	Power-off leakage current		V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5V		±5.0	±100		±100	μA
I <sub>PU/PD</sub>	Power-up/down 3-State output current <sup>4</sup>		V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = Don't care		±5.0	±50		±50	μA
I <sub>IH</sub> + I <sub>OZH</sub>	3-State output High current		V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	μA
I <sub>IL</sub> + I <sub>OZL</sub>	3-State output Low current		V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		−5.0	−50		−50	μA
I <sub>CEX</sub>	Output high leakage current		V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>		V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	−50	−65	−180	−50	−180	mA
I <sub>CCH</sub>	Quiescent supply current		V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		110	250		250	μA
I <sub>CCL</sub>				20	30		30	mA	
I <sub>CCZ</sub>				110	250		250	μA	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>		V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		0.3	1.5		1.5	mA

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any  $V_{CC}$  between 0V and 2.1V, with a transition of 10msec. From  $V_{CC} = 2.1\text{V}$  to  $V_{CC} = 5\text{V} \pm 10\%$ , a transition time of up to 100 $\mu\text{sec}$  is permitted.

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74ABT544

## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Bn, Bn to An	2	1.1 1.4	3.6 3.9	5.1 5.4	1.1 1.4	6.1 6.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LEBA to An, LEAB to Bn	1, 2	1.6 2.1	4.1 4.6	5.6 6.1	1.6 2.1	6.6 7.1	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time OEBA to An, OEAB to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time OEBA to An, OEAB to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time EBA to An, EAB to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time EBA to An, EAB to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns

## AC SETUP REQUIREMENTS

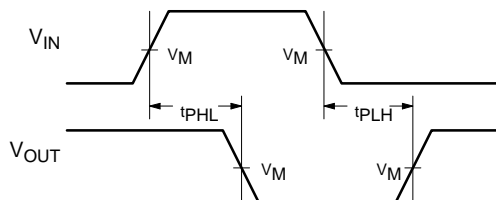
GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time An to LEAB, Bn to LEBA	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time An to LEAB, Bn to LEBA	3	0.5 0.5	-0.3 -1.3	0.5 0.5	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time An to EAB, Bn to EBA	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time An to EAB, Bn to EBA	3	0.5 0.5	-0.2 -1.3	0.5 0.5	ns
$t_w(\text{L})$	Latch enable pulse width, Low	3	3.5	1.8	3.5	ns

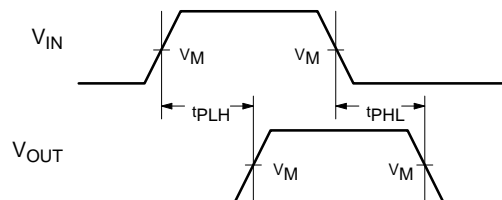
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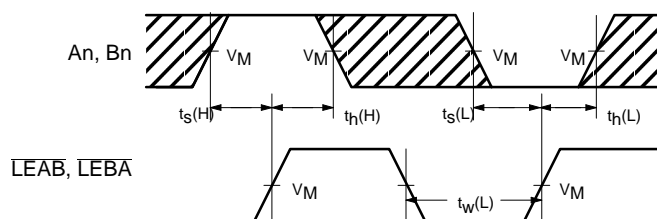
## AC WAVEFORMS

 $V_M = 1.5V$ ,  $V_{IN} = GND$  to  $3.0V$ 


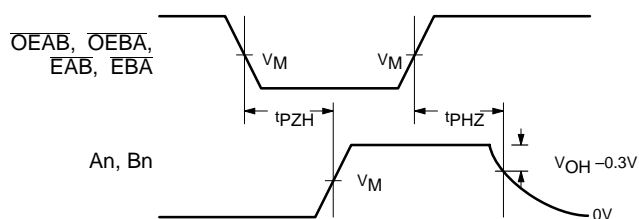
Waveform 1. Propagation Delay For Inverting Output



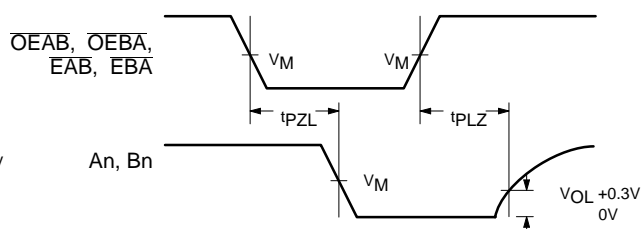
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

**NOTE:** The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORM

