

# DATA SHEET

**74ABT16241A**  
**74ABTH16241A**  
16-bit buffer/driver (3-State)

Product specification  
Supersedes data of 1997 Jun 12  
IC23 Data Handbook

1998 Feb 25

# 16-bit buffer/driver (3-State)

**74ABT16241A**  
**74ABTH16241A**

## FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16241A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74ABT16241A is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-State outputs.

Two options are available, 74ABT16241A which does not have the bus hold feature and 74ABTH16241A which incorporates the bus hold feature.

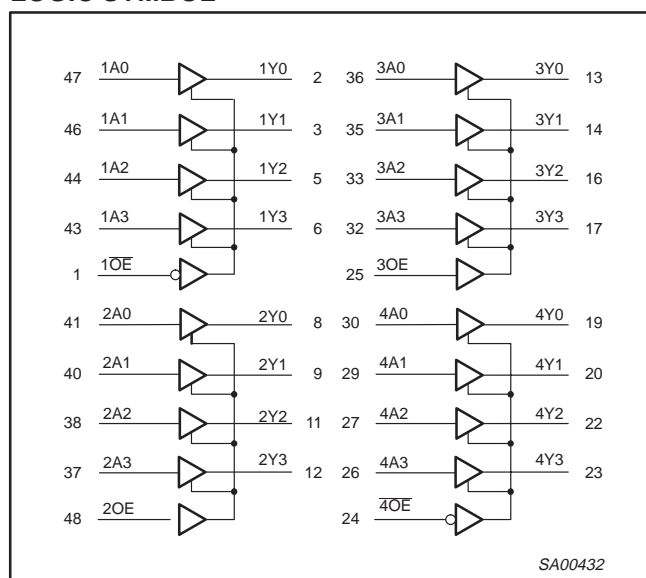
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nAx to nYx	$C_L = 50\text{pF}$ ; $V_{CC} =$	1.8 1.6	ns
$C_{IN}$	Input capacitance nOE	$V_I = 0\text{V}$ or 3.0V	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or	6	pF
$I_{CCZ}$	Quiescent supply current	Outputs disabled; $V_{CC} =$	500	$\mu\text{A}$
$I_{CCL}$		Outputs low; $V_{CC} = 5.5\text{V}$	8	mA

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT16241A DL	BT16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT16241A DGG	BT16241A DGG	SOT362-1
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABTH16241A DL	BH16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABTH16241A DGG	BH16241A DGG	SOT362-1

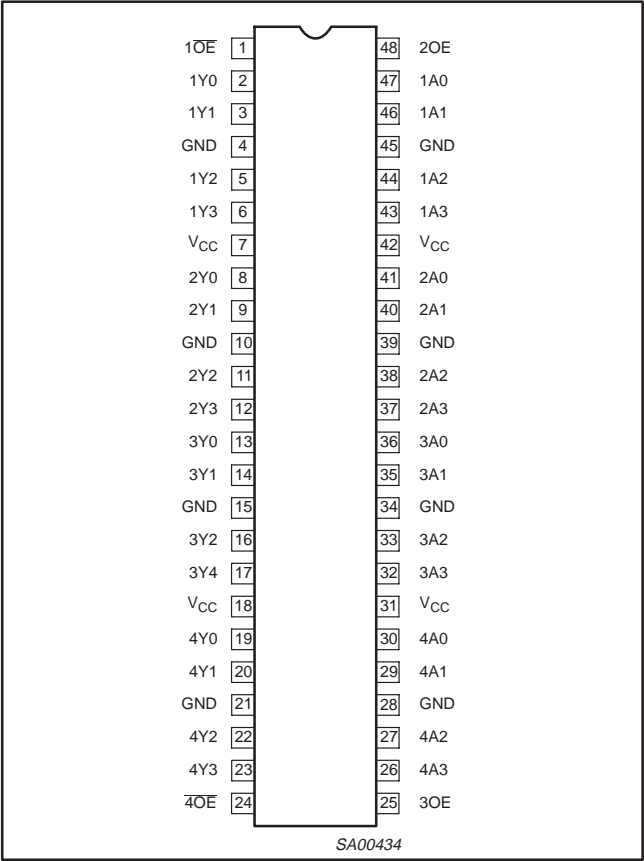
## LOGIC SYMBOL



16-bit buffer/driver (3-State)

74ABT16241A  
74ABTH16241A

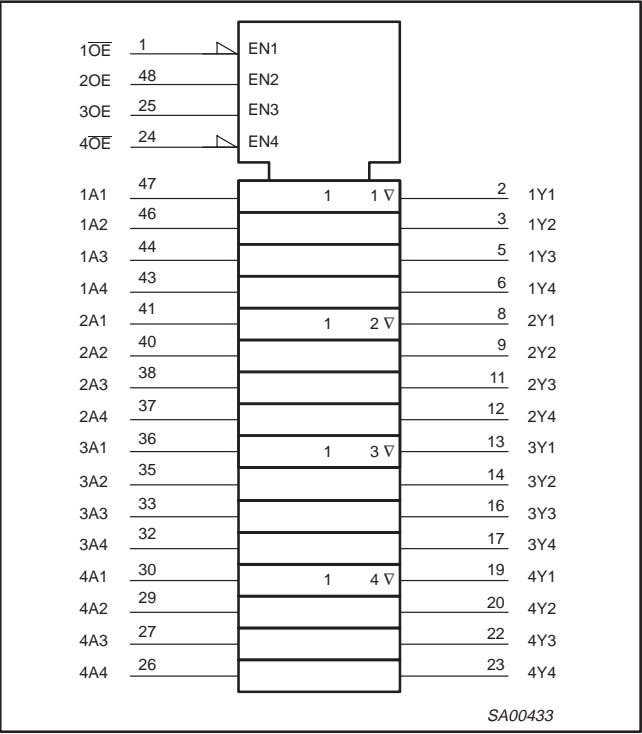
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

Inputs		Outputs
1OE, 4OE	1An, 4An	1Yn, 4Yn
L	L	L
L	H	H
H	X	Z
2OE, 3OE	2An, 3An	2Yn, 3Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High Impedance "off" state

## 16-bit buffer/driver (3-State)

74ABT16241A  
74ABTH16241AABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	Output in Low state	128	mA
		Output in High state	-64	
$T_{stg}$	Storage temperature range		-65 to +150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{kHz}$		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## 16-bit buffer/driver (3-State)

74ABT16241A  
74ABTH16241A

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA			-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>			0.42	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V			±0.01	±1.0		±1.0	μA
I <sub>I</sub>	Input leakage current 74ABTH16241A	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		±0.01	±1		±1	μA
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub>	Data pins		0.01	1		1	μA
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0			-2	-3		-5	μA
I <sub>HOLD</sub>	Bus Hold current A inputs <sup>3</sup> 74ABTH16241A	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0.8V		75			75		μA
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.0V		-75			-75		
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0 to 5.5V		±500					
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V			±5.0	±100		±100	μA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = V <sub>CC</sub>			±5.0	±50		±50	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>			1.0	10		10	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>			-1.0	-10		-10	μA
I <sub>CEX</sub>	Output high leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>			1.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V		-50	-70	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>			0.5	1.0		1.0	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>			8	19		19	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>			0.5	1.0		1.0	mA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	Outputs enabled, one input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V			10	200		200	μA

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

## AC CHARACTERISTICS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

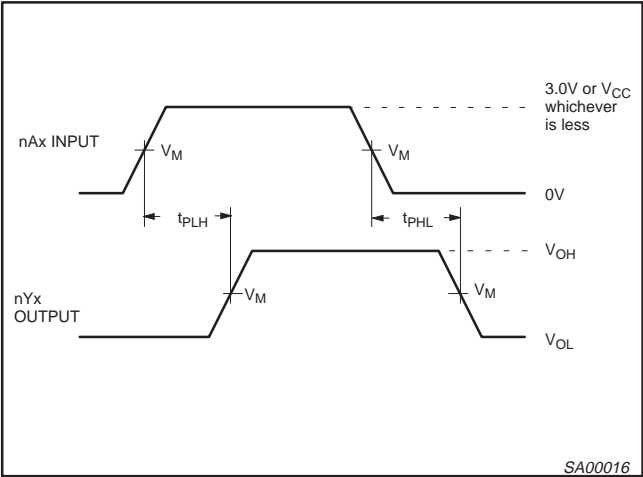
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nAx to nYx	1	1.0 1.0	1.8 1.6	2.6 2.4	1.0 1.0	3.1 2.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	2	1.0 1.0	2.4 2.6	3.4 4.6	1.0 1.0	3.9 5.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	2	1.3 1.3	3.0 2.4	4.3 3.6	1.0 1.0	5.3 4.2	ns

16-bit buffer/driver (3-State)

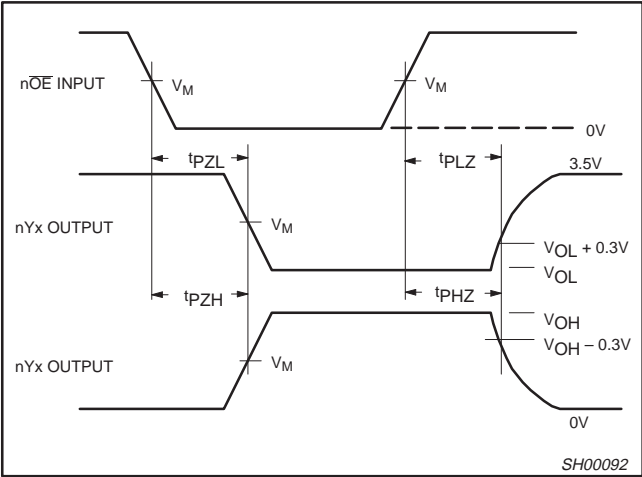
74ABT16241A  
74ABTH16241A

AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $2.7V$

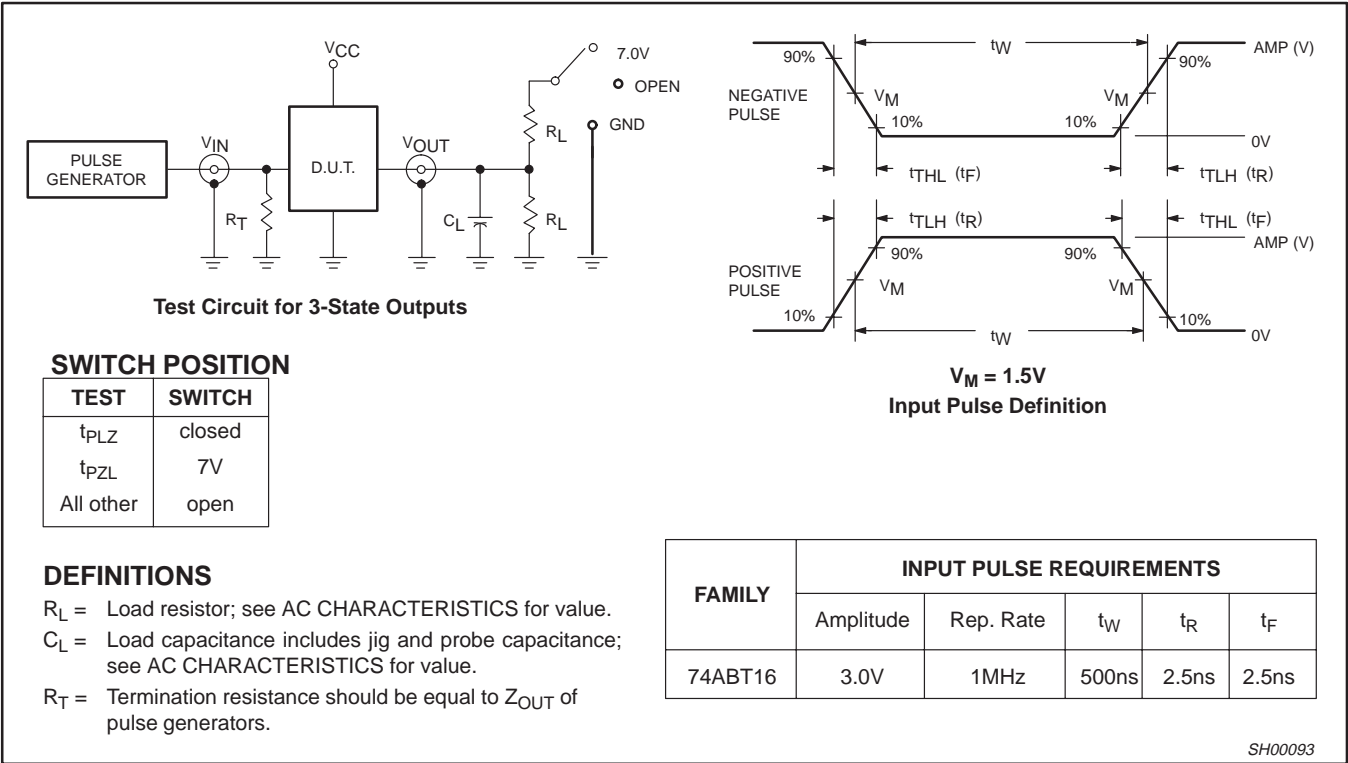


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

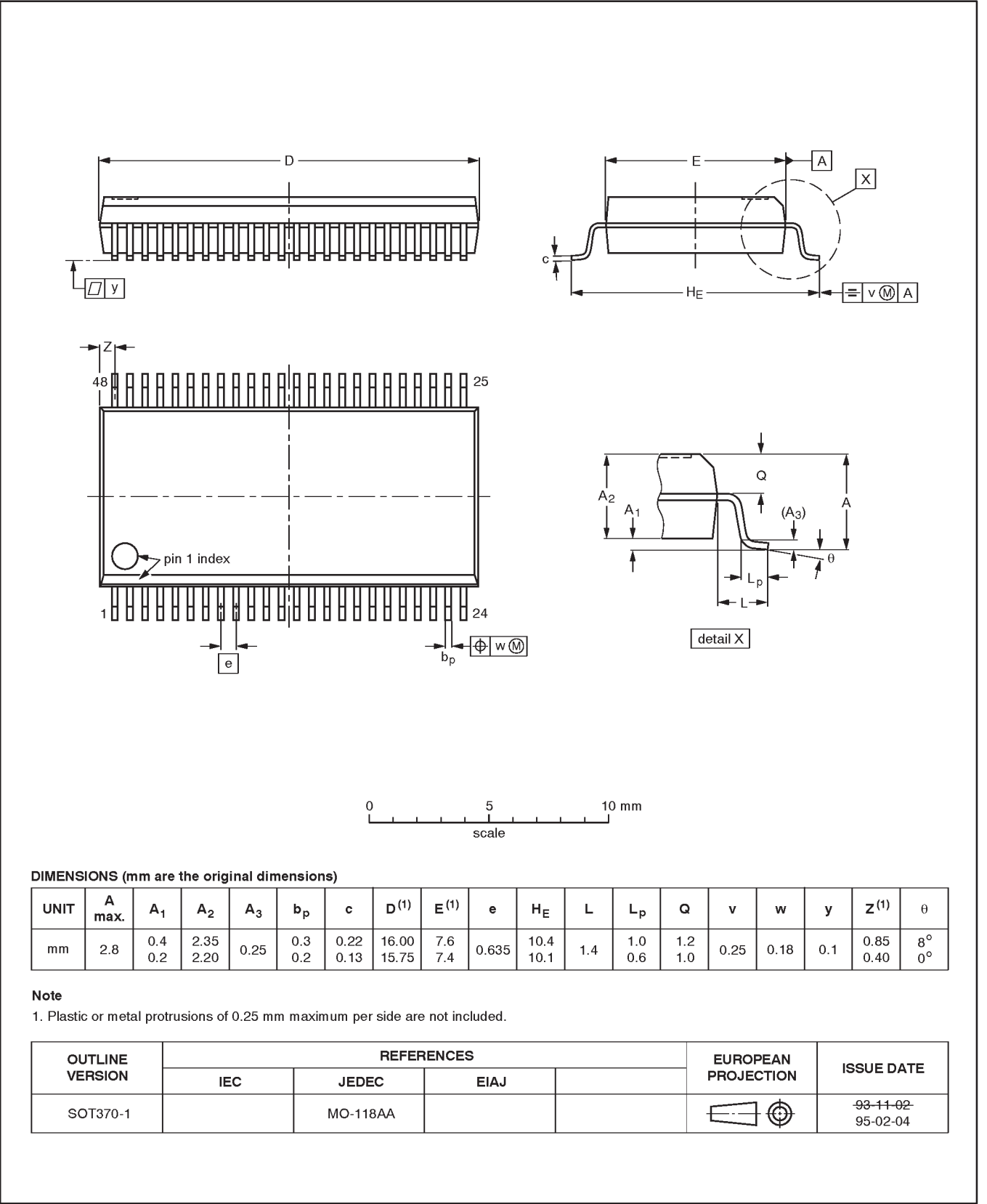


16-bit buffer/driver (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

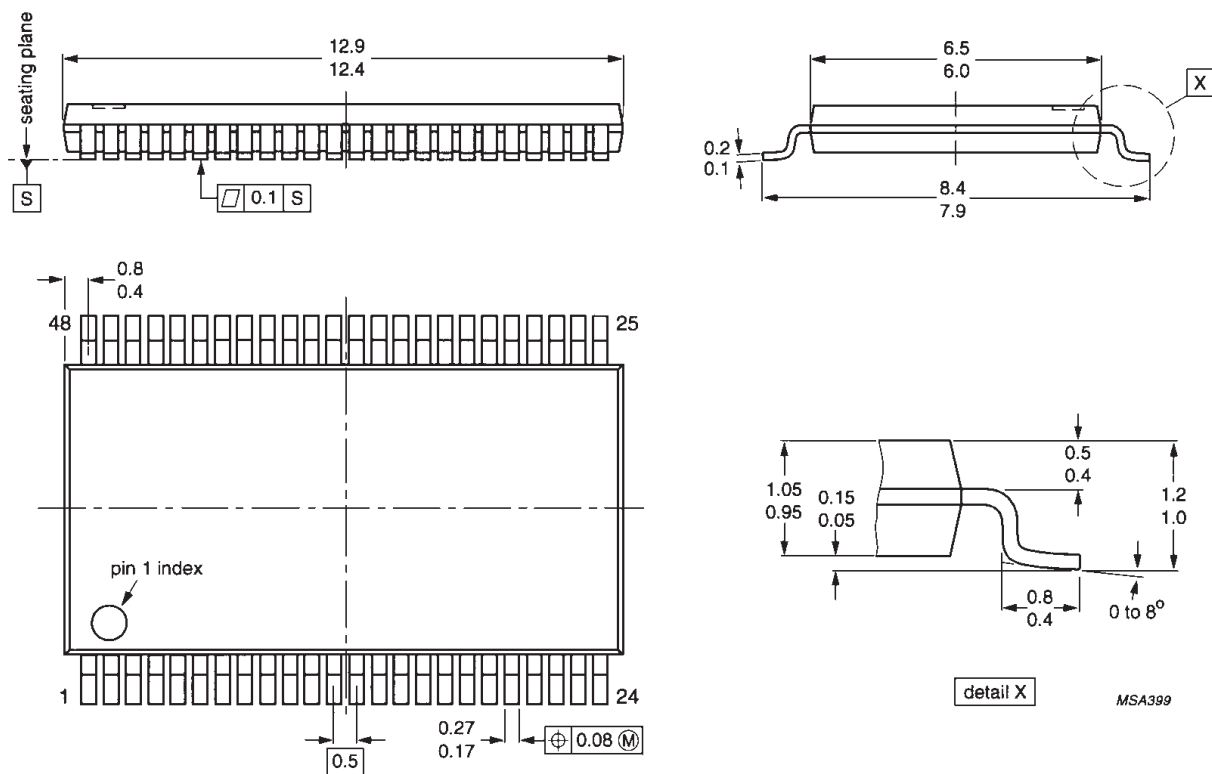


## 16-bit buffer/driver (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



Dimensions in mm.

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**NOTES**

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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