256Kx32 SRAM

FEATURES

- 256Kx32 bit CMOS Static
- DSP Memory Solution
  - ADSP - 21060L (SHARC)
  - ADSP - 21062L (SHARC)
  - TMS320LC31
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17 and 20ns
  - Individual Byte Enables
  - User Configurable Organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC MO-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single 3.3V (±5%) Supply Operation

The EDI8L32256V is a high speed, 3.3 volt, 8 megabit SRAM. The device is available with access times of 12, 15, 17 and 20ns, allowing the creation of a no wait state DSP memory solution.

The device can be configured as a 256Kx32 and used to create a single chip external data memory solution for Texas Instruments' TMS320LC31 (figure 3), or Analog Device's SHARC™ DSP (figure 4).

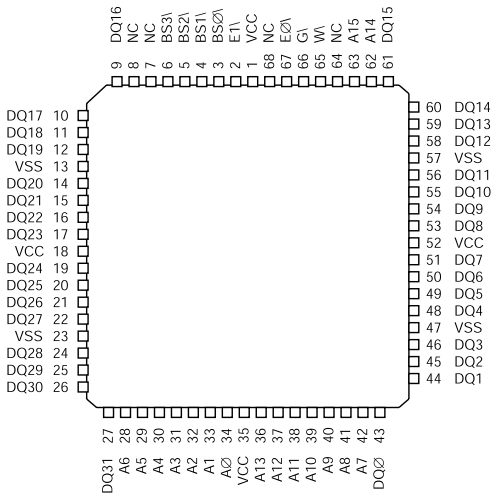
Alternatively the device's chip enables can be used to configure it as a 512Kx16. A 512Kx48 program memory array for Analog's SHARC DSP is created using three devices (figure 5). If this memory is too deep, two 256Kx24s (EDI8L24256V) can be used to create a 256Kx48 array or two 128Kx24s (EDI8L24128V) can be used to create a 128Kx48 array.

The device provides a 32% space savings when compared to two monolithic 256Kx16, 44 pin SOJs.

The device provides a memory upgrade of the EDI8L32128V (128Kx32). For more memory the device can be upgraded to the EDI8L32512V (512Kx32). For additional upgrade information see figure 6.

NOTE: Solder Reflow temperature should not exceed 260°C for 10 seconds.

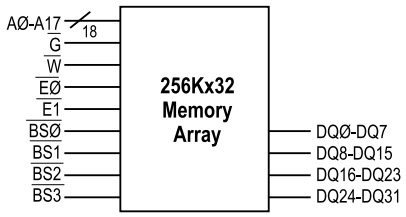
PIN CONFIGURATIONS



PIN DESCRIPTION

AØ-A17	Address Inputs
$\overline{EØ}$-$\overline{E1}$	Chip Enables (One per Word)
$\overline{BSØ}$-$\overline{BS3}$	Byte Selects (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (3.3V±5%)
VSS	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1.7 Watts
Output Current.	20 mA
Junction Temperature, TJ	175°C

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.135	3.3	3.465	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

CAPACITANCE

(F=1.0MHZ, VIN=VCC OR VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	20	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	W, G	6	pF
Chip Enable Lines/Byte Select	E, BS	9	pF

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{BSØ-3}$	Mode	Output	Power
H	X	X	X	Standby	High Z	ICC2,ICC3
L	H	H	X	Output Disable	High Z	ICC1
L	X	X	H	Output Disable	High Z	ICC1
L	H	L	L	Read	DOUT	ICC1
L	L	X	L	Write	DIN	ICC1

X Means Don't Care

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				12/15	17/20	ns
Operating Power Supply Current	ICC1	$\overline{W}$= VIL, II/O = 0mA, Min Cycle		480	440	mA
Standby (TTL) Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH, f=ØMHz		100	100	mA
Full StandbySupply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		20	20	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±10	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±10	±10	µA
Output High Volltage	VOH	IOH = -4.0mA	2.4			V
Output Low Voltage	VOL	IOL = 8.0mA		0.4	0.4	V

AC TEST CIRCUIT

Figure 1

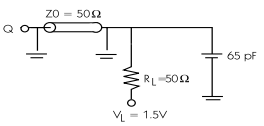
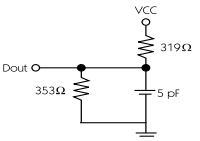


Figure 2



AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, see figure 2)

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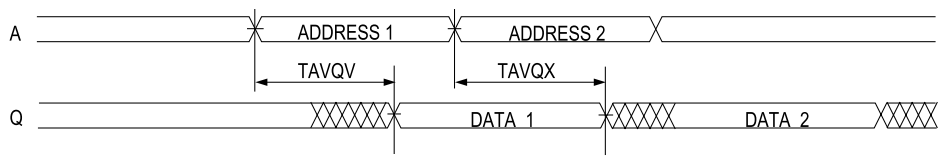
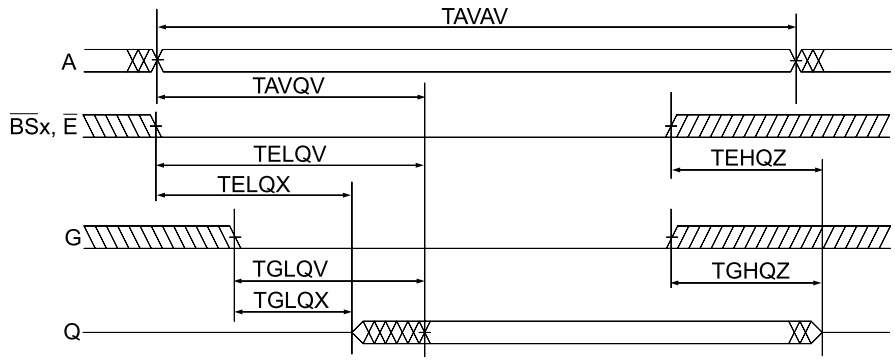
AC CHARACTERISTICS - READ CYCLE

	Symbol		12ns		15ns		17ns		20ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	TAVAV	TRC	12		15		17		20		ns
Address Access Time	TAVQV	TAA		12		15		17		20	ns
Chip Enable Access Time	TELQV	TACS		12		15		17		20	ns
Byte Select Access Time	TBLQX	TBLZ		12		15		17		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Byte Select to Output in Low Z	TBLQX	TBLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		7		8		8		10	ns
Byte Select to Output in High Z	TBHQZ	TBHZ		7		8		8		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		6		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	2		2		2		2		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		4		5		6		8	ns

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW



READ CYCLE 2 - $\overline{W}$ HIGH

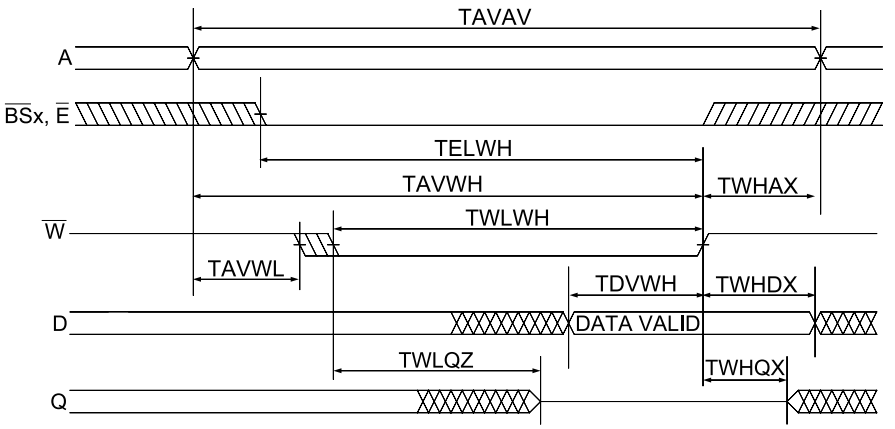


AC CHARACTERTISTICS - WRITE CYCLE

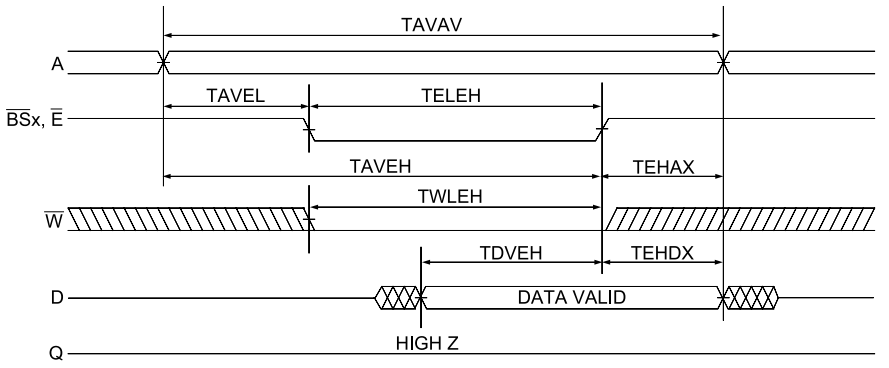
	Symbol		12ns		15ns		17ns		20ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	12		15		17		20		ns
Chip Enable to End of Write	TELWH	TCW	8		12		10		15		ns
	TELEH	TCW	8		12		10		15		ns
Byte Select to End of Write	TBLWH	TBW	8		12		10		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	9		12		12		15		ns
	TAVEH	TAW	9		12		12		15		ns
Write Pulse Width	TWLWH	TWP	9		12		12		15		ns
	TWLEH	TWP	9		12		12		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	7	ns
Data to Write Time	TDVWH	TDW	5		8		8		10		ns
	TDVEH	TDW	5		8		8		10		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		2		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



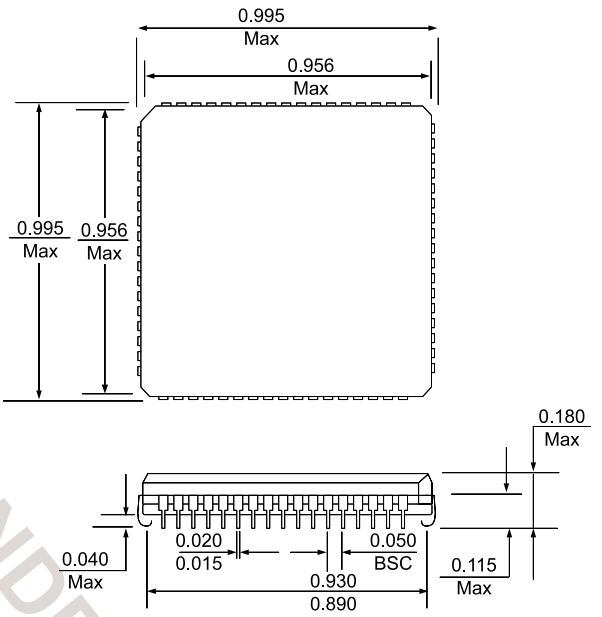
WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



PACKAGE DESCRIPTION

Package No. 99
68 Lead PLCC JEDEC
MO-47AE

Weight = 4.2g
Theta J_A = 40°C/W
Theta J_C = 15°C/W



ORDERING INFORMATION

COMMERCIAL (0°C TO 70°C)

Part Number	Speed (ns)	Package No.
EDI8L32256V12AC	12	99
EDI8L32256V15AC	15	99
EDI8L32256V17AC	17	99
EDI8L32256V20AC	20	99

INDUSTRIAL (-40°C TO +85°C)

Part Number	Speed (ns)	Package No.
EDI8L32256V15AI	15	99
EDI8L32256V17AI	17	99
EDI8L32256V20AI	20	99

Figure 3 - Interfacing the Texas Instruments TMS320LC31 with the EDI8L32256V (256K x 32)

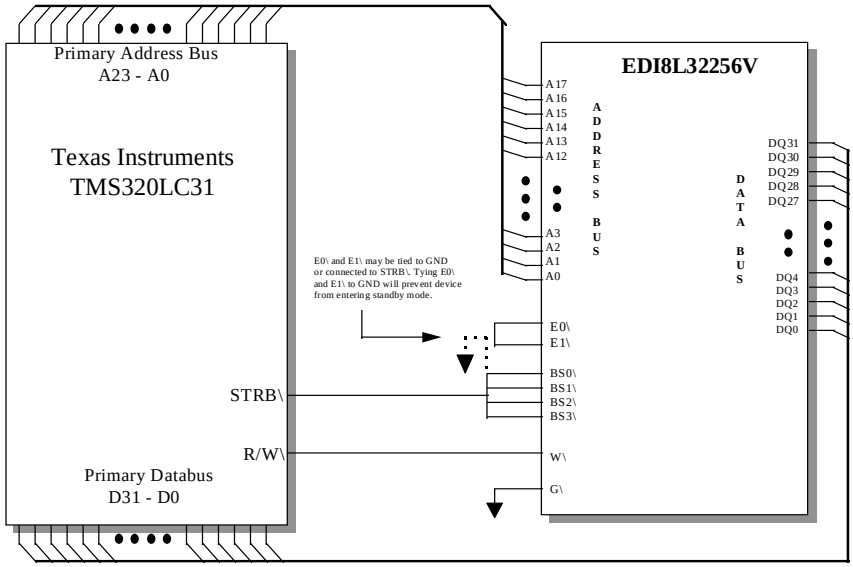


Figure 4 - Interfacing the Analog SHARC DSP w/ the EDI8L32256V (256K x 32 Array)

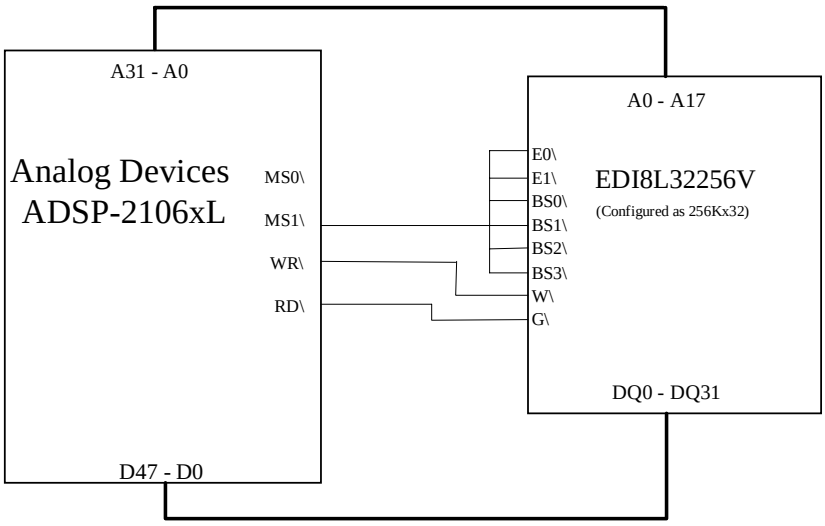


Figure 5 - Interfacing the Analog SHARC DSP w/ the EDI8L32256V (512K x 48 Array)

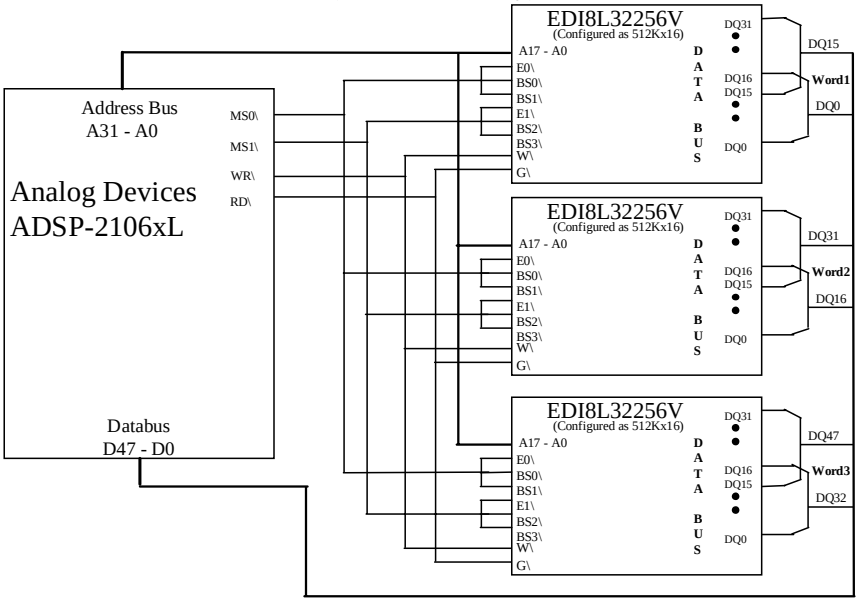


FIGURE 6

512Kx32

256Kx32

128Kx32