

# Dual 4-bit static shift register

## BU4015B / BU4015BF

The BU4015B and BU4015BF are 4-stage static shift registers, each consisting of two circuits.

The D flip-flops for each stage share a common reset input, enabling external asynchronous reset at any point.

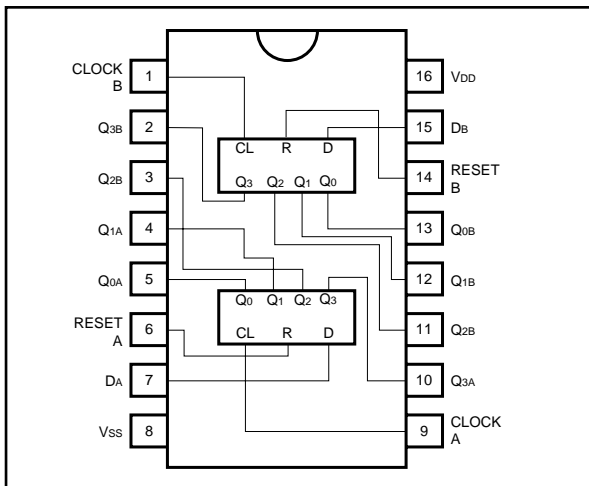
Also, the flip-flops at each stage are triggered by the rising edge of the clock input.

“H” level reset input resets the contents of all stages to “L”, regardless of the clock and data input, and sets data outputs Q0 to Q3 to “L”.

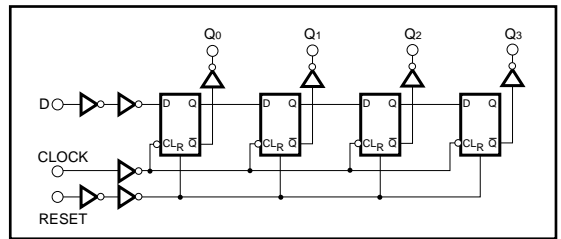
●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Block diagram



●Logic circuit diagram



●Truth table

CLOCK	D	RESET	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
	L	L	L	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
	H	L	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
	X	L	No Change			
X	X	H	L	L	L	L

X : Irrelevant

●Absolute maximum ratings ( $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{DD}$	- 0.3 ~ + 18	V
Power dissipation	$P_d$	1000 (DIP), 500 (SOP)	mW
Operating temperature	$T_{opr}$	- 40 ~ + 85	$^\circ C$
Storage temperature	$T_{stg}$	- 55 ~ + 150	$^\circ C$
Input voltage	$V_{IN}$	- 0.3 ~ $V_{DD} + 0.3$	V

●Electrical characteristics

DC characteristics (unless otherwise noted,  $T_a = 25^\circ C$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
						$V_{DD}$ (V)	
Input high level voltage	$V_{IH}$	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input low level voltage	$V_{IL}$	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input high level current	$I_{IH}$	—	—	0.3	$\mu A$	15	$V_{IH} = 15V$
Input low level current	$I_{IL}$	—	—	- 0.3	$\mu A$	15	$V_{IL} = 0V$
Output high level voltage	$V_{OH}$	4.95	—	—	V	5	$I_o = 0mA$
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	$V_{OL}$	—	—	0.05	V	5	$I_o = 0mA$
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	$I_{OH}$	- 0.16	—	—	mA	5	$V_{OH} = 4.6V$
		- 0.4	—	—		10	$V_{OH} = 9.5V$
		- 1.2	—	—		15	$V_{OH} = 13.5V$
Output low level current	$I_{OL}$	0.44	—	—	mA	5	$V_{OL} = 0.4V$
		1.1	—	—		10	$V_{OL} = 0.5V$
		3.0	—	—		15	$V_{OL} = 1.5V$
Static current dissipation	$I_{DD}$	—	—	20	$\mu A$	5	$V_I = V_{DD}$ or GND
		—	—	40		10	
		—	—	80		15	

Switching characteristics (unless otherwise noted,  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 50\text{pF}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	V <sub>DD</sub> (V)	Conditions
Output rise time	t <sub>TLH</sub>	—	180	—	ns	5	—
		—	90	—		10	
		—	65	—		15	
Output fall time	t <sub>THL</sub>	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Propagation delay time, CLOCK, D→Q	t <sub>PLH</sub> t <sub>PHL</sub>	—	310	—	ns	5	—
		—	125	—		10	
		—	90	—		15	
Propagation delay time, RESET to Q	t <sub>PLH</sub> t <sub>PHL</sub>	—	460	—	ns	5	—
		—	180	—		10	
		—	120	—		15	
Setup time	t <sub>su</sub>	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Minimum clock pulse width	t <sub>WH (CLK)</sub>	—	185	—	ns	5	—
		—	85	—		10	
		—	55	—		15	
Minimum reset pulse width	t <sub>WH (R)</sub>	—	200	—	ns	5	—
		—	80	—		10	
		—	60	—		15	
Maximum clock frequency	f <sub>(CLK) Max.</sub>	—	20	—	MHz	5	—
		—	6.0	—		10	
		—	7.5	—		15	
Maximum clock rise time and fall time	t <sub>r (CLK)</sub> t <sub>f (CLK)</sub>	—	100	—	μs	5	—
		—	40	—		10	
		—	15	—		15	
Input capacitance	C <sub>IN</sub>	—	5	—	pF	—	—

● Measurement circuits

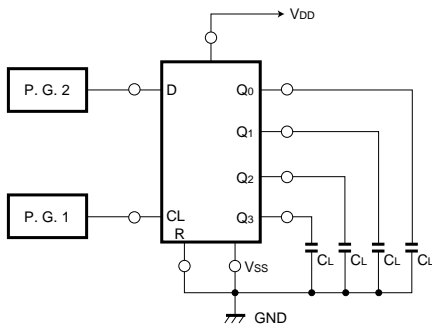


Fig.1 Switching characteristics measurement circuit

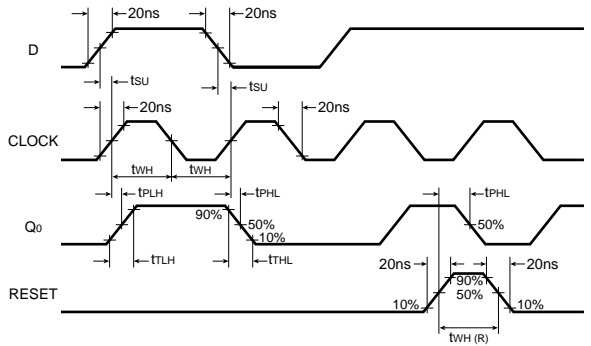


Fig.2 Switching time measurement waveform

● Electrical characteristic curve

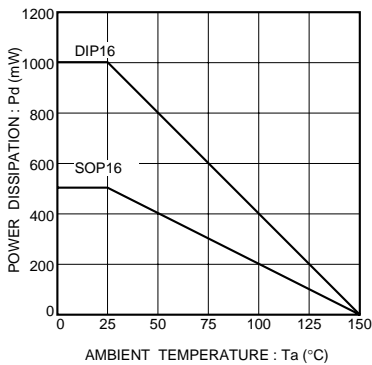


Fig.3 Power dissipation vs. ambient temperature

● External dimensions (Units: mm)

